A Wide Range Level Shifter using a Self Biased Cascode Current Mirror with PTL based Buffer

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ABSTRACT
As demand of handheld devices like multimedia devices, cellular phones, etc. are increasing and we are approaching towards portable devices which are small in size and which requires large battery life. But power dissipation has become most important design factor for VLSI circuits and system in low power devices. So the Level shifter plays very critical role in low power devices. Level shifter is an interfacing circuit which can interface low core voltage to high input-output voltage. The level shifter is used to allow communication between different modules without adding any extra supply pin. This level shifter circuits are uses self biased cascode current mirror and CMOS logic gate. A new family of low power dynamic logic called Data Driven logic is used. The simulation and measurement results were verified using a 22-nm technology.

Keywords
Current Mirror, Level shifter, Subthreshold circuit.

1. INTRODUCTION
Now days the demand of hand-held devices like cellular phones, and private note books etc will increase, therefore the low power consumption has become major design factor for VLSI circuits and system. With increase in power consumption, the price of the packaging additionally will increase. In VLSI circuit, Power consumption is divided in two types, dynamic and static power consumption. Dynamic power has 2 elements i.e. switch power owing to the charging and discharging of the load capacitance and also the contact power owing to the non-zero rise and fall time of the input waveforms. Power consumption of VLSI circuits will be reduced by scaling down voltage and capacitance. With the reduction in voltage, there are issues of voltage swing, noise margin and outpouring currents. The dynamic energy is directly proportional to power supply voltage in CMOS circuits. As the supply voltage increases, the energy consumption is also increases. So the dynamic energy consumption can be reduced by using low voltage power supply in a circuit, without affecting its suitability for the desired purpose. But, when a low supply voltage circuit drives a high voltage circuit, the PMOS presents in the high voltage gate may not turn off completely by the low voltage high logic input. In this case requirement of level shifter arises. The level up shifters is used wherever low supply voltage gates drive high voltage gates. Now a days, the whole circuits can be designed on a single chip and that designing technique is called System on Chip (Soc) in which the entire system can be fabricated on a single chip. However, the fact is different gates present on the chip can use different voltage levels. The output from a high supply voltage gate can be connected to the input of a low supply voltage gate and vice versa. Here the level shifter is the major component of the CMOS devices. One more purpose to use the level shifter circuits is the difference between the voltage levels of core circuits and I/O circuits in multi-voltage devices, where multiple blocks work on different voltages. Therefore, level shifters are necessary when signal passes from one block to another block.

There are various methods available to reduce the power consumption in the circuits. One method for reducing the power is using a supply voltage less than the device threshold voltage, which is referred to as sub-threshold. Because of that sub-threshold voltages, the devices operate at well below the nominal supply voltage that is VDD, so level converters are necessary to interface sub-threshold circuits to core voltage levels. So the current mirror circuit can be used for this purpose, the current mirror is one of the main building blocks of analog and mixed-signal integrated circuits. Another method is to reduce the power consumption in the circuit by using data driven dynamic logic for CMOS OR gate. In this logic style the synchronization clock has been eliminated, and correct sequencing is generated by appropriate use of data instances. So the replacement of the clock with input data gives less power dissipation without speed degradation compared to conventional dynamic logic.

This paper presents a novel level shifter that uses a self biased cascode current mirror with PTL based buffer. The minimum operating voltage of this LS is deep subthreshold which is close to the minimal supply voltage of the digital circuit and maximal operating voltage is standard supply voltage which is defined in a transistor technology. This level shifter is designed for full range conversion as well as bidirectional level conversion.

The rest of the paper is organized as follows. Section 2 introduces different types of level shifters and there comparison with the proposed level shifter; Section 3 presents proposed level shifter structure; Section 4 provides simulation and measurement results of power consumption ; and finally section 5 offers conclusion.

2. SUBTHRESHOLD LEVEL SHIFTER: SURVEYS AND QUALITATIVE COMPARISONS
Subthreshold level shifters are surveyed in this section. The proposed level shifter has compared with five different level shifters. Table I shows five qualities involved in using an LS in wide range DVS applications. The proposed LS satisfy all

five qualities. Each quality and the comparison are described in the next paragraph according to the level shifter.

A cross-coupled structure: Fig. 1(a) shows cross coupled structure for level shifting. A cross-coupled level shifter is differential cascade voltage switch logic for raising a low voltage level. To overcome the leakage of weakly conducting PMOS transistors, drive strength of NMOS transistor is enhanced. The operating range of CC LSs depends only on the transistor threshold voltage (Vt) and size; but, the operating range of CC LSs is difficult to extend to the subthreshold region because the NMOS drive strength decreases exponentially. CC LSs require an exponential increase in NMOS transistor size, for converting a subthreshold voltage, which is impractical. So the subthreshold level conversion is not possible for small area. This level shifter supports bidirectional level conversion but full range bidirectional level conversion is somewhat challenging. Pull-up and pull-down strength must be analyzed for all combinations of input and output levels. Therefore, it has limited bidirectional regions because of unbalanced pull-up and pull-down strength.

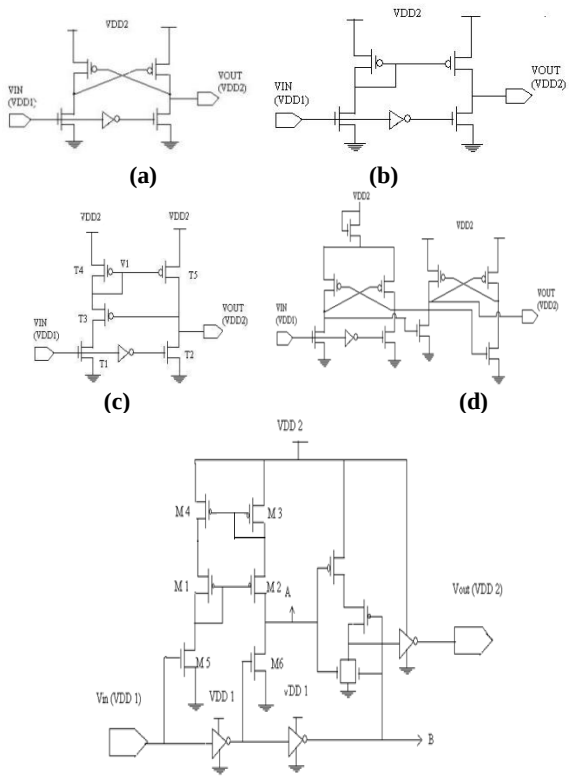


Fig. 1 Conventional level shifters using (a) a cross coupled structure (CC); (b) a current mirror structure (CM); (c) a Wilsons current mirror structure (WCM); (d) a two stage cross coupled structure (TSCC); (e) a modified Wilsons current mirror structure

A Current Mirror structure: Fig. 1(b) shows a LS that uses a basic current mirror (CM). This can convert a deep subthreshold level because a high drain-to-source voltage of PMOS transistors facilitates the construction of a stable current mirror, which offers an effective on-off current comparison at the output node. However, when the input voltage is suprathreshold, a high amount of quiescent current occurs. Because of this high power consumption limits the use of the conventional CM LS. A CM LS has a high quiescent current because of the bias currents.

Wilson current mirror structure: Fig. 1(c) shows Wilson current mirror (WCM) structure, which reduces the power consumption under a suprathreshold input.

Table I: Qualitative Comparisons For Subthreshold and Wide-Range Level Conversion

Criteria	CC	CM	WCM [3]	TSCC [6]	MWCM [4]	Proposed
1 .Small area for sub.vt. LC		√	√	√	√	√
2. Low power	√		√	√		√
3.Bidirectional LC.	√	√		√	√	√
4. Size & vt Insensitivity		√	√		√	√
5. Balanced Rising falling Delay	√	√		√	√	√

Here Balanced rising and falling delay ensures a 50% signal duty cycle. When input and output levels are close to each other, the duty cycle of the WCM LS is problematic. The WCM LS has a long rising delay, Because of a weak Pull up network, which is up to one hundred times longer than the falling delay. So the signal skew arises.

Two stage cross coupled structure: Fig. 1(d) shows a two-stage CC LS (TSCC), in which the pull-up driving strength is reduced by a header NMOS, which expands the convertible input voltage. Operating range of the LS is determined by the transistor size and the Vt. As this is two stages cross coupling structure so the size automatically gets increases.

Modified Wilson current mirror structure: Fig. 1(e) shows modified Wilson current mirror structure. This level shifter also satisfy basic criterion that is small area for threshold level conversion. Bidirectional level conversion is possible; that is input and output levels can be scaled independently. This structure also balances the rising and falling delay. This provides less power consumption.

3. PROPOSED LEVEL SHIFTER STRUCTURE

The proposed level shifter is a hybrid structured having Self biased cascode current mirror; CMOS logic gate and PTL based buffers. With the help of self biased cascode current mirror, the levels of voltage/current increases easily than the mirror circuit. It is also useful for low voltage analog and mixed mode circuit. The cascode connection is an effective method to suppress the channel length modulation. It also reduces the ratio errors due to difference in output and input voltages. The advantages of the cascode arrangement are it provides higher output impedance and it reduces the effect of miller capacitance on the input. The biasing technique is applied to keep the cascode transistor always operating in the saturation region so that the high precision and high output impedance can be maintained over a large operating range.

Pass transistor logic style is more power efficient than the CMOS logic style. The basic difference between the pass transistor logic style and CMOS logic style is that the source

side of the logic transistor is connected to the some input signals instead of the power supply. In this logic style one pass transistor is sufficient to perform the whole logic operation, which reduces the number of transistors. In CMOS inverter, the tripping of the inverter is depends upon the input. When input is LOW, the output of the inverter is HIGH. When input is HIGH, the output of the inverter is LOW. But in Pass transistor logic the output of the inverter depends upon the input as well as the circuit input.

Current mirror is the basic building block, which is widely used in analog VLSI design. Sensitivity and temperature variation should be very less for high performance analog circuit applications. Also it has the wide range of the working frequency. The proposed level shifter structure is shown in Fig. 2.

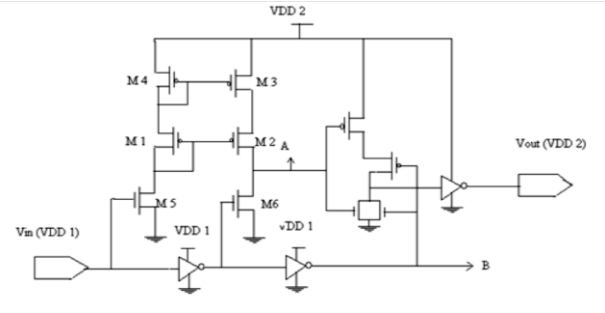
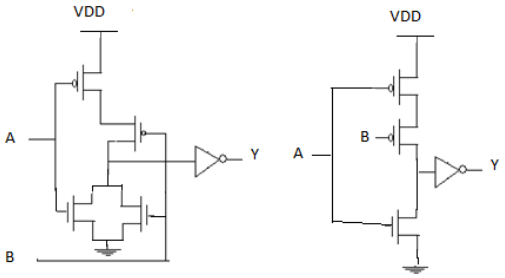


Fig.2 Proposed circuit diagram

A cascode current mirror is located with the help of transistors M1, M2, M3 and M4. The level shifter can be divided in three main blocks; first modified Wilsons current mirror; second delay circuit and third one is the CMOS OR gate. Here modified Wilsons current mirror circuit balances the rising and falling delay but when input and output levels are close to each other then there is a problem skews that is cascade PMOS has insufficient drive currents which increases the rising delay. To reduce the rising delay, a delay path is designed. This delay path is designed with the help of inverters which acts as a buffer. At last the CMOS OR gate is there in output stage which gives proper output, and limits the leakage current. When VDD1 is sub-threshold and VDD2 is high, the cascode current mirror structure balances the rising and falling delay at Node A, without losing the original static bias. The CM-type structure provides a wide operating range, and the stacked PMOS transistors in the complementary OR gate limit the leakage current.

There are two types of OR gates used in this circuit. First one is simple CMOS OR gate using static logic and other one is CMOS OR gate using dynamic logic that is Data driven dynamic logic [8]. When creating conventional dynamic logic gates, in which one of the PDN or PUN of static logic is removed and a set of conditions must be imposed on the inputs. In a Domino logic block, all of the inputs must be low in precharge phase, but in NP-CMOS all inputs to a P-block must be high in the precharge phase. It means the corresponding gate is precharged with a combination of input data, and then there is no need for a clock signal. Instead of clock precharging such a use of data precharging can be used. Therefore this logic style is called as Data-Driven Dynamic Logic or D3L. In D3L the clock signal is replaced by one or more inputs. For implementing n-input CMOS logic gate, 2n transistors required while D3L style requires only n+2 transistors. Fig. 3 Shows the an example where the OR gate is designed by two logic styles, from this it is clear that by the number of transistors get reduced by using D3L logic, so reduction in silicon area.



(a) Using CMOS Logic Style (b) Using Data Driven Dynamic Logic Style

Fig. 3 OR gate

According to this dynamic approach the area and smaller parasitic capacitance get reduces, so the power dissipation and speed are improved. When input voltage increases, the rising signal from Nodes A and B that achieves the trip-point voltage more quickly triggers the rise of VOUT. When VDD2 is higher than VDD1, then the voltage level at the point A get increases. When VDD2 is lower than VDD1, then the voltage level at the point B get increases. When VDD2 is considerably greater than VDD1, the cascode current mirror has similar rising and falling delays. To balance the rising and falling delay when VDD2 is less than VDD1, two VDD1 inverters are used long channel length. All low-Vt transistors (LVTs) were used for performance analysis. Using these LVTs reduces circuit delay and power consumption in the circuit. When the input level is ultra-low and has a slow slew rate at that time it has high short circuit power. In this level shifter, NMOS LVTs reduces the transition time and short-circuit power consumption where as PMOS LVTs reduces the rising delay and the voltage drop.

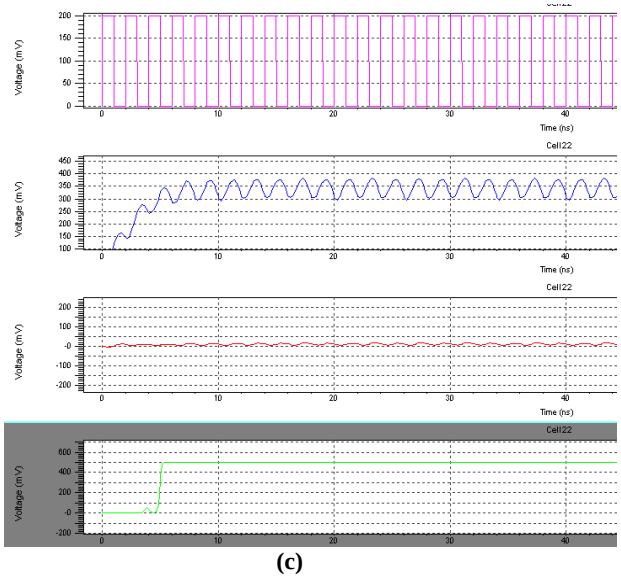
4. SIMULATION AND MEASUREMENT RESULTS

Tanner tool is used for the simulation of the proposed level shifter circuit. The simulation and measurement results were verified using 22-nm technology. The minimal operating range for the proposed level shifter circuit in less than 200mv.

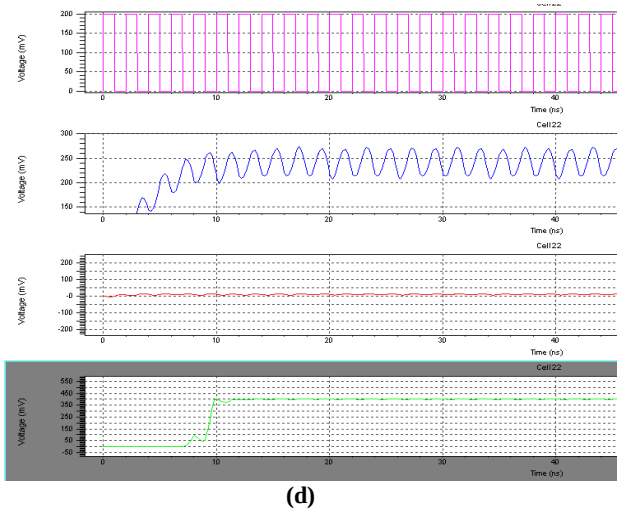
Fig. 4 shows four simulation waveform of the proposed level shifter circuit. Here the input of the level shifter is constant at 200mv. The VDD2 levels are 1200mv, 800mv, 500mv and 400mv, as shown in fig. 4 (a)-(d). In 22-nm technology the ΔV that is the voltage drop is 100mv.

(a)

(b)



(c)



(d)

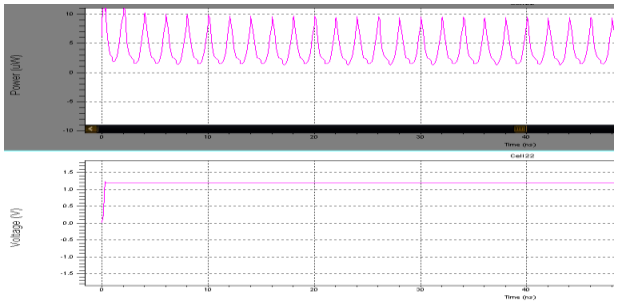
Fig 4. Simulation waveform and corresponding power consumption: (a) 200mv-1200mv (b) 200mv-800mv (c) 200mv-500mv (d) 200mv-400mv

Table II shows the details of the power consumption of the proposed level shifter circuit.

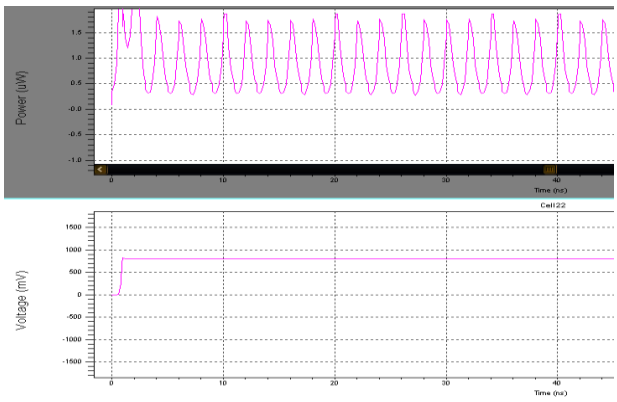
Table II Power consumption details

VDD2 / VDD1	0.1	0.2	0.3	0.4	0.5	0.8	1.2
0.1	0.61	2.64	7	15.93	31.9	0.15u	1.10u
0.2	1.37	9.68	29.9	77.95	142.8	0.89	4.03
0.3	1.08	9.26	25.92	51.75	95.03	1.13	9.11
0.4	1.14	9.26	26	51.97	95.59	0.48	2.72
0.5	1.13	9.26	26.2	52.2	96.19	0.49	2.72
0.6	0.97	8.65	26.11	52.83	97.39	0.49	2.73
0.7	0.82	7.78	25.28	52.45	98.91	0.49	2.73
0.8	0.7	6.97	24.22	50.68	95.57	0.49	2.73
0.9	0.61	6.24	23.13	48.75	92.37	0.47	2.73
1	0.52	5.51	21.88	46.66	88.5	0.45	2.73
1.1	0.43	4.75	20.42	44.34	84.33	0.43	2.74
1.2	0.38	4.22	19.29	42.63	81.14	0.41	2.75
Power in nw							

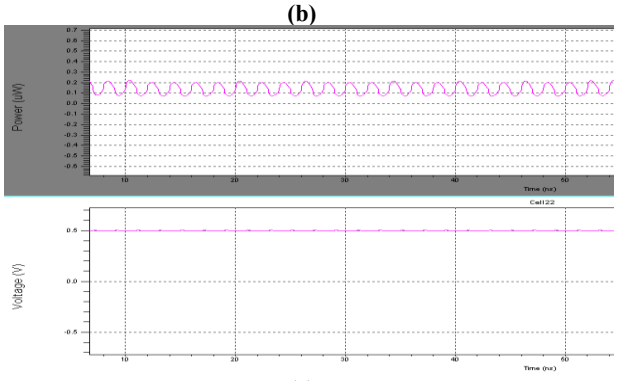
Fig. 5 shows the graphical representation of power consumption for input that is constant 200mv and the VDD2 which is 1200mv, 800mv, 500mv, and 400mv respectively.



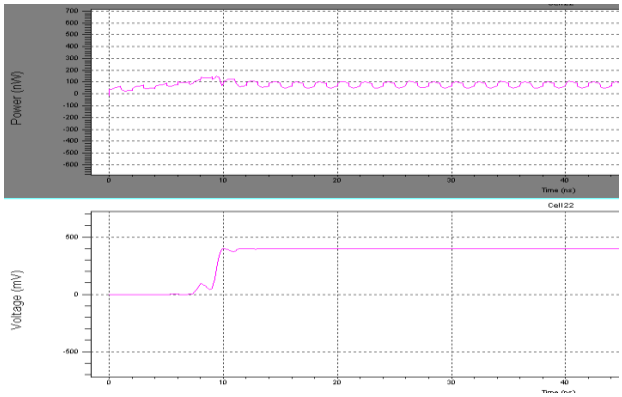
(a)



(b)



(c)



(d)

Fig 5. Simulation waveform of corresponding power consumption: (a) 200mv-1200mv (b) 200mv-800mv (c) 200mv-500mv (d) 200mv-400mv

5. CONCLUSION

In this paper, A Wide range level shifter using self biased cascade current mirror with PTL based buffer is presented. This is used for various applications where the ultra low power is required. This self cascode current mirror with PTL based level shifter is designed for full rang and bidirectional level conversion. The minimal operating voltage is the deep sub-threshold voltage, close to the minimal supply voltage of the digital circuit and the maximal operating voltage is the standard supply voltage defined in transistor technology. Here the minimum operating voltage in 200mv. The power consumption of the proposed level shifter is verified using 22nm technology. A new dynamic logic style called Data-Driven Dynamic Logic, or D3L has been discussed in this paper. D3L is an improved type of dynamic logic in which precharge and evaluation phases are performed under control of input data and without an explicit clock. With the help of this logic style inverting functions also implemented. So for the future scope, this Data-Driven Dynamic Logic can be used to design OR gate which increases the speed and reduces the power consumption.

6. REFERENCES

[1] K. Hagihara J. Y. Sugimoto, F. Ino. Performance analysis of various level shifters using lecc. International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, 2(4), 2013.

[2] M. Alioto. Ultra-low power vlsi circuit design demystiffed and explained: A tutorial. IEEE Trans. Circuits Syst. I, 59(1), Jan 2012.

[3] Sven Liutkemeier and Ulrich Riuckert. A subthreshold to above-threshold level shifter comprising a wilson current mirror. IEEE TRANSACTIONS ON CIR- CUITS AND SYSTEMS|II, 57(9):721 724, 2010.

[4] Ching-Ji HuangYuan-Hua Chu Shien-Chun Luo. A wide-range level shifter using a modiffed wilson current mirror hybrid buffer. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS 2004.

[5] R. Rufati', S. M. Fukhraie', K. C. Smith2Low-Power Data-Driven Dynamic Logic (D3L) ISCAS 2000 - IEEE international Symposium on Circuits and Systems, May 28-31, 2000.

[6] S. N. Wooters, B. H. Calhoun, and T. N. Blalock, "An energy-efficient subthreshold level converter in 130-nm CMOS," IEEE Trans Circuits Syst. II, Exp. Briefs, vol. 57, no. 4, pp. 290–294, Apr. 2010.

[7] M. Lanuzza, P. Corsonello, and S. Perri, "Low-power level shifter for multi-supply voltage designs," IEEE Trans Circuits Syst. II, Exp. Briefs, vol. 59, no. 12, pp. 922–926, Dec. 2012.

[8] Low-Power Data-Driven Dynamic Logic (D3L)R. Rufati', S. M. Fukhraie', K. C. Smith2 ISCAS 2000 - IEEE international Symposium on Circuits and Systems, May 28-31, 2000, Geneva, Switzerland.

[9] A. Hasanbegovic and S. Aunet, "Low-power subthreshold to above threshold level shifter in 90 nm process," in Proc. Conf. NORCHIP, 2009, pp. 1–4.