Realization of Analog Circuits using Double Gate MOSFET at 32nm CMOS Technology

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ABSTRACT
In this paper, design of analog circuit using double gate (DG) MOSFET where the front gate output is changed by control voltage on the back gate. The DG devices can be used to improve the performance and reduce the power dissipation when the front gate and back gate both are independently controlled. The analysis of the analog circuits such as CMOS amplifier pair, Schmitt trigger circuit and operational trans-conductance amplifier. Transient response and output DC response of analog tunable circuits are going to be analyzed. These circuit blocks are used for low-noise, high performance integrated circuits for analog and mixed-signal applications. The design and simulation results are predicted by Microwind tool in 32nm complementary metal oxide semiconductor (CMOS) technology.

Keywords
Analog Circuits, Double Gate, Transient and output DC response

1. INTRODUCTION
Electronic devices and instruments touch our lives in more than one way these days. They come across as extremely important and almost indispensable in many of our daily activities. Their performance, functionality and accessibility define many facets of our daily productivity. At another level, companies designing and manufacturing electronic systems drive whole economies of many parts of the world, both in the developed and developing countries. Thus research and development of better and more capable electronic circuits is an extremely important and continuously evolving process ever since the dawn of the electronics age. Major milestones in the electronic revolution involve the discovery of high purity semiconductor materials such as silicon, development of modern fabrication techniques and the development of the integrated circuit (IC) technology. The development of IC technology has successfully harnessed the metal oxide field effect transistors (MOSFETs) to give birth to miniature, reliable and power efficient circuits. With the improvements in MOSFET designs over the years, ICs have continued to evolve to be faster, cheaper and better. As per the Moore's law, the number of transistors on a chip would double every 24 months. Thus, in the future we are looking at several billion transistors on a single chip, and each transistor thus would be no more than 20 nanometers in size. Such high levels of miniaturization put a tremendous strain on the device engineers and researchers who continue to confront the law of physics and limits of technology in allowing the transistors to be progressively scaled down. They need to continuously develop new transistor architectures that can perform better with each passing and are able to cope with the demands of modern analog and digital circuit designs without affecting their signal integrity or increasing their power requirements. Several solution exist on the drawing board, some of them revolutionary like molecular transistors, nano-wires and nano-tube transistors [4][5] while others build upon current technologies like FinFETs, multi-gate transistors etc. [6]. It remains to be seen if all these technologies hold long-term feasibility or not, but building upon existing MOSFET technology seems to be a highly attractive notion in the near future due to the evolutionary nature of the latter, avoiding a more radical bottoms up approach required by the former.

Scaling of the CMOS technology have reached to nanometer, therefore the double gate (DG) MOSFETs have replaced the single gate (SG) MOSFETs [4, 5]. Double-gate (DG) SOI MOSFET has tremendous short-channel effect (SCE) immunity, higher trans-conductance and ideal sub threshold voltage [1-3]. Whereas DG MOSFETs are ideal for digital performance, they will also be strong competitors for linear radio frequency (RF) applications such as wireless communication market because of their ability to handle large gigahertz modulation [7]. Due to analog tunable functionality, these circuits provide extra gains in terms of area, power and speed by using DG-MOSFET in independently driven mode (IDDG) where the two gates are separated and biased in a different way as compared to symmetrically driven mode (SDDG) counterparts used in digital applications to maximize ION/IOFF ratio[6, 8]. The tunability of the DG-MOSFETs has been largely ignored by the analog designers because utilities of the DG-MOSFETs in RF mixing applications have been published [8-10]. In this work, we will realize various analog circuit blocks ramped up using DG-MOSFETs, where back gate will be used for the tuned circuit performance.

2. DOUBLE GATE MOSFET
Double Gate MOSFET (DG-MOSFET) is a unique variation on the conventional MOSFET architecture with two gates controlling the channel instead of the usual single gate. Sekigawa first put the concept of the DG-MOSFET forth in 1984. The DGMOSFET holds a great promise for nanometer scale transistors in highly dense IC architecture. The basic concept of the DG-MOSFET involves placing two gate terminals at the top and bottom of the channel in an ultra thin SOI body, thereby allowing effective gate control over the channel from both the gates. The increased gate control enhances the "ON" state drain to source current (Id) and in the "OFF" state would prevent leakage current to flow between the drain and source terminals. It reduces the SCE in the process and has a higher ON-OFF ratio as compared to a conventional MOSFET.

In double gate MOSFET (DGMOSFET), Si channel is very small in width and can be controlled by applying gate control on both sides of channel. In double gate device both gate are

coupled each other and this reduce the short channel effect andleakage. By using two gates circuit with double gate transistor can be operated as low input voltage as compared to the planer CMOS circuit and these means low power consumption. Gate leakage is also low in double gate device [13]. It is occur due to gate tunneling and overlap tunneling current. Here short channel effect is controlled by two gates so there is no need of heavy doping. Since very light doped or undoped channel can be used in double gate transistors.

The figure 1 below shows the basic conceptual model of a Double Gate MOSFET.

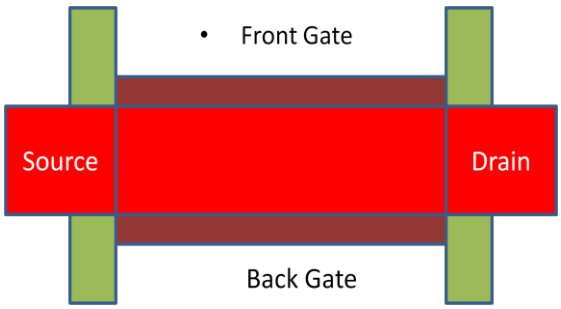

Fig.1 DG-MOSFET device structure

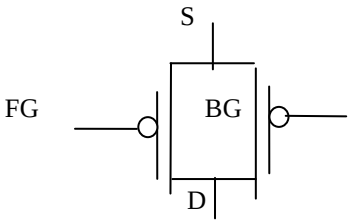

Fig.2 (a) P-type DG-MOSFET

In this design DG-MOSFETs have minimum body thickness ($t_{si} \leq 10$nm), oxide insulator thickness ($t_{ox} \leq 2.2$nm), gate length ($L_g \leq 32$nm) and the maximum Ion/Ioff ratio because greater controllability to OFF state leakage current. Figure 1 & 2(a), 2(b) shows the DG-MOSFET device structure and p-type and n-type DG-MOSFETs transistors.

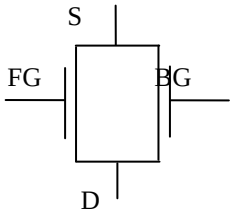

Fig. 2(b) N-type DG-MOSFET

The double gate (DG) is operating in two modes such as Symmetrical driven mode (SDDG) and independent driven (IDDG) mode double gate MOSFET to design analog circuits. In SDDG, the front and back gates are connected together as shown below.

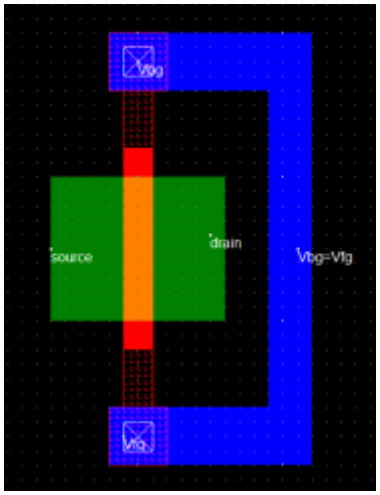

Fig.3 (a) Layout of SSDG-MOSFET

In IDDG mode, separate biasing are provided to both the front and back gates as shown below

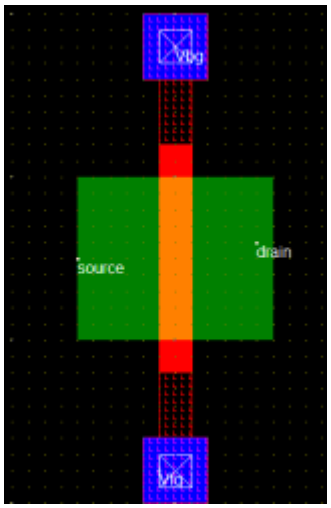

Fig. 3 (b) Layout of IDDG-MOSFET

In SDDG inverters (front and back gates tied), which would have higher performance (frequency) but no tunability. The effect of back bias control however can be best studied when the amplifier is operated in the IDDG mode with independent biasing for the back gates. This can be done in two ways: i) the back gates may be tied together to the same bias voltage in single control mode or ii) each one of the back connected independently to a different bias voltages in the dual control modes.

3. DESIGN OF ANALOG CIRCUITS

3.1 CMOS Amplifier circuit

In the analog circuit designing, the CMOS Amplifier is the key element which determines the overall performances of many analog and mixed circuits. The DG CMOS inverter pair can serve as a high-gain push-pull amplifier when biased in the transition region. Depending on the selection of the sign and magnitude of the bottom-gate bias, the simple amplifier's characteristics can be altered in a number of ways, which greatly enhances the variety of applications for this otherwise simple circuit. The voltage applied on the gate terminals controls the electric field, determining the amount of current flow through the channel. The layout representation of CMOS Amplifier using Double gate (DG)-MOSFET as shown below

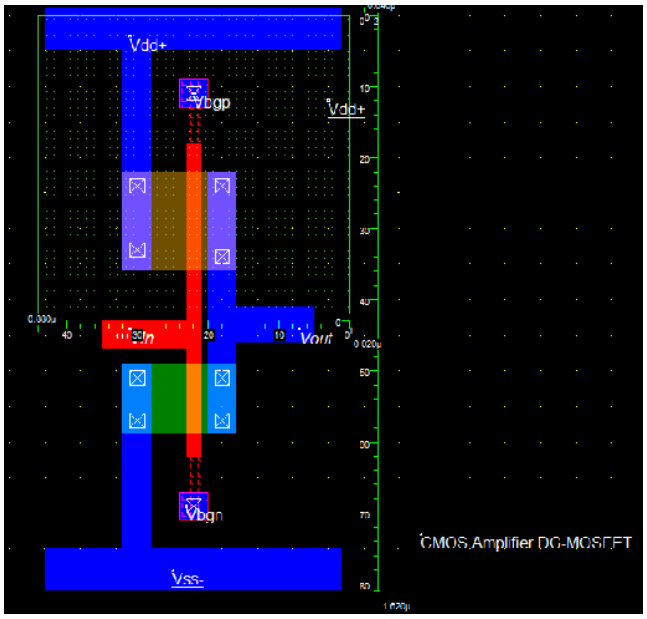

Fig. 3.1 Layout of DG MOSFET CMOS Amplifier circuit

For instance, Fig.3.1 (a) shows the transient response of CMOS amplifier DG-MOSFET, by an alternative scheme for programming the CMOS pair in conjugate bias, whereby the two complementary back-gates are driven by separate signals of equal magnitude but opposite polarity, i.e. Vbgn = - Vbgp. In a mixed-mode design using bipolar supply voltages, this biasing scheme is indeed possible and provides a method of varying the amplifier gain. Similarly Fig.3.1 (b) shows the output DC response of DG-MOSFET CMOS amplifier.

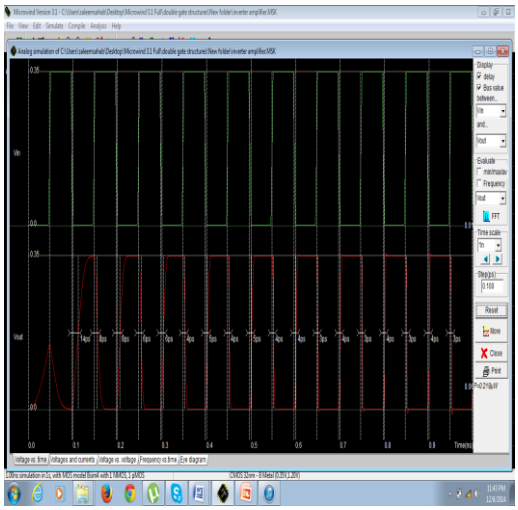

Fig.3.1(a) Transient response of CMOS DG-MOSFET amplifier

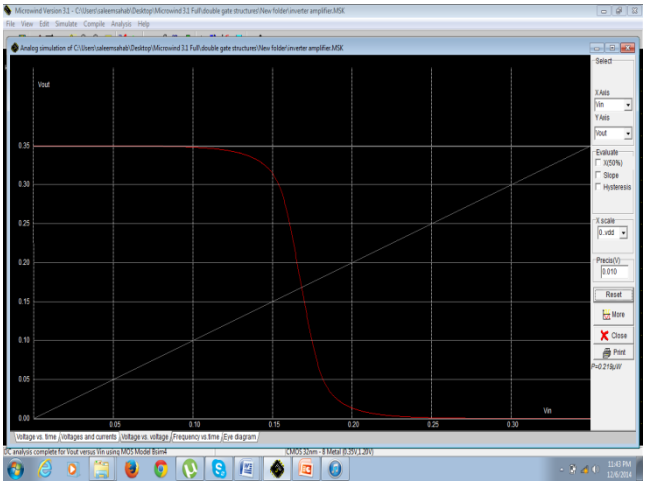

Fig.3.1 (b) Output DC response of CMOS DG-MOSFET amplifier

3.2 SCHMITT TRIGGER CIRCUIT

Schmitt-trigger inputs offer improved noise immunity during switching transitions, which is especially useful on analog mixed-mode designs. Schmitt-trigger inputs reject input noise, ensure integrity of output signals, and allow for slow input signal transition. Schmitt Trigger circuit is a nonlinear analog circuit block. In single gate (SG) MOSFET, the sizes of Schmitt Triggers are improved (to reduce the rise times and fall times of signals) due to increased layout area and power consumption of chips. Double gate (DG) Schmitt Trigger has the ability to reduce layout area, power consumption and used in static memory applications in digital circuits [14]. In DG Schmitt Trigger, we use only 4 DG MOSFETs as compared to 6 MOSFETs in traditional CMOS design [14, 15]. In Fig. 3 (b) shows two stage CMOS circuit where conjugate biasing of the second stage (Vsetp = -Vsetn) used to shift the first stage's output to two opposite extremes.

The transient response of the Schmitt Trigger circuit is as shown in Fig.3.2 (a). The conjugate bias required to set the two extremes, i.e. the width of the hysteresis, can be decided from Fig.3.1 (b). The relatively large gain of the second stage is a key here in producing a very large hysteresis width. To design a small hysteresis, application of a relatively large conjugate bias may be needed, limiting the output swing of the second stage or the amount of shift for the first stage. An upper limit for the resulting power savings in this Schmitt Trigger circuit with four transistors is expected to be around 11% to 14% as shown by earlier works (Cakici et al., 2003).

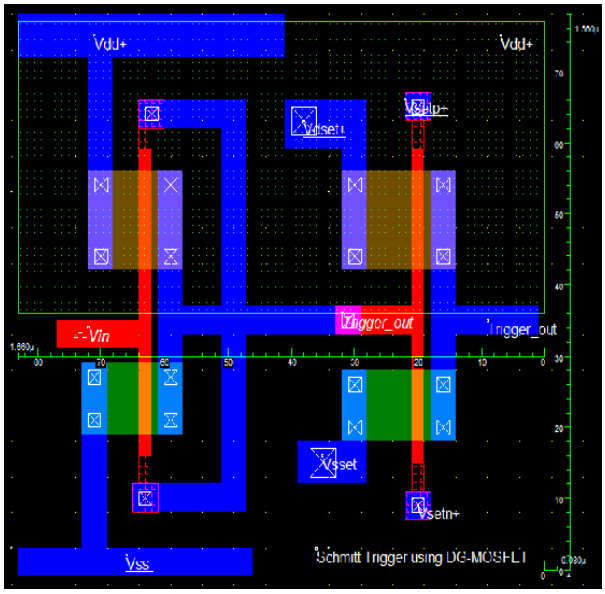

Fig.3.2 Layout of Schmitt triggers using DG-MOSFET

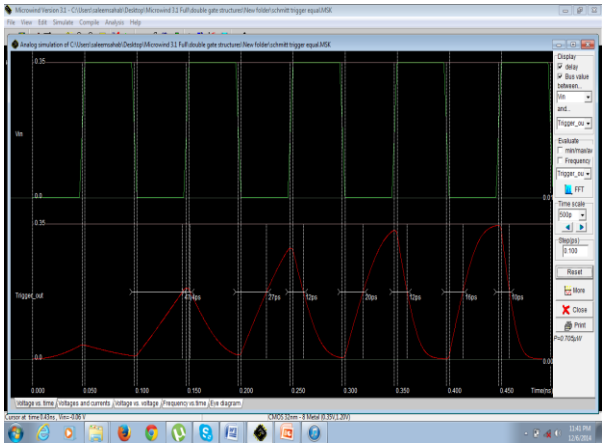

Fig.3.2(a) Transient response of Schmitt triggers DG-MOSFET

It is also possible to scale the whole hysteresis by adopting a different topology in the second stage. In this case the rail voltages are the programmable nodes (Vdset and Vsset), and the back gates are tied to front gates (Vsetp=Vsetn=Vout1), i.e., the SDDG inverter configuration. The output DC response of Schmitt triggers using DG-MOSFET are given in Fig.3.2 (b) for a conjugate bias voltage the hysteresis is scaled both vertically and horizontally as the feedback voltage from the output of the second stage changes. Also, the gain of the second stage is higher, resulting in a non-inverting Schmitt trigger with almost ideal shapes and more spacing between them.

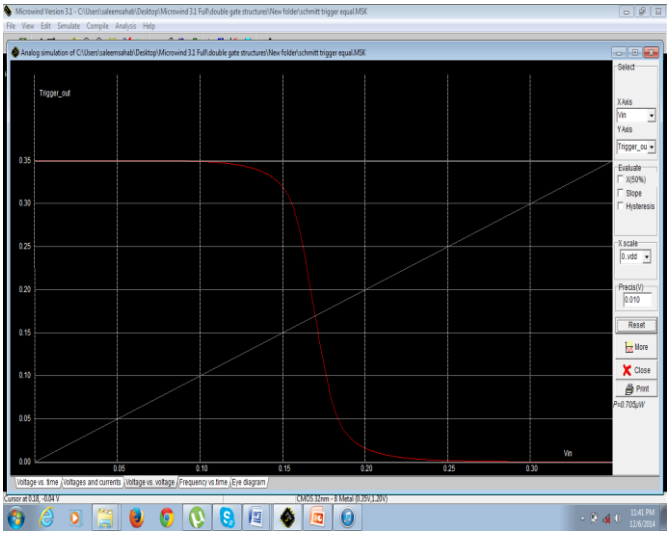

Fig.3.2 (b) Output DC response of Schmitt triggers using DG-MOSFET

3.3 OPERATIONAL TRANS-CONDUCTANCE AMPLIFIER (OTA) CIRCUIT

OTA is a voltage controlled current source, its takes the difference of the two voltages as the input for the current conversion. There is an additional input for a current to control the amplifier's transconductance. The OTA is an amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source (VCCS). There is usually an additional input for a current to control the amplifier's transconductance. OTA have become increasingly popular in the last two decades due to ease of design and reduction in circuit complexity compared to operational voltage amplifiers in certain applications and also they often drive a capacitive load in a compact OTA-C block Fig.3.3 shows a simple OTA structure modified from conventional MOSFET that can act as very efficient integrators and appear also in other filter elements. Since the back-gate biasing in DG-CMOS architecture offers real advantages to current mode circuit design to alter circuit operation with minimal intrusion, the OTAs with current outputs are set best for taking advantage of the tunability in amplifier designs. Conventional MOSFET, which required 6 transistors [16] as compared to 4 DG MOSFET used in Fig. 3.3. The availability of the individual back gates allows the elimination of the two extra transistors for transconductance (gm) tuning across the two branches of the OTA, which should save both power and area while also minimizing the parasitic.

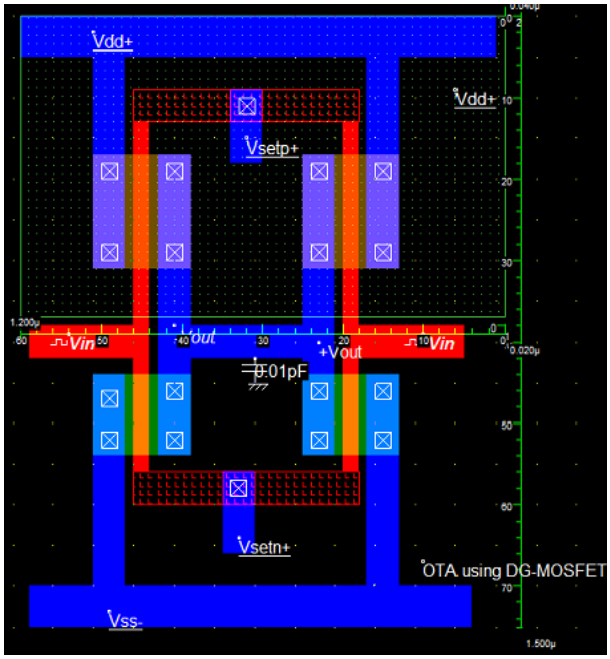

Fig.3.3 Layout of Operational Trans-conductance Amplifier using DG-MOSFET

Similar to CMOS amplifier case, there are two tuning methods available to this simple operational trans-conductance amplifier (OTA) circuit such as 1) asymmetric bias (Vsetn ≠ Vsetp) to shift the frequency response or 2) a conjugate bias (Vsetn = -Vsetp) to change the trans-conductance(g_m). When a conjugate bias is used to tune the OTA, we can conveniently shift the frequency response. For a fixed realistic load of CL = 10 fF and Vsetp=−Vsetn=0.35V, the resulting OTA-C circuit serves as a low-pass filter with a corner frequency 5 GHz, as shown in Fig.3.3(a). The same corner frequency can be tuned almost a decade depending on the asymmetric bias on the back gates. This simple but powerful example aptly illustrates the potential of DG-MOSFET analog circuits.

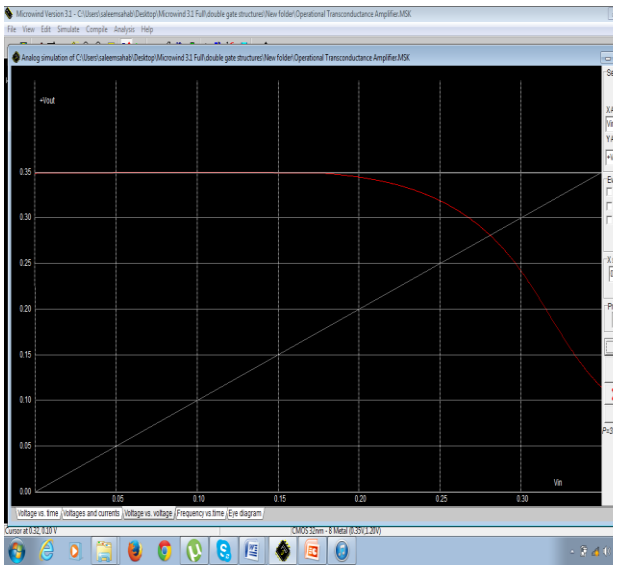

Fig.3.3 (a) Output DC response of OTA DG-MOSFET

4. CONCLUSION

Low power analog circuit using double gate MOSFET at 32nm have been analyzed. Layout design and simulation results were performed using Microwind tool, also shown design and test of analog circuit with tunable performance metrics using back gate of an IDDG MOSFET is better than SDDG MOSFET. Analog circuit blocks such as CMOS amplifier, a Schmitt Trigger circuit and an OTA circuit have been analyzed. In all cases, by varying the back gate bias conditions to provide the transient response and output DC response of these building blocks which has tunable performance, thanks to the DG-CMOS devices expected to make a big impact in the final stretch of Si scaling. Especially in the independently driven configuration, the DG devices are capable of providing the design latitude and flexibility that will be especially valuable when conventional circuits cannot be further pursued due to matching problems & power dissipation.

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