Design of Adaptive Hold Logic (AHL) Circuit to Reduce Aging Effects

Vaishali S. Chirde
PG Student Department of ENTC
D.Y. Patil College of Engineering.
Akurdi, Pune

Usha Jadhav
Assistant Professor Department of ENTC
D.Y. Patil College of Engineering.
Akurdi, Pune

ABSTRACT
In VLSI, scaling methods plays an important role in reducing the power dissipation from one technology node to other technology node. The two major constraints for delay in any VLSI circuits are latency and throughput. The negative bias temperature instability (NBTI) effect occurs when a pMOS transistor is under negative bias (V_{gs}= -V_{DD}) increasing the threshold voltage of pMOS transistor and reducing the speed. A similar phenomenon, positive bias temperature instability (PBTI) effect occurs when an nMOS transistor is under positive bias. These both effects degrade the transistor speed and system may fail due to timing violations. In this paper, an Adaptive Hold Logic (AHL) circuit is proposed to mitigate the performance degradation due to aging effects.

Keywords
Aging Effects, Aging Indicator, Bias Temperature Instability.

1. INTRODUCTION
CMOS reliability can be categorized into two unreliability effects as:-

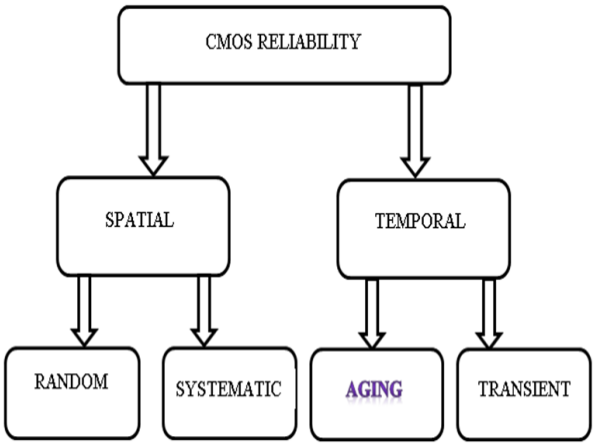

Fig. 1.1 CMOS Reliability

1.1 Aging Effects
Due to aggressive scaling of the device geometries and increasing electric fields, circuit aging has become an issue. Measurements on individual transistors were used to determine circuit design margins in order to guarantee reliability. Integrated-circuit aging phenomena observed in sub-90nm CMOS technologies are as follows [2]:-

1. Hot Carrier Injection (HCI).
2. Time-Dependent Dielectric Breakdown (TDDB).
3. Bias Temperature Instability (BTI).
4. Electro-migration (EM).

1.1.1. Hot Carrier Injection (HCI)
Hot carriers are particles that obtain a very high kinetic energy from being accelerated in a high electric field. These energetic carriers can be injected into `forbidden' region of the device such as the gate oxide, instead of following their intended trajectory. When injected into such a region they can get trapped or cause the generation of interface states. These defects in turn lead to shifts in the electrical characteristics of the transistor such as a shift of the V_{th}, the current factor β and the output conductance g_o. The degradation of integrated circuits due to Hot Carrier Injection (HCI) [2] comes into existence due to the continuous scaling of transistor dimensions without accompanying supply voltage reduction. The circuit operating voltage was dropped to reduce power consumption and graded drain junctions were introduced to solve reliability problems. Hence, HCI became less of an issue. HCI can still be a problem since supply voltage scaling is slowing down because of the non-scalability of the sub-threshold slope. HCI is primarily a problem in nMOS devices. Although pMOS devices are less sensitive to HCI, the effect can enhance other aging effects such as negative bias temperature instability (NBTI).

1.1.2. Time-Dependent Dielectric Break-down (TDDB)
The correct operation of a MOS transistor relies on the insulating properties of the dielectric layer below the gate electrode of the transistor. Each dielectric material has a maximum electric field in which it can sustain. When a larger electric field is applied, this leads to Hard Breakdown (HBD). HBD is an extremely local phenomenon, characterized by a loss of the gate oxide insulating properties and allowing a large gate current to flow. At lower electric fields, the insulator can wear-out after some time and finally break down completely. This is called Time-Dependent Dielectric Breakdown (TDDB) [2].

1.1.3. Bias Temperature Instability (BTI):-
Bias Temperature Instability (BTI) has gained a lot of attention due to its increasingly adverse impact in nano-meter CMOS technologies. It is a threshold voltage (V_{th}) shift after a bias voltage has been applied to a MOS gate at elevated temperature. It causes threshold voltage (V_{th}) increments to the MOS transistors. Threshold voltage V_{th} increment in a pMOS transistor that occurs under the negative gate stress is referred to as Negative Bias Temperature Instability (NBTI) and the one that occur in an nMOS transistor under positive gate stress is known as Positive Bias Temperature Instability (PBTI). The NBTI or PBTI impact can become more

significant depending on the dielectric type. For a MOS transistor, there are two BTI phases [10].

a. Stress phase.

b. Relaxation phase.

These two phases differ by the gate biasing (i.e. V_{DD} or – V_{DD}) of the MOS transistors.

1.1.4. Electro-migration (EM)

Electro-Migration (EM) is an aging effect taking place in interconnect wires, contacts and vias in an integrated circuit [2]. The effect causes material transport by gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and the diffusing metal atoms. EM is important in applications where high direct current densities are used.

These aging effects are caused due to scaling of transistors in VLSI chips. The device aging causes loss on circuit performance and lifetime which are the main factors in the reliability degradation of VLSI circuit. Thus, to reduce this aging effect on CMOS, an Adaptive Hold Logic (AHL) circuit is founded to be more efficient than other methods.

2. RELATED WORK

A traditional method to reduce the aging effects is overdesign which includes techniques like guard-banding ad gate oversizing. This approach can be area and power inefficient [8]. To avoid this problem, an NBTI- aware technology mapping technique was proposed in [7] which guarantee the performance of the circuit during its lifetime. Another technique was an NBTI- aware sleep transistor in [3] which improve the lifetime stability of the power gated circuits under considerations. A joint logic restructuring and pin reordering method in [6] is based on detecting functional symmetries and transistor stacking effects. This approach is an NBTI optimization method that considered path sensitization. Dynamic voltage scaling and bogy-biasing techniques were proposed in [4] and [5] to reduce power or extend circuit life. These techniques require circuit modification or do not provide optimization of specific circuits.

Every gate in any VLSI circuit has its own delay which reduces the performance of the chip. Traditional circuits use critical path delay as the overall circuit clock cycle in order to perform correctly. However, in many worst-case designs, the probability that the critical path delay is activated is low. In such cases, the strategy of minimizing the worst-case conditions may lead to inefficient designs. For noncritical path, using the critical path delay as the overall cycle period will result in significant timing waste. Hence, the variable latency design was proposed to reduce the timing waste of traditional circuits. The variable latency design divides the circuit into two parts.

a. Shorter path.

b. Longer path.

For a given timing constraint T, a path is a long path if the delay of the path is longer than or equal to T otherwise, a path is a short path. Also, a gate is a critical gate if the gate is in a long path. The basic concept of variable latency design is to execute a shorter path using the shorter cycle and longer path using two cycles. Since most paths execute in a cycle period that is much smaller than the critical path delay, the variable latency design has smaller average latency.

3. PROPOSED WORK

A novel architecture of an Adaptive Hold Logic (AHL) circuit is proposed which will reduce the aging effects. The Adaptive Hold Logic (AHL) circuit can decide whether the input patterns require one or two cycles and can adjust the judging criteria to ensure that there is minimum performance degradation after considerable aging occurs.

The Adaptive Hold Logic (AHL) circuit is as shown in fig. 3.1. Assume the AHL circuit has a m bit input. The Adaptive Hold Logic (AHL) circuit consists of the following blocks.

a. Judging Blocks

b. D Flip-Flop

c. One Multiplexer

d. Aging Indicator

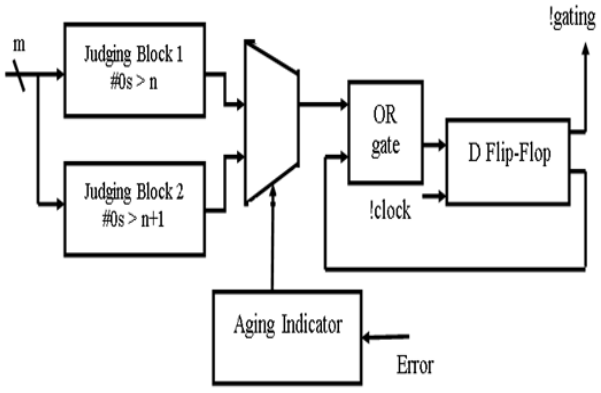

Fig 3.1. Proposed design of Adaptive Hold Logic (AHL) circuit

3.1. Aging Indicator

The Aging Indicator indicates that whether the circuit has suffered significant performance degradation due to aging effects. The aging effect is not significant in the beginning, so the aging indicator produces output as 0. The Aging Indicator is implemented in a counter that counts the number of errors over a certain amount of operations. These operations may be multiplication or addition. It resets to zero at the end of those operations.

3.2. Judging Blocks

There are two judging blocks in Adaptive Hold Logic (AHL) circuits. The 1st judging block will generate an output as 1 if the number of zeros in the input sequence is larger than n. If the number of zeros in the input sequence is larger than n+1 then the output of the 2nd judging block is 1. The value of n is defined by the user.

The operation of Adaptive Hold Logic (AHL) [1] circuit are as follows: when an input sequence is given, both the judging blocks will decide whether the sequence requires one cycle or two cycle to complete their operation and pass both results to the multiplexer. The multiplexer selects one of either result based on the output of the Aging Indicator. The result of the multiplexer and the output signal to the D flip-flop is ORed. This output of the OR operation is used to determine as the input of the D flip-flop. When the input sequence requires one cycle, the output of the multiplexer is 1. The !(gating) signal will become 1 and the input flip-flops will latch new data to perform operation in the next cycle. If the output of the

multiplexer is 0 which means the input sequence requires two cycles to complete it's operation. The OR gate will output 0 to the D flip-flop. Thus, to disabled the clock signal of the input flip-flops in the next cycle the !(gating) signal will become 0. Only one cycle of the input flip flop will be disabled because the D flip-flop will latch 1 in the next cycle.

4. METHODOLOGY

The proposed architecture of the Adaptive Hold Logic (AHL) circuit can be designed using Tanner EDA (Electronic Design and Automation) tool. The Schematic Capture (S-Edit) can be used for the process of drawing a schematic. It is a schematic entry tool that is used to document circuits that can be driven forward into layout of an Integrated Circuit. It provides the ability to perform SPICE simulations of the circuits using a simulation engine called T-SPICE. Waveform Editor (W-Edit) is used for waveform creation.

5. RESULTS

The circuit is designed in Tanner EDA 13.0 tool in 22 nm technology. Here it is assumed that the number of zeros in input A is 0 and in input B is 1 or greater than 1. Here both the judging blocks are AND gates. The aging indicator is also a AND gates.

Consider that there is no error in the operation. The circuit for that will look like as shown in the fig. 5.1.

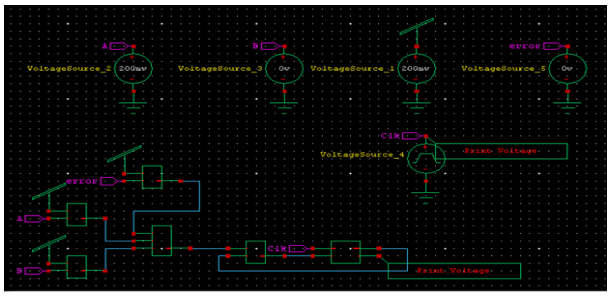

Fig. 5.1. AHL circuit without an error signal

The result of above circuit is shown in fig. 5.2. Here an error is shown at the output of the Gating signal. Thus this !(gating) signal will enable the clock signal of the input flip flop and next input will perform their operation in next clock signal.

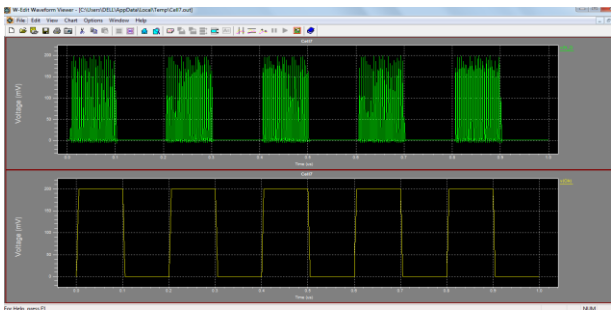

Fig. 5.2. Result of AHL circuit without error signal.

Consider that if any error occurs in execution of operation. The circuit of this condition will look like as shown in the fig. 5.3.

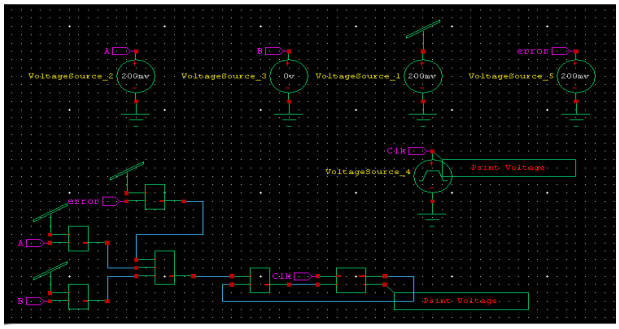

Fig 5.3. Circuit of AHL with an error signal

The result of above circuit is as shown in the fig. 5.4. Here the gating signal follows the clock signal. This !(gating) signal will disable the clock of the input flip flop and re-execution will occur of the same inputs.

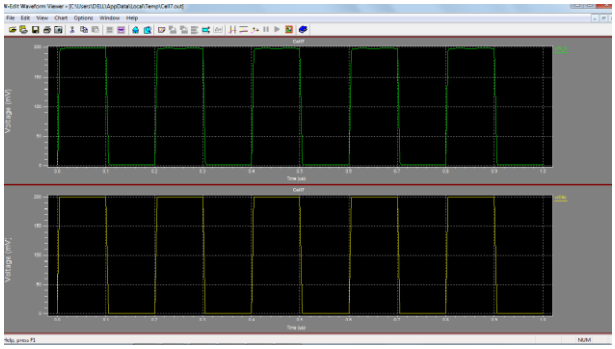

Fig. 5.4. Result of AHL with an error signal

6. CONCLUSION

An aging aware design of a novel Adaptive Hold Logic (AHL) circuit is proposed in this paper. The AHL circuit adjusts itself to mitigate performance degradation which is caused due to aging effects. This proposed work can be used in various VLSI applications to perform operations like addition, multiplication etc. The AHL circuit will produce output which will be both power and area efficient. The results will be in terms of Latency and Power consumption which will improve the circuit performance.

7. REFERENCES

[1] I. C. Lin, Y. H. Cho and Y. M. Yang, "Aging Aware Reliable Multiplier Design With Adaptive Hold Logic", IEEE Transaction on Very Large Scale Integration (VLSI) System, 2014.

[2] E. Maricau and G. Gielen. 2013 Analog IC Reliability in Nanometer CMOS. Springer Science Business Media, New York.

[3] Calimera, E. Macii and M. Poncino. 2012 "Design techniques for NBTI tolerant power-gating architecture", IEEE Transaction on Circuits System, vol. 59, no. 4, pp. 249–253.

[4] Y. Lee and T. Kim. 2011 "A fine-grained technique of NBTI-aware voltage scaling and body biasing for standard cell based designs", in Proceeding of Asia South Pacific Design Automation Conference, pp. 603–608.

[5] M. Basoglu, M. Orshansky and M. Erez. 2010 "NBTI-aware DVFS: A new approach to saving energy and increasing processor lifetime", in Proceeding of

ACM/IEEE International Symposium on Low Power Electronics and Design, 253–258.

[6] K. C. Wu and D. Marculescu. 2009 "Joint logic restructuring and pin reordering against NBTI-induced performance degradation", in Proceedings of Design, Automation and Test in Europe, 5–80.

[7] S. V. Kumar, C. H. Kim and S. S. Sapatnekar 2007 "NBTI-aware synthesis of digital circuits", in Proceedings of ACM/IEEE Design Automation Conference, 370–375.

[8] R. Vattikonda, W. Wang and Y. Cao. 2004 "Modelling and minimization of pMOS NBTI effect for robust nanometer design", in Proceedings of ACM/IEEE Design Automation Conference, 1047–1052.

[9] N. Weste and Kamaran "Principles of CMOS VLSI Design", Education Asia.

[10] S. Khan, H. Kukner, P. Raghavan and F.Catthoor, "BTI Impact on Logical Gates in Nano-scale CMOS Technology".