Simulation of 8T SRAM Array for Low Power Sensor Application

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ABSTRACT
The sensor network has become an important aspect in the day today life because of its wide range of application from medical field to the military application. The raw data from sensor node are of large quantity and hence it is necessary to store these data bits. In this paper, design of optimized SRAM array for low power applications is implemented. SRAM cell is designed using 8T. In this, transmission gate is used as access transistor to increase write-ability and decrease the power dissipation. The peripheral circuits are chosen to construct the SRAM array. Simulation are carried out using 180nm technology and result show that the reading and writing of data takes place correctly.

Keywords
SRAM, Sensor Network, Static Noise Margin.

1. INTRODUCTION
The development of wireless sensor network revolutionized our lifestyle. The sensor networks are used in various applications like military surveillance, environment monitoring, medical diagnosis, farming field. In the field of medical electronics wireless sensors are used for medical diagnosis like heart beat monitoring, blood sugar values etc.

The sensed raw data from the sensor network will be in large quantity [6]. Hence signals are processed to reduce the amount of data transmission. This requires large memory area to store the data bits. The computation intensive wireless sensor node with increased memory size significantly reduces the requirement of data transmission.

The trade off of SRAM array area for achieving low power consumption is a viable option for reducing the overall form factor of wireless sensor network. The increased energy efficiency of SRAM array would require smaller size battery.

In [6] and [9] 8T SRAM architecture was used to overcome the 6T SRAM cell hindrances. Using 8T SRAM they were able to decrease the power consumption and increase Write Ability (WA). In Differential Data Aware Power Supplied (D^2AP) 8T SRAM cell powering done through bit line pairs [7].

Half Select Condition Free Cross Point 8T (CR8T) [11] are developed using two additional access transistors. The other structure available are Read Decoupled 8T and 10T Cell [12]. In this, read operation has been decoupled to avoid half select problem by providing separate read/ write ports.

The proposed design is a further modification of CR8T structure which gives us better WM and also low power dissipation. The proposed CR8T is implemented using two Transmission Gates (TG).

Section 2 describes the design of SRAM array with the peripheral circuits such as sense amplifier, decoder and write driver. Section 3 gives simulation result and section 4 gives the conclusion.

2. DESIGN OF SRAM ARRAY
2.1 Design of CR8T SRAM Cell
Figure 1 shows the schematic of Half Select Free Cross Point (CR8T) SRAM Cell [6]. It comprises additional access transistors (M3, M4, M5, M6), cross coupled inverters (M1, M2, M7, M8). These access transistors controlled by the Horizontal Word Line (WLH) and Vertical Word Line (WLV). When signals are activated, the internal storage nodes are exposed to bit lines. The SRAM cells are selected only if both WLV and WLH are high and hence internal storage node gets exposure to the bit lines. For un-accessed SRAM cells either WLV or WLH is high and internal nodes are never exposed to bit line information.

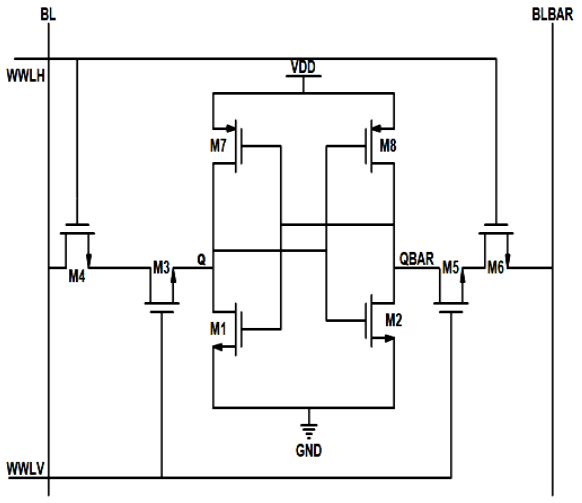

Fig 1: **8T SRAM Cell Free Cross Point (CR8T)**

Because of the existence of two access transistor, there will be degradation in the WM. Also in the read current, there is a considerable degradation. These are overcome by voltage optimization technique called as voltage optimization technique [6]. Figure 1 CR8T cell is designed based on the standard equation 1 and 2.

$$(W/L)_3/(W/L)_1 = 2[(V_{DD}-1.5V_{tn})/(V_{DD}-2V_{tn})^2] \quad (1)$$

$$(W/L)_5/(W/L)_3 = \mu_n/\mu_p[(V_{DD}-1.5V_{tp})/(V_{DD}+2V_{tp})^2] \quad (2)$$

Where $(W/L)_3/(W/L)_1$ is the Aspect Ratio (AR) of access transistor to the driver transistor and $(W/L)_5/(W/L)_3$ is the AR of load transistor to access transistor. V_{tn} is the threshold voltage of NMOS in equation 1 and V_{tp} threshold voltage of PMOS in equation 2. For the stable working, the cell is designed for kp = kn and $\mu_n=2\mu_p$.

2.2 Proposed CR8T SRAM Cell

The proposed CR8T SRAM cell is shown in Figure 2. In the, proposed CR8T design, two access transistors of CR8T are replaced by Transmission Gates (TG). As in CR8T the data will pass from bitline to cell only when access transistor is on. Here the data to NMOS and PMOS of TG should be complementary, then data passes from BL to the cell node Q, due to the TG the impedance has been reduced, the Write Ability (WA) of the cell has been enhanced.

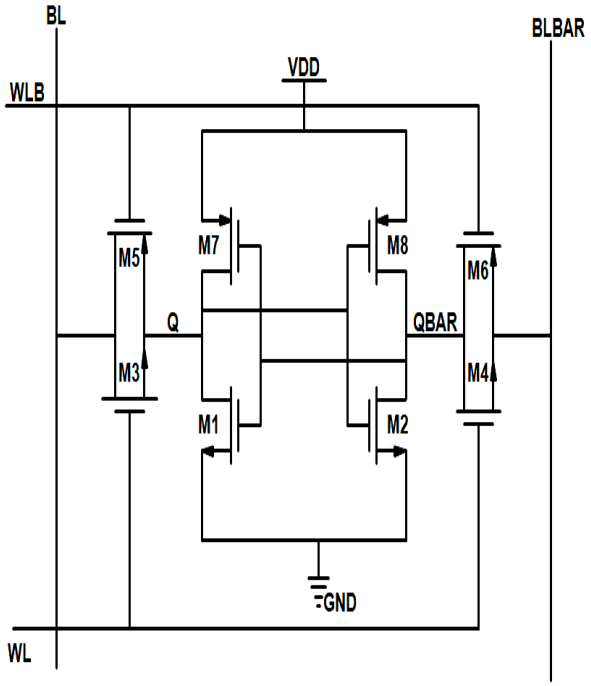

Fig 2: **Proposed CR8T SRAM Cell**

2.3 Sense Amplifier

Different type of sense amplifier are available [16]. Current Mode Latch Sense amplifier (CMVSA) is preferred over current mirror and voltage latch type sense amplifier. The hindrance in current mirror and voltage latch sense amplifier is shown in Table 1.

Sense Amplifier	Hindrance
Current Mirror Type	Rail to Rail simulation
Voltage Latch Type	Read 1 was hindered

In this work, CMVSA shown in Figure 3 is chosen based on high speed of operation and low power dissipation [16]. The CMVSA is used as sense amplifier in this paper. It requires a time of pre-charging then the PMOS (M8 and M9) are switched off and the sense enable signal is applied to NMOS (M1).

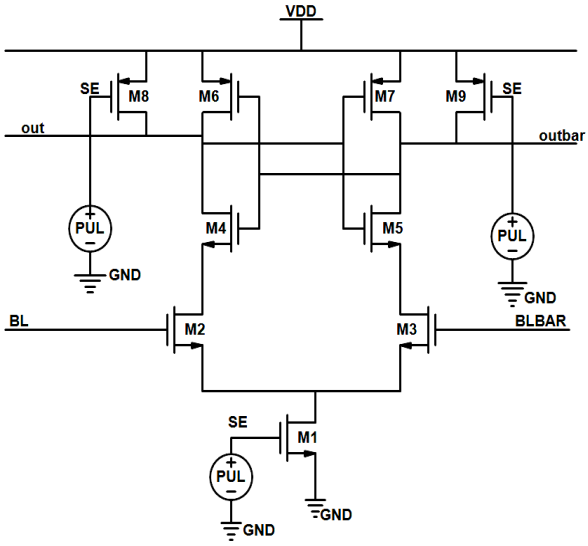

Fig 3: **Current Mode Voltage Latch Sense Amplifier (CMVSA) [16]**

2.4 Domino CMOS Wallace Tree Decoder

The domino CMOS Wallace tree Decoder is shown in the Figure 4. This decoder has two inputs given A and B which is inverted using two inverter circuits. Because of this the switching speed is superior and also the static power dissipation is the lower .

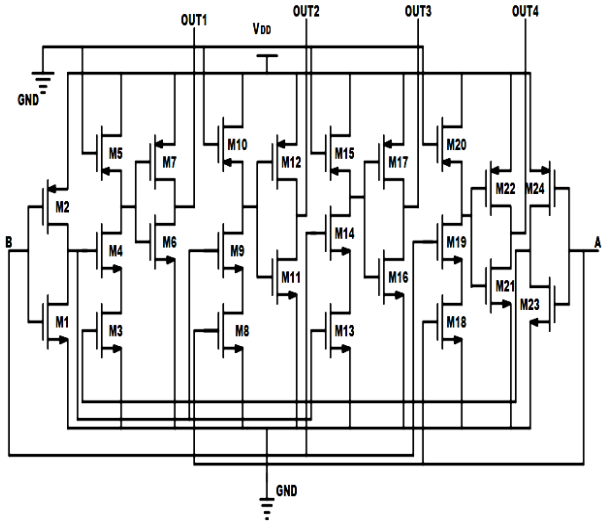

Fig 4: **Domino CMOS Wallace Tree Decoder**

2.5 Write Driver

The write driver circuit is shown in Figure 5 [5]. The basic function of any type of write driver used in the SRAM cell is to quickly discharge one of the bitlines from pre-charge level to below the write margin of the cell. The write driver is enabled by Write Enable (WE) signal and drives the bitline using full swing discharge from pre-charge level to ground. The input data is passed on to the cell if the WE signal is high else the data is not passed. The difference between Write drive for bit line bar and bit line is a single inverter before the input data .

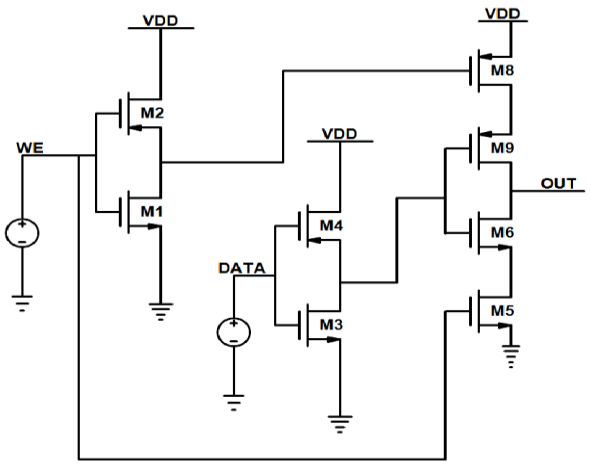

Figure 5: Write Driver Circuit Blbar

3. SIMULATION RESULT

3.1 Read Write Operation of CR8T

The write operation of CR8T as shown in Figure 6.The response shows that data is not written properly.

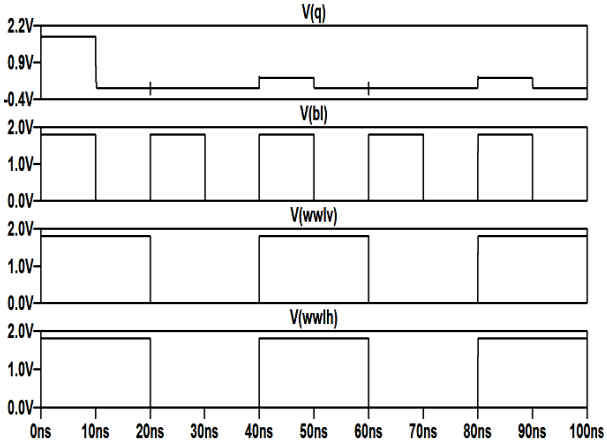

Fig 6: Write Operation of CR8T

Write operation in proposed CR8T, there is enhancement in the write-ability of the circuit shown in Figure 6. The problem that was faced in conventional 6T SRAM and CR8T has been rectified by use of transmission gates as access transistor in the circuit.

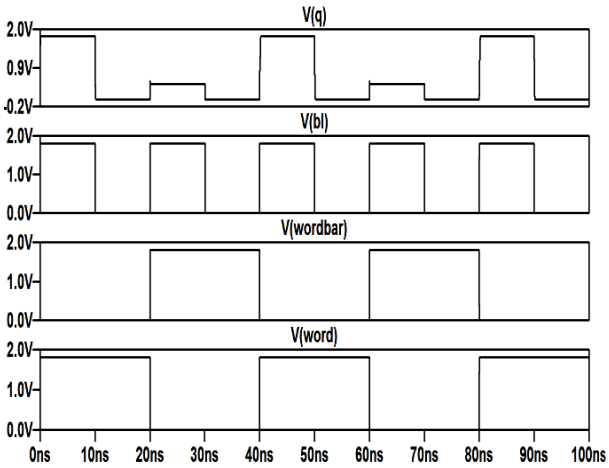

Fig 7: Write Operation of Proposed CR8T

3.2 Butterfly Diagram

The equal butterfly response of proposed CR8T SRAM Cell is shown in Figure 8. It is observed that low noise margin and high noise margin are equal. This is the required condition for the stable circuit.

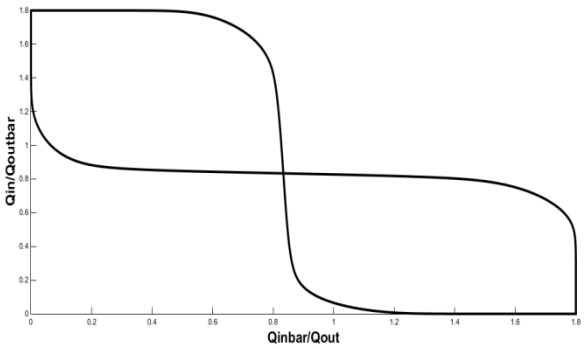

Fig 8: Butterfly Diagram of Proposed CR8T Structure

3.3 Simulation of Current Mode Voltage Sense Amplifier

The simulation of CMVSA is shown in Figure 9. The SA is enabled after 1.5µs and the data is read at the V_{out}.

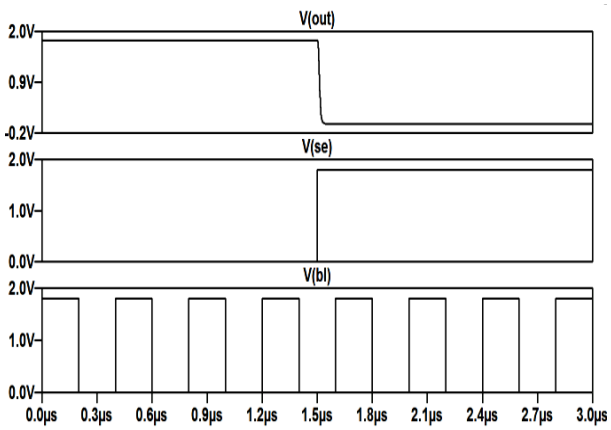

Fig 9: Simulation Result of CMVSA Sense Amplifier

3.4 Simulation of Domino Wallace Tree Decoder

The Table 1 shows the output of the decoder. The schematic output is shown in Fig 10.

Table 1: Output of Domino Wallace Tree Decoder

V(a)V(b)	V(q0)	V(q1)	V(q2)	V(q3)
00	1	0	0	0
01	0	1	0	0
10	0	0	1	0
11	0	0	0	1

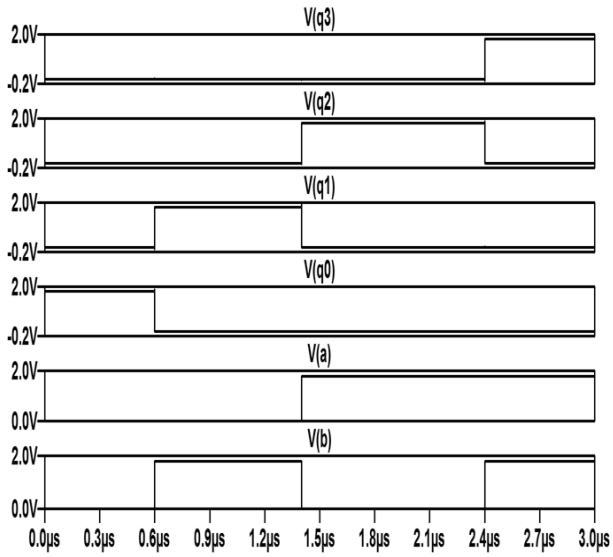

Fig 10: Simulation of Domino CMOS Wallace Tree Decoder

3.5 Simulation of Write Driver Connected to BLBAR

The data is passed on to the BLBAR only during the WE period, after this cycle it does not write data into the cell. The wave forms are as shown Figure 11.

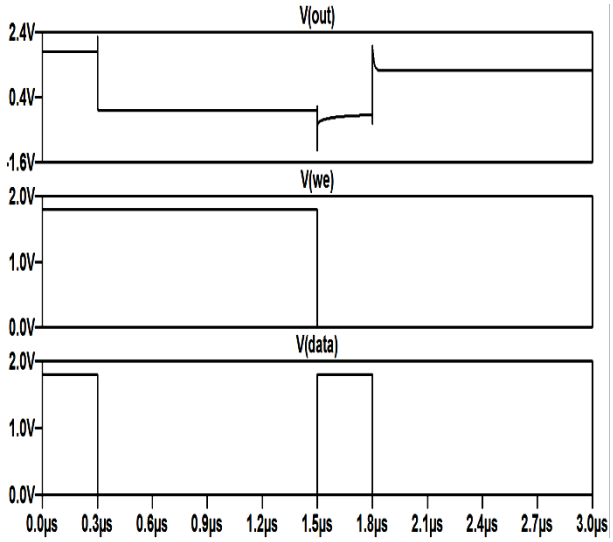

Fig 11: Output of Write Driver Connected To BLBAR

3.6 Result of 4x4 Proposed CR8T Structure

The block diagram of 4x4 proposed CR8T SRAM array is shown in Figure 12. The simulation of the schematic is shown in Figure 13. Data '1' is written into first cell of first row indicated by V (q) and data '0' is written into second cell of second row indicated by V (q5). This data is read at V (out1) and V (out2) when sense amplifier is enabled after 150µs

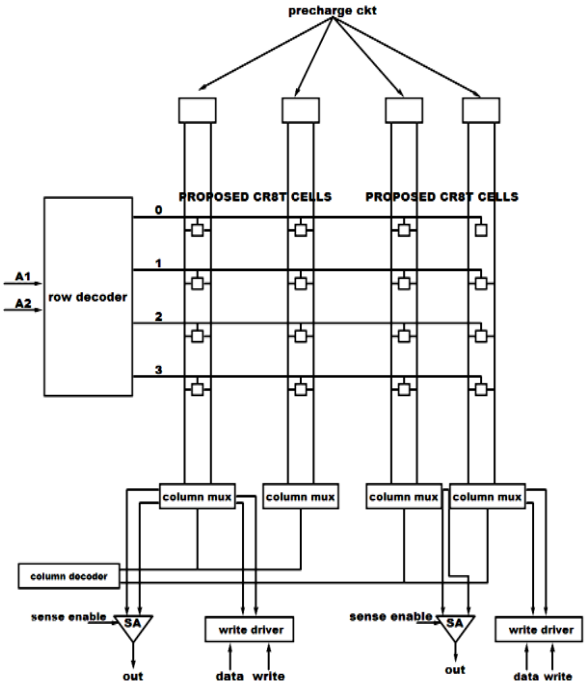

Fig 12: Block Diagram 4X4 Proposed CR8T Array

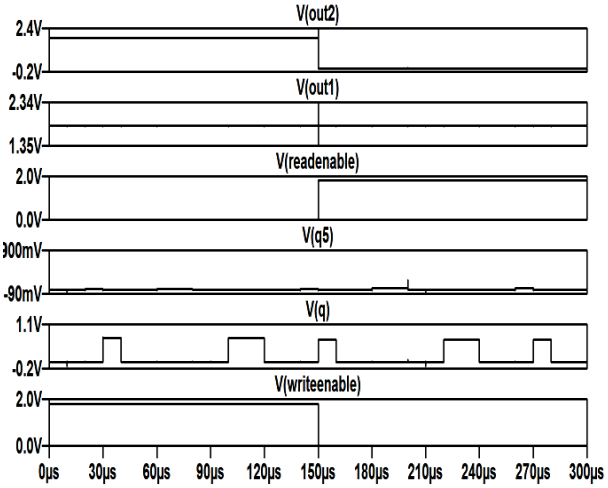

Fig 13: Output of Schematic SRAM 4X4 Array with Peripheral Circuits

3.7 Power Dissipation in Different SRAM Structures

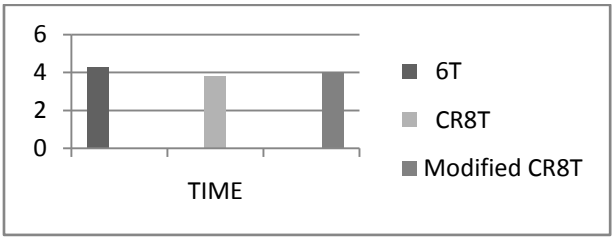

Fig 14: Power Dissipation of SRAM Cells

The power dissipation in different SRAM in mw is given in Figure 14. It is observed that CR8T consumes less power.

3.8 Comparison of Different Decoder Structure

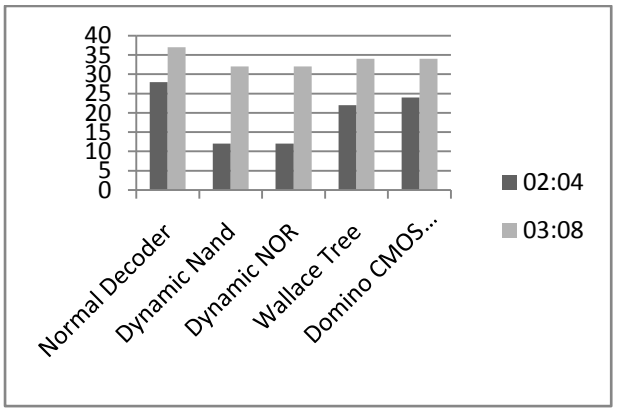

Fig 15:Number of Transistors in Different Decoder Structures

Figure 15 gives the number of transistors used in each type of decoder structure for 2:4 and 3:8. The dynamic decoder NAND and NOR are unstable at higher frequency. Wallace and Domino CMOS Wallace tree decoder are found to be more stable and consume less area for larger SRAM arrays.

4. CONCLUSION

Different 8T SRAM cells are analysed and CR8T is modified by replacing NMOS access transistors by transmission gates. It is observed that write ability was enhanced and power dissipation is reduced when compared to 6T SRAM cell. Different SA's are analysed and it is found that CMVSA suits to our designed CR8T SRAM cell. Analysis on different decoder architectures are made and it is found that Domino CMOS Wallace tree decoder suits for low power and high speed application. Using these circuits, SRAM array of 4x4 is created schematically. It is found that all these peripheral circuits are working correctly according to the requirement. This array is tested for reading and writing data.

5. AKNOWLEDGEMENT

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6. REFERENCES

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