

# Analysis, Design and Optimization of On-Chip Inductors on Sapphire for Gan based Rfics

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## ABSTRACT

The on chip spiral inductors are one of the key components in the development of the RFIC's as they determine the performance of the circuits such as VCO, LNA, mixers etc. In this paper, the design of an inductor for GaN based RFICs operating in C-band is presented. Sapphire ( $Al_2O_3$ ), which is a common substrate for GaN, is used as substrate and silicon nitride ( $Si_3N_4$ ), which is a common passivation layer in GaN technology, is used as insulator layer between the metal layers. While the use of  $Al_2O_3$  alleviates the problem of substrate losses that are common in Si substrate, use of  $Si_3N_4$  increases the inter-metal layer capacitance. IE3D EM simulation tool was used for the design and optimization of the spiral inductors. An inductor of 5 nH operating at 5 GHz has been designed and optimized to achieve high quality factor (Q) in low foot print. Finally a parallel LC resonant tank circuit was designed to resonate at 5 GHz to demonstrate the operation of the designed inductor.

## Keywords

RFICs, on chip inductor, quality factor, foot print, self-resonance frequency.

## 1. INTRODUCTION

With the emergence of communication technologies and particularly for the portable, small size, low-cost, more functionality, low power consumption consumer applications, spiral inductors on silicon have established itself as the standard passive components in high-frequency silicon (Si) technologies [1]. Besides, on chip inductors are also used in RFICs which are made on various other materials such as GaAs and GaN [1]. Recently GaN has attracted the research interest in the field of high power and high frequency due to its attractive material properties. However, the technological parameters for the design of inductor are different. In this paper, design of on chip inductors for GaN RFICs is discussed. While the use of  $Al_2O_3$  alleviates the problem of substrate losses that are common in Si substrate, use of  $Si_3N_4$  increases the inter-metal layer capacitance due to its high dielectric constant. An inductor of 5 nH operating at 5 GHz has been designed and optimized to achieve high quality factor in as less floor area as possible.

In section 2 the fundamental definitions of the performance parameters (Q factor,  $f_{sr}$ , inductance (L)), loss mechanisms, and physical model of an inductor are described. The effects of various design parameters such as width of the spiral turns (w), separation between the turns (s), number of turns (N), area of an inductor layout (a) and thickness of the metal ( $t_m$ ) and insulator ( $t_{ox}$ ) on the performance parameters are demonstrated through simulations. In section 3 design of inductor for a given specifications and the use of same in the parallel LC resonant tank circuit is described. Finally, conclusions are drawn in section 4.

## 2. DESIGN AND PERFORMANCE PARAMETERS

### 2.1 Performance Parameters

Three important parameters are used to qualify the performance of an inductor for certain applications. These include quality factor, inductance and self-resonant frequency.

#### 2.1.1 Quality factor (Q)

One of the most frequently mentioned figure of merit of the on chip inductors is Q factor, defines the efficiency of an inductor to store the magnetic energy in spite of parasitic effects. This leads to the following definition of the Q factor [2]

$$Q = 2 * \pi * \left( \frac{\text{Peak Magnetic Energy} - \text{Peak Electric energy}}{\text{Energy Loss in One Oscillation Cycle}} \right) \quad (1).$$

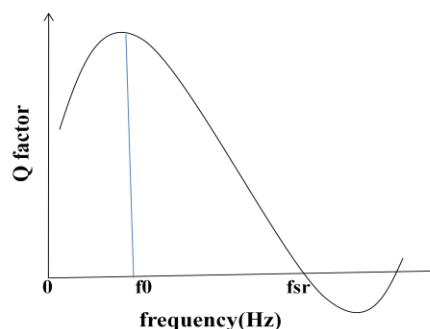


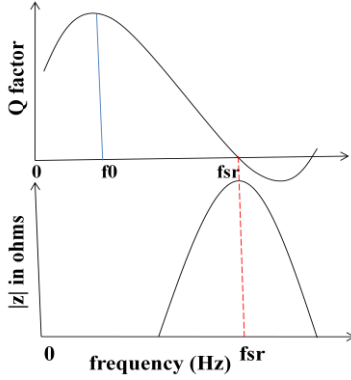
Figure 1: Plot of variation of Q factor of an inductor as a function of frequency

An inductor is at self resonance when the peak magnetic and electric energies are equal [3], therefore the Q vanishes to zero at the self-resonant frequency ( $f_{sr}$ ) as shown in the figure 1.

#### 2.1.2 Inductance (L)

Another important parameter to measure the performance of an inductor is its energy storing capacity measured in terms of the inductance. It may be defined in terms of energy, which an inductor can store in the magnetic field for a given current flowing through the inductor. In this paper I have considered one of the new approximate expressions as given in the equation (2) to calculate the inductances of different inductor geometries developed by Mohan et al., as it includes the design specifications [4]. This equation further simplifies the calculations based on the current sheet concept and serves as an adequate approximation for the geometries where the conductor thickness is dwarfed by the length and width and the equation is given by

$$L_{mon} = \beta d_{out}^{\alpha 1} w^{\alpha 2} d_{avg}^{\alpha 3} N^{\alpha 4} s^{\alpha 5} \quad (2)$$



**Figure 2: Plot of Q factor (top) and |Z| (bottom) as a function of frequency**

Where  $\beta$  is a layout dependent constant,  $d_{out}$  = outer diameter,  $w$  = width of the spiral turn,  $d_{avg} = (d_{out} + d_{in})/2$  is the average diameter of the spiral layout,  $d_{in}$  = inner diameter,  $N$  = number of spiral turns,  $s$  = spacing between the spiral turns,  $\alpha_i$  where  $i = 1$  to 5 are the coefficients and are layout dependent. For square layout  $\alpha_1 = -1.21$ ,  $\alpha_2 = -0.147$ ,  $\alpha_3 = 2.40$ ,  $\alpha_4 = 1.78$ ,  $\alpha_5 = -0.03$  and  $\beta = 1.62 \times 10^{-3}$ .

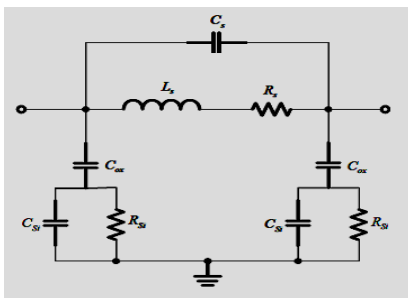
### 2.1.3 Self-resonant frequency ( $f_{sr}$ )

One more critical parameter used to validate the quality of an inductor is its self-resonant frequency, at which the reactance of inductor and the parasitic capacitances are equal in value and are thus caused to resonate [2].  $f_{sr}$  can be calculated from the peak value of impedance ( $|Z|$ ) or by locating the frequency where Q factor goes to zero as shown in the figure 2. From the graph of  $|Z|$  versus frequency the  $f_{sr}$  can be calculated using the following equation [4]

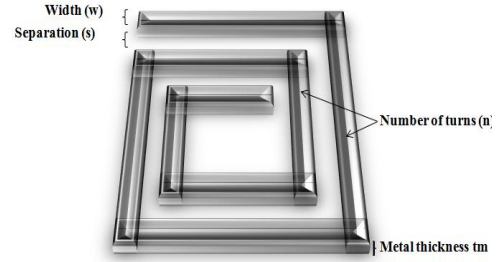
$$f_{sr} = \frac{1}{2 \cdot \pi \cdot \sqrt{LC}} \quad (3)$$

## 2.2 Physical Model and Loss Mechanisms

Physical model of an inductor with the parasitic resistances and capacitances is shown in the figure 3 [5]. In this model the series branch consists of  $L_s$ ,  $R_s$ , and  $C_s$  [3].  $L_s$  represents the series inductance of the spiral inductor that can be computed by using an approximate equation given in equation (3).  $R_s$  represents the series resistance of the metal. This resistance is used to symbolize the losses due to the skin effect in the spiral interconnects and the induced eddy currents, and is given by the equation (4) [5].  $C_s$  represents the series feed forward capacitance due to the overlap between the spirals and center tap overpass. This capacitance is very important as it constitutes relatively large potential difference between the spirals and center tap overpass and is given by the equation (5).  $C_{ox}$ ,  $C_{si}$  and  $R_{si}$  represents the parasitics in



**Figure 3: Physical model of an Inductor**



**Figure 4: Schematic of an on chip inductor with design parameters**

the shunt branch as given by the equations (6), (7) and (8) respectively.  $C_{ox}$  represents the oxide capacitance between the spirals and substrate.  $C_{si}$  and  $R_{si}$  represent the substrate capacitance and resistance respectively. The ohmic loss in  $R_{si}$  signifies the energy dissipation in the substrate.

$$R_s = \frac{\rho \cdot l}{w \cdot \delta \cdot \left(1 - e^{-\frac{t_m}{\delta}}\right)} \quad (4)$$

$$C_s = n \cdot w^2 \cdot \frac{\epsilon_{ox}}{t_{oxM1-M2}} \quad (5)$$

$$C_{ox} = \frac{1}{2} \cdot l \cdot w \cdot \frac{\epsilon_{ox}}{t_{ox}} \quad (6)$$

$$C_{si} = \frac{1}{2} \cdot l \cdot w \cdot C_{sub} \quad (7)$$

$$R_{si} = \frac{2}{l \cdot w \cdot G_{sub}} \quad (8)$$

Where  $\rho$  = metal resistivity,  $l$  = overall length of the spirals,  $w$  = width of the spiral track,  $\delta$  = skin depth,  $t_m$  = metal thickness,  $t_{oxM1-M2}$  = oxide thickness between the spirals and center tap,  $n$  = number of overlaps between the spirals and center tap =  $N-1$  ( $N$ =number of spiral turns),  $t_{ox}$  = oxide thickness between the spirals and substrate,  $C_{sub}$  = substrate capacitance per unit area,  $G_{sub}$  = substrate conductance per unit area.

It may be noted that, the values of  $R_{si}$  is extremely large for insulating substrates, such as sapphire that has been used in this work, and may be considered open circuit for all practical purposes.

## 2.3 Influence of Design Parameters

Figure 4 shows the spiral inductor layout with the design parameters. These parameters are classified as geometrical and technological parameters. The technological parameters include material parameters of the substrate ( $Al_2O_3$ ) and inter metal layer insulator ( $Si_3N_4$ ) as well as its thicknesses and are not under the control of an inductor designer. Hence in this section I am concentrating only on the effects of geometrical parameters such as conductor width ( $w$ ), separation between the spiral turns ( $s$ ), number of turns ( $N$ ), and area ( $a$ ) on the performance parameters. However, for the sake of understanding, the effect of metal thickness ( $t_m$ ) and the insulator thickness ( $t_{ox}$ ) on the performance parameters are also presented. These parameters will have the influence over the electrical properties and losses of a spiral inductor. The exact interaction between these parameters and the electrical properties is not exactly known [6]. But the qualitative relationship is understood and is discussed in this subsection.

Figure 5 shows the effect of width ( $w$ ) on the performance parameters of the spiral inductor. Increase in ' $w$ ' decreases the resistance ( $R_s$ ), resulting in the improvement of Q factor. But the metal to substrate capacitance ( $C_{ox}$ ) also increases, resulting in the decrease of values of L and  $f_{sr}$ . Figure 6 shows the effect of separation ( $s$ ) between the turns on the performance parameters. For small values of  $s$ , signals can couple directly between the adjacent turns through metal-to-metal parasitic capacitance resulting in the decrease of the Q factor and  $f_{sr}$ . However, due to the increase in the value of mutual inductance, the overall inductance of the structure increases.

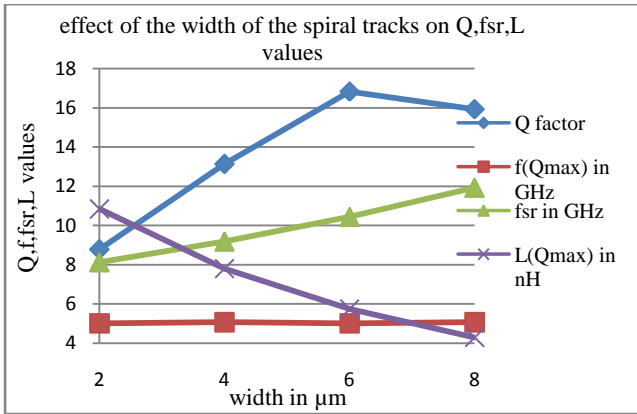


Figure 5: Effect of width ( $w$ ) of the spiral turns on the performance parameters

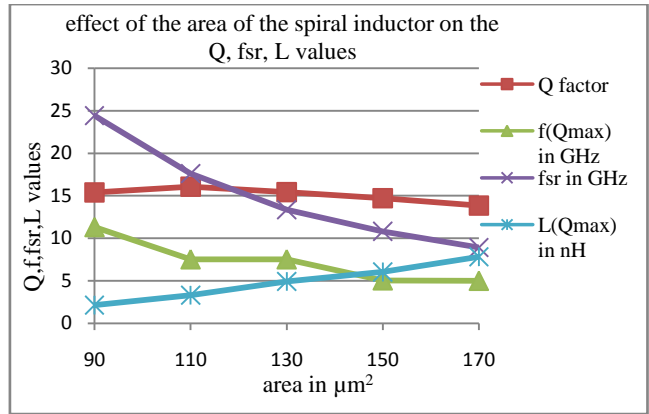


Figure 8: Effect of area ( $a$ ) on the performance parameters

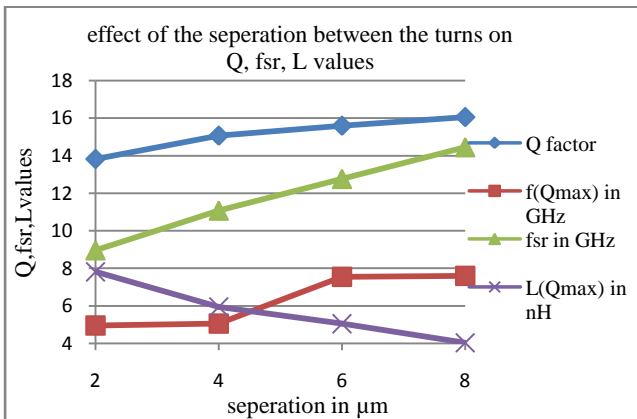


Figure 6: Effect of separation ( $s$ ) between the spirals turns on the performance parameters

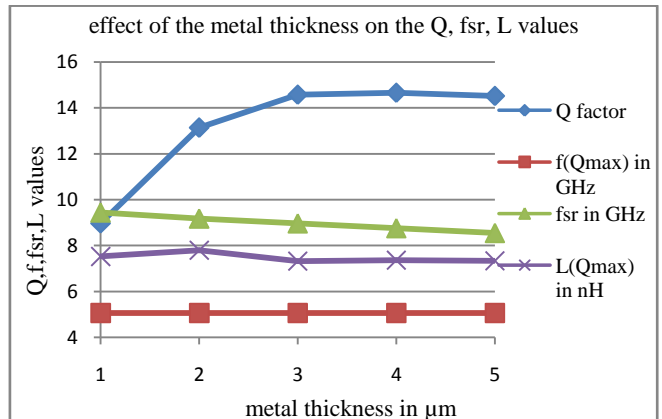


Figure 9: Effect of metal thickness ( $t_m$ ) on the performance parameters

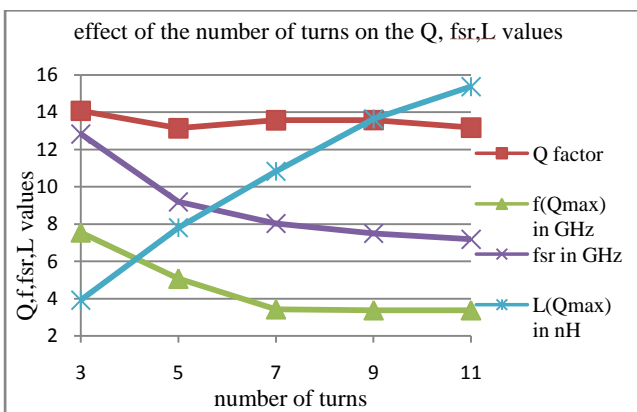


Figure 7: Effect of number of turns ( $n$ ) on the performance parameters

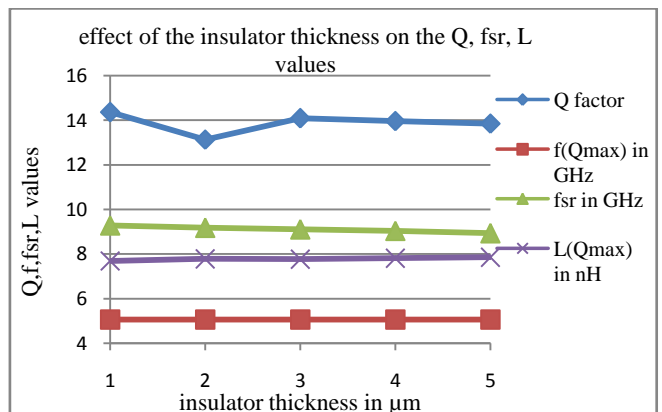


Figure 10: Effect of insulator thickness ( $t_{ox}$ ) between the spiral turns and the substrate on the performance parameters.

and substrate also increases and hence the Q factor and  $f_{sr}$  values decrease. Figure 9 shows the effect of metal thickness ( $t_m$ ) on the performance parameters. As the thickness of the metal is increased, the resistance ( $R_s$ ) decreases and the Q factor improve, but the metal-to-metal capacitance also increases. Therefore the resonant frequency ( $f_{sr}$ ) of an inductor reduces. Figure 10 shows the effect of insulator thickness ( $t_{ox}$ ) on the performance parameters. This represents the vertical distance between the metal spiral tracks and the conductive substrate, associated with the integrated inductor losses. The magnetic field generated by the conductor induces the eddy currents in substrate and the magnetic energy is lost as the heat. Hence this distance is often set to be large enough to avoid the significant losses in substrates.

### 3. DESIGN AND OPTIMIZATION

In this section I have described the design and optimization of the planar spiral inductors on  $Al_2O_3$  with  $Si_3N_4$  as the insulating material. The inductors in this paper have been designed using the single layer planar spirals. I took up a problem to optimize the design of an inductor with  $L = 5$  nH at 5 GHz and  $f_{sr}$  in the range of 10-14 GHz in an optimum area for the C band applications. The design constraints and technological parameters are given in the table 1 and 2 respectively.

The specifications mentioned in the table 1 can be achieved by the different combinations of the geometrical and technological parameters for a given area. But for a given technology, material and process parameters are fixed and only layout parameters are available for variation. Therefore based on some limits in the fabrication technology, I have selected the technological parameters as mentioned in the table 2 and the same were used throughout the work. Since several combinations of geometrical parameters will result in the constraints mentioned in the table 1, I have tried to optimize the design of an inductor by providing bounds to the geometrical parameters as follows

$$1\mu m (w_{min}) < w < 6\mu m (w_{max})$$

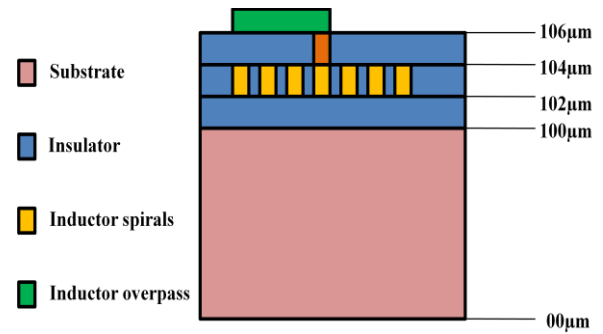
$$1\mu m (s_{min}) < s < 3\mu m (s_{max})$$

**Table 1: Design specifications for inductor design**

Parameters	Values
Inductance	5nH
Operating frequency	5GHz
Resonant frequency	10-14GHz
Area	140-160 $\mu m^2$

**Table 2: Technological parameters**

Parameters	Values
Substrate	Sapphire
Substrate di-electric constant	9( $Al_2O_3$ )
Insulator thickness	2 $\mu m$
Insulator di-electric constant	7.5( $Si_3N_4$ )
Metal conductivity	$4.7 \cdot 10^7$ S/m
Metal thickness	2 $\mu m$
Geometry of an Inductor	Square



**Figure 11: Cross section of on chip inductor design**

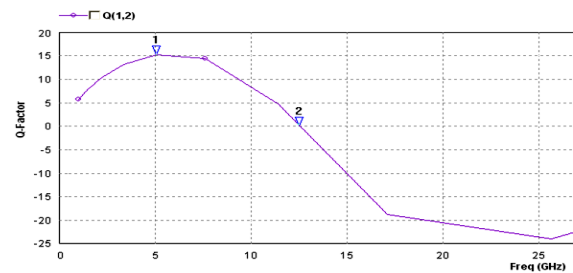
$$60\mu m d_{in (min)} < d_{in} < 80\mu m d_{in (max)}$$

$$140\mu m d_{out (min)} < d_{out} < 160\mu m d_{out (max)}$$

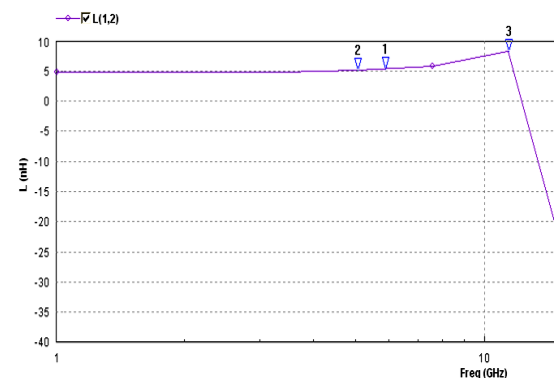
$d_{in}$  and  $d_{out}$  represent the inner and outer diameters of the square spiral layout. The lower limitations are mainly imposed by the lithography capabilities of the foundry. For each different combinations of these values the N was calculated using the equation

$$d_{out} = d_{in} + 2wN + 2s(N-1) \quad (9)$$

I have calculated the inductance values for different combinations of  $d_{out}$ ,  $d_{in}$ ,  $w$ ,  $s$ , and  $N$  using the equation (2). Table 3 shows the calculated inductance values for different combinations of the  $d_{in}$ ,  $w$ ,  $s$ , and  $N$  values with  $d_{out} = 140\mu m$ .



**Figure 12(a): Graph of simulated Q factor values as a function of frequency for the inductor designed in 140 $\mu m^2$  area**



**Figure 12(b): Graph of simulated inductance values as a function of frequency for the inductor designed in 140 $\mu m^2$  area**

**Table 3: The calculated values of L for different combinations of  $d_{in}$ ,  $w$ ,  $s$  and  $N$  for  $d_{out} = 140\mu m$**

Width $\mu m$	Separation $\mu m$	For $D_{in}=80\mu m$		For $D_{in}=70\mu m$		For $D_{in}=60\mu m$	
		Number of turns	Inductance nH	Number of turns	Inductance nH	Number of turns	Inductance nH
1	1	15.5	43.98	18	51.594	20.5	58.236
2		10.33	19.534	12	22.931	13.66	25.857
3		7.75	10.995	9	12.898	10.25	14.559
4		6.2	7.037	7.2	8.255	8.2	9.318
5		5.16	4.874	6	5.733	6.833	6.471
6		4.42	3.576	5.142	4.21	5.875	4.783
1	2	10.33	19.534	12	22.931	13.66	25.857
2		7.75	10.995	9	12.898	10.25	14.559
3		6.2	7.037	7.2	8.255	8.2	9.318
4		5.16	4.874	6	5.733	6.833	6.471
5		4.42	3.576	5.142	4.21	5.875	4.783
6		3.875	2.749	4.5	3.225	5.125	3.64
1	3	7.75	10.995	9	12.898	10.25	14.559
2		6.2	7.037	7.2	8.255	8.2	9.318
3		5.16	4.874	6	5.733	6.833	6.471
4		4.42	3.576	5.142	4.21	5.875	4.783
5		3.875	2.749	4.5	3.225	5.125	3.64
6		3.444	2.171	4	2.548	4.5	2.806

To design an inductor with the inductance of 5 nH, the possible combinations of geometrical parameters were then selected from the table 3. Since there are no combinations corresponding to exact 5 nH, nearest value i.e., 4.87 nH from the table 3 was considered. It can be observed from the table 3 that there are three combinations of geometrical parameters corresponding to the 4.87 nH. One of these geometrical parameter values were then adjusted by slightly varying their values, such that the inductance value was 5 nH. The inductor was designed using IE3D EM simulator and the inductance, Q factor values were simulated.

The optimized values of geometrical parameters were  $w = 5.4 \mu m$ ,  $s = 1.5 \mu m$ ,  $N = 6$ ,  $d_{out} = 140 \mu m$  and  $d_{in} = 80 \mu m$ . The

**Table 4: Performance parameter values with and without insulator between an inductor and substrate**

With insulator			Without insulator		
Q factor	Inductance in nH	$f_{qr}$ in GHz	Q factor	Inductance in nH	$f_{qr}$ in GHz
15.2174	5.08062	12.5147	15.32	5.096	12.71

inductance value calculated using the equation (2) for these values was 4.8518 nH. But the simulated inductance value was 5.0806 nH with  $Al_2O_3$  as the substrate. So there was an error of 4.5% between the calculated and simulated inductance values. The simulated Q factor value for these geometrical parameter values was 15.271. Figure 11 shows the schematic of an inductor design with an insulating layer between the inductor and substrate. Figure 12 shows the frequency dependence of Q factor and inductance plots for the designed inductor. Next I have placed the inductor directly on the substrate, instead of using an insulator to isolate an inductor from the substrate. This is possible on sapphire substrate as it is insulating. Table 4 compares between the performance parameter values of an inductor with and without an insulating layer.

### 3.1 Design Of Parallel LC Resonant Circuit

A parallel LC resonant circuit with center frequency of 5 GHz was designed to demonstrate the use of the designed inductor. Such a LC resonant circuit can be used for WLAN applications. To design the LC resonant tank circuit, I have considered the inductor designed in  $140\mu m^2$  area with  $Al_2O_3$  as the substrate. The tuning capacitance C required to design the LC resonant tank circuit was calculated using the equation

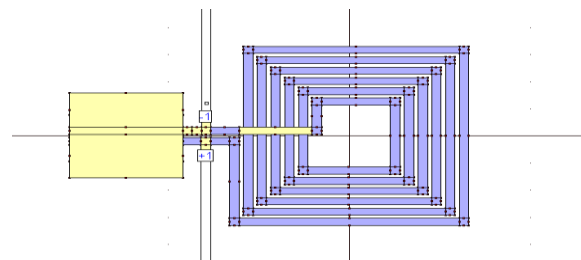
$$f_0 = \frac{1}{2\pi\sqrt{LC}} \text{ or } \omega_0^2 = \frac{1}{LC} \quad (10)$$

After substituting the center frequency as 5GHz and inductance value as 5nH in equation (10), I have got the tuning capacitance value as 0.2025pF. This capacitor with the capacitance of 0.2025pF for the design of LC resonant tank circuit was designed as the parallel plate capacitor with the  $Si_3N_4$  as the dielectric between the two plates and separated by the distance d, using the equation

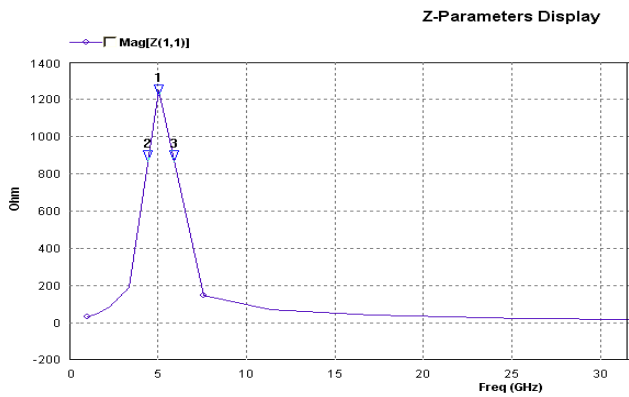
$$C = \frac{(\epsilon_0)(\epsilon_r)(A)}{d} \quad (11)$$

Substituting  $\epsilon_0 = 8.854 \times 10^{-12}$  permittivity of the free space,  $\epsilon_r = 7.5$  di-electric constant of the dielectric ( $Si_3N_4$ ) used between the parallel plates,  $d = 2 \mu m$  distance between the parallel plates in equation (11), I have got the Area  $A = 6098.73 \mu m^2$ , which is the area of each of the two parallel plates to design the capacitor. The parallel plate capacitor was then designed using the calculated specifications and LC resonant tank circuit was designed on the  $Al_2O_3$ . Figure 13 shows the 2D view of the designed LC resonant tank circuit. Figure 14 plots the frequency behavior of the tank impedance for 5GHz LC resonant tank circuit.

Q factor for the resonant circuit can be calculated as the ratio



**Figure 13: 2D view of the designed LC parallel resonant tank circuit**



**Figure 14: Graph of simulated impedance value of the LC resonant circuit**

of resonant frequency at which the tank impedance is maximum to the bandwidth and  $Q_{\text{tank}}$  is given by

$$Q_{\text{tank}} = \frac{f_0}{\text{BW}} \quad (12)$$

The calculated quality factor of the LC tank circuit is 3.3369.

#### 4. CONCLUSION

As the need for high power RFIC's becomes increasingly important in wireless communication, GaN based RFIC's have been considered as one of the novel devices for the high power applications as they feature high speed, high power density and low noise. High performance passive devices on these materials/substrate play a major role in the overall performance of the RFICs. In this paper the method of designing the on chip spiral inductors on the sapphire as this is one of the common substrates for the GaN based RFIC's is proposed. Also, the effects of geometrical parameters on the performance parameters are discussed. The parasitic effects of an inductor were analyzed with the help of physical model. The layout of an inductor was designed and performance parameter values were simulated using IE3D software. An inductor of 5 nH operating at 5 GHz was designed and the dimension of the inductor was reduced to  $140 \times 140 \mu\text{m}^2$  with the  $Q_{\text{max}} = 15.2701$ . Then the designed inductor was validated by using the same in a parallel LC resonant circuit.

In this work planar spiral inductors are used for the inductor design with the tradeoff between the achievable maximum value of Q and area of an inductor layout. The inductors can also be designed using other structures available in literature such as horizontal shunt, vertical shunt and line width optimization to achieve the high Q factor with the desired inductance and stacked or miniature-3D structures to achieve the desired L value in a low foot print.

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