Design and Performance Evaluation of Reconfigurable Architecture of FIR Filter for signal processing Applications

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ABSTRACT
Finite impulse response (FIR) filters are tremendously used in signal processing applications like RADAR processing, noise cancellation, biomedical imaging, removing DC component in signal etc. Most of Digital signal processing algorithm such as FFT,FIR and IIR are now implemented on FPGA because it offers very attractive solutions than any other in terms area ,power and speed. Reconfigurable architecture used in this paper is Distributed arithmetic . Here DA based FIR filter implemented on vertex5 with device XC5VLX110T. DA based FIR filter proposes advancement in speed, performance and area.

General Terms
Distributed arithmetic is efficient algorithm used for FIR filter design.

Keywords
DA-distributed arithmetic, FPGA-field programmable gate array, RADAR –Radio direction and ranging.

1. INTRODUCTION
Reconfigurable architecture of digital FIR filters main intension is reducing complexity of filter, increasing speed performance, low power loss, higher flexibility .In this paper, proposed method is most convenient and well performed filter. FIR filter has infinite number of impulse responses and it has highly reconfigurable filter. DA based filter which consist of mainly shift register, look up table and Accumulator unit. Look up table are used to minimize the number of adder in design. Hence number of multiplier units replaced by simple adder circuit.

Basic time domain equation for FIR filter is given by

$$F[n]=\sum_{n=0}^{N-1} s[n]\times g[n]$$

Here F[n] is filter output , G[n] is filter coefficient and s[n] is filter input [1]

2. DISTRIBUTED ARITHMETIC EQUATION
DA equation is derived from basic filter equation,

$$F[n]=\sum_{n=0}^{N=0} s[n]\times g[n]=$$

$$s[0]g[0]+s[1]g[1]+.....+s[N-1]g[N-1]$$

$$s[n]=\sum_{a=0}^{A-1} s_a[n]\times 2^a \qquad s_a[n]\in[0,1]$$

By substituting s[n] into above equation, we get

Unsigned equation [1]

$$F=\sum_{n=0}^{N-1} g[n]\sum_{a=0}^{A-1} s[n]\times 2^a$$

For signed equation is given by

$$s[n]=-2^{A-1}\times s_{A-1}[n]+\sum_{a=0}^{A-2} s_a[n]\times 2^a$$

$$F[n]=-2^{A-1}\times\sum_{n=0}^{N-1} g[n]\times s_{A-1}[n]+$$

$$\sum_{a=0}^{A-2} 2^a\times\sum_{n=0}^{N-1} g[n]\times s_a[n]$$

3. EXAMPLE FOR DA
Consider a=1010 ,b=1011

$$F=1\times(1010)2^0+1\times(1010)2^1+0\times(1010)2^2+$$

$$1\times(1010)2^3=1101110$$

3.1 Working of DA
FIR filter implementation using DA method is simple to design and very efficient method and bit serial in nature . DA based FIR filter consist of mainly three components shift registers ,look up table, and accumulator unit. In DA costly MAC units are replaced with LUT .Shift Registers act as input buffer, LUT main functional block for addition operation. Accumulator unit mainly for shifted addition operation.

3.2 Shift register
Shift registers mainly used as input buffer to store shifted inputs. Mainly two type of shift registers are used first one is parallel in serial out(PISO) and serial in serial out shift register(SISO).

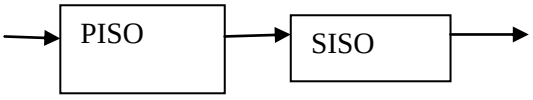


Fig 1:block model of shift register

Here input s[n] is fed to PISO shift register ,then it serial out given to SISO shift register .

3.3 Look Up Table

DA includes LUT for faster computation of multiplications . LUT which contains address and data . Filter coefficients are stored in LUT .It operates based on address lines. Each data is accessed from corresponding address value.

Table for content LUT is given in Table1

Table 1: Content of LUT

A2	A1	A0	DATA
0	0	0	0
0	0	1	A0
0	1	0	A1
0	1	1	A0+A1
1	0	0	A2
1	0	1	A2+A0
1	1	0	A2+A1
1	1	1	A2+A1+A0

3.4 Accumulator unit

This unit used for shifting and adding operations. Here right shift operation is performed before computing next addition operation. Left shift resembles 2's power multiplication. Operation of accumulator resembles repetitive adding and shifting. Accumulator unit which takes input from LUT and stores in accumulator before computing next operation. Accumulated value is added with coming input. This process occurs repeatedly until final output.

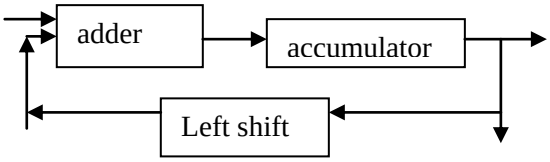


Fig 2: block model for Accumulator

3.5 Computational block for DA based FIR filter

Block model for FIR filter is given by

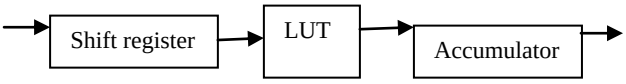


Fig 3: Block model for DA based FIR filter

Distributed arithmetic is bit serial in nature . Here multiplication is done by repetitive addition .DA which reduces area and power required for computation and it is faster one than other circuits.

3.6 Example for FIR design

Step 1: consider inputs as

S0=1100

S1=1010

S2=1000

S3=1001

Step 2: Consider coefficients of FIR filter

G0=0.0137

G1=0.4863

G2=0.4863

G3=0.0137

Step3: Input of shift register

$$S_0[0]S_1[0]S_2[0]S_3[0] = 0001$$
$$S_0[1]S_1[1]S_2[1]S_3[1] = 0100$$
$$S_0[2]S_1[2]S_2[2]S_3[2] = 1000$$
$$S_0[3]S_1[3]S_2[3]S_3[3] = 1111$$

Step4:Output of LUT

$$0001 \rightarrow out1 = 0\times 0.0137 + 0\times 0.0137 + 0\times 0.4863 + 1\times 0.0137 = 0.0137$$

$$0100 \rightarrow out2 = 0\times 0.0137 + 1\times 0.4863 + 0\times 0.4863 + 0\times 0.0137 = 0.4863$$

$$1000 \rightarrow out3 = 1\times 0.0137 + 0\times 0.4863 + 0\times 0.4863 + 0\times 0.0137 = 0.0137$$

$$1111 \rightarrow out4 = 1\times 0.0137 + 1\times 0.4863 + 1\times 0.4863 + 1\times 0.0137 = 1$$

Step 5: Accumulator unit operation

$$F0 = 0.0137\times 2^0 + 0 = 0.0137$$
$$F1 = 0.4863\times 2^1 + 0.0137 = 0.9863$$
$$F2 = 0.0137\times 2^2 + 0.9863 = 1.0411$$
$$F3 = 1\times 2^3 + 1.0411 = 9.0411$$

3.7 Simulation results

RTL schematic of DA based FIR filter

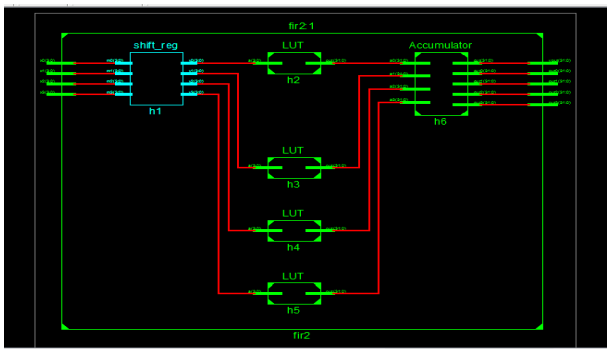
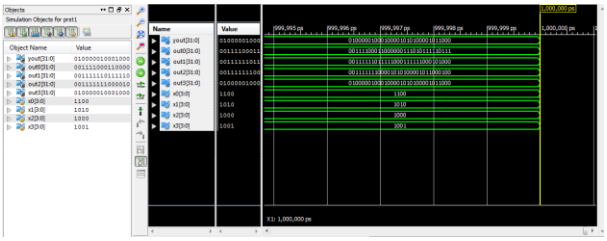


Fig 4:RTL schematic Simulation results



4. LITERATURE SURVEY

Several authors discussed about implementation of FIR on FPGA by using varies methods .

4.1 H.S.O migdadi and R.A Abd-alhameed et al, discussed about "FIR implementation on FPGA: Investigate the FIR order on SDA and PDA algorithms" ,IEEE publication

FPGA is on verge of revolutionizing digital signal processing .DA is most suitable then convultion approach, because in DA costly MAC units are replaced with LUT . LUT reduces power consumptions.

4.2 Sang yoon park ,pramod kumar meher et al ,discussed about "Efficient FPGA and ASIC Realisation of DA based reconfigurable FIR digital filter " IEEE transction on circuit.

DA approaches for high through put reconfigurable implementation FIR filter. Reconfigurable DA based implementation of FIR filter look up table required to be implemented in RAM.

4.3Yajun zhou , Pingzheng Shi et al,proposed about "Distributed arithmetic for FIR filter implementation on FPGA "*978-1-61284-774-0/11/$26.00 ©2011 IEEE*

Distributed arithmetic structure used to increase the resource useage while pipeline structure is used to increase system speed. Divided LUT reduces memory requirement.

5. CONCLUSION

In this paper , we designed and implemented efficient Reconfigurable architecture of FIR filter on vertex 5 with device XC5VLX110T . Coefficients are obtained from MATLAB, that are stored in LUT .Floating point coefficients are stored in IEEE 754 format. DA offers tremendous applications in DSP. Applying this architecture on field like biomedical ,signal processing ,digital communication gives highest performance results in terms speed ,power reduction and area.

6. ACKNOWLEDGEMENT

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7. REFERENCES

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