Delay and Power Reduction in RLC VLSI Interconnect Models

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ABSTRACT
This paper presents a comparative analysis of reduced segment; T and π RLC interconnect models. With down scaling of technology, the interconnect structures have became a predominant factor in determining the overall circuit performance. Controlling interconnect propagation delay is the fundamental parameter to high speed VLSI designs. In this work, model performance has been evaluated in terms of propagation delay and power dissipation. The design models have been implemented using Cadence Virtuoso Analog Design Suite at 180nm CMOS technology at high frequency range of 0.1GHz to 2GHz. A significant decrease of 38.424ps in propagation delay has been observed in π-Model as compared to the reduced segment interconnect model. 7.3253aW less power dissipation has been observed in reduced tree model when compared to RLC π-Model.

Keywords
Interconnects; T-model; π-model; delay; power dissipation; Very Large Scale Integration (VLSI).

1. INTRODUCTION
As per International Technology Roadmap for Semiconductor (ITRS-2013), VLSI interconnect is a thin film of conducting material that provides an electrical connection between two or more nodes of the circuits/system formed over the single silicon chip [1]. These interconnects occupy 40 to 44% of total chip area, which makes them too important to ignore as interconnects have strong impact on the overall circuit performance [1].

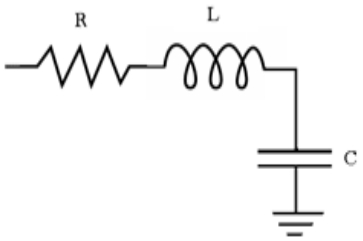

Fig 1: RLC Equivalent Interconnect Model

Figure 1 shows the basic RLC equivalent of interconnect. As the technology scales down, the length of the on-chip interconnect increases. This increase in the interconnect length leads to an equivalent increase in the resistance, capacitance and inductance.

Apoorva et al. in [2] proposed a mathematical expression for crosstalk noise in RLC interconnects model and observed less than 10% error is observed when results are compared to SPICE simulation under the effect of the input step response. The feature size has been decreased while there is an increase in the die size [3]. As the frequency of operation is increased, the power consumption is also increased [4]. Owing to continuous down scaling, interconnects come in close proximity to each other resulting in signal integrity issues like ground bound, ringing, distortion and crosstalk which may further results in circuit failure. D. Zhou et al. studied lumped RC model with the help of well know telegraph equations and analysed that wire length is approximately linear for the metal wire and decrease in the wire width below a particular point will drastically increase the propagation delay [5].

Power consumption sources in digital CMOS circuits are broadly categorised as: static, short-circuit and dynamic power dissipation [6]. The power consumed by any system is the mainly due to the current drawn from any power supply (V_{dd}).Static Power is due leakage sources in the circuit and is expressed as

$$P_{static}=I_{static}*V_{dd} \quad (1)$$

Dynamic power which is due to the switching current required to charge and discharge output load and is expressed as:

$$P_{dynamic}=\alpha*V_{dd}^2*f_{CLK}*C_L \quad (2)$$

Where, C_L is the load capacitance, V_{DD} is supply voltage, f_{CLK} is the clock frequency and α is the average activity factor or the switching factor whose value lies between 0 and 1.

The researchers in [7] studied RLC interconnect models aiming to reduce the delay. A.B Kahng et al. in [8] calculated the value of delay with the help of moment matching approach. While researchers in [9] ignored the initial line voltage. Feng Shi et. Al [10] in presented two improved delay models for coupled interconnects i.e. three wire model and five wire model and analyzed that these models have better accuracy than the previous work done. [11] was studied under the limitation of Bessel's function and thus derived the expression for the transient response of a distributed RLC interconnects model. R. Venkatesan et al. in [12] improved the previous work done by introducing the capacitive load to the distributed RLC interconnect to provide exact estimation of the interconnect time delay and crosstalk. O. Milter et al. in [13] proposed a design for noise effects by limiting the range of gate and main penalty for this work is increase in area and power dissipating. Chen et al. [14] modeled the strategy to find the time domain solution of the RLC interconnects with the help of Fourier series but the main drawback of this work were ignored fifth and higher order harmonics thus leading to less precision. Lin et al. limited themselves only to LC coupling effects resulting in crosstalk minimizing under delay constraints [16]. Under such conditions, the minimum delay path may cause unwanted race condition.

The rest of the paper is organized as follows: Section II describes the proposed interconnect models design.

Simulation results have been discussed in Section III and section IV concludes the paper.

2. PROPOSED INTEROCONNECT MODELS

In this section, the schematic of different RLC interconnect models namely reduced segment, T-model and π-model has been implemented in Cadence Virtuoso Analog Design Suite at 180nm CMOS technology. Sine wave as an input signal has been applied within the frequency range of 0.5GHz to 2GHz and amplitude of 1volts.

Table I. Parameter Values

Parameter	Value
Technology	180nm
Voltage	1V
Resistance(Ω/μm)	220
Capacitance(fF/μm)	470
Inductance(fH/μm)	360

Table I presents the various parameter values used for the design approach.

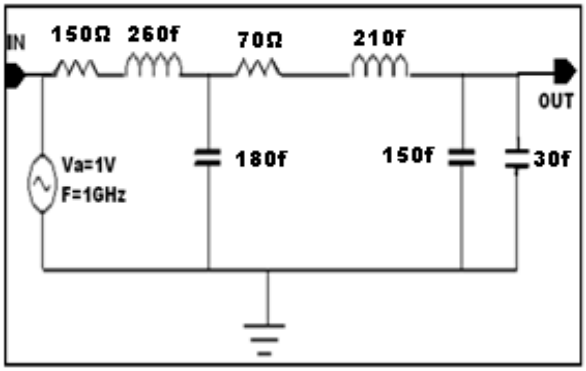

Fig. 2: Schematic of Reduced RLC Interconnect Model

Figure 2 depicts the schematic of reduced RLC interconnect model with resistance, capacitance and inductance represented per unit length terminated by the load capacitance of 30fF.

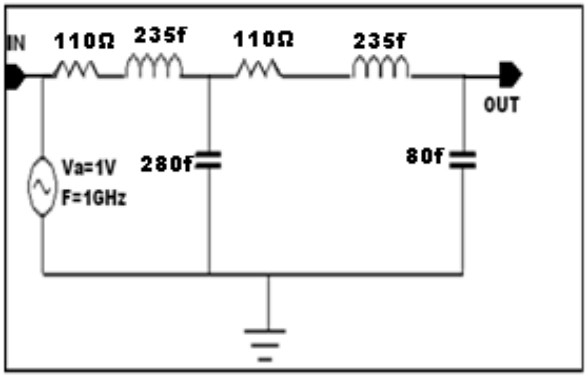

Fig. 3: Schematic of T- RLC Interconnect Model

In figure 3, the schematic of T-RLC interconnect model with resistance, capacitance and inductance taken per unit length have been implemented which is terminated with load capacitance of 80fF.

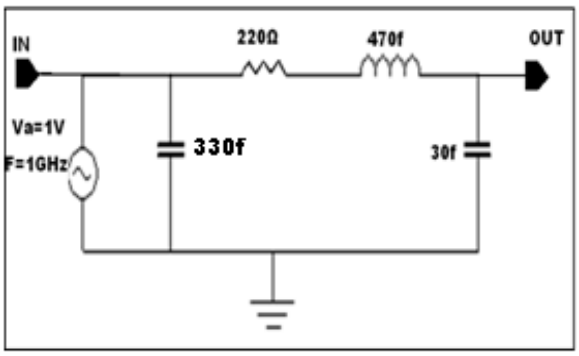

Fig. 4: Schematic of π-RLC Interconnect Model

Figure 4 presents the schematic of π-model RLC interconnect model with resistance, capacitance and inductance considered per unit length have been implemented with load capacitance of 30fF.

3. SIMULATION RESULTS AND DISCUSSIONS

For all the design models implemented, transient analysis has been done at the stop time of 5ns and at 2GHz frequency.

From figure 5, it is clear that the signal obtained at the output is distorted. This distortion leads to affect the delay. Here, the maximum output voltage observed is 881.56mV.

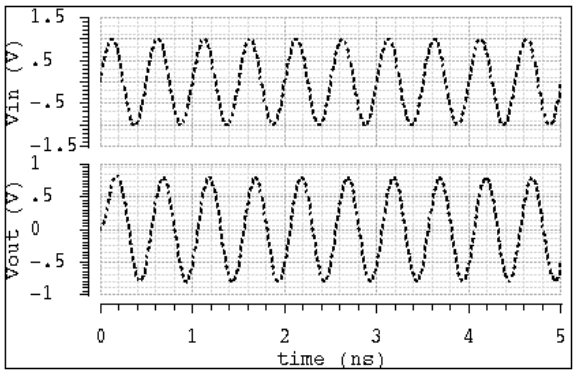

Fig. 5: Transient Analysis for Reduced tree model

Due to the distortion appeared in the output waveform observed in reduced tree model; the model has been redesigned and thus observed less distortion is produced in T-model. The maximum output voltage appeared is 923.49mV as shown in the figure 6.

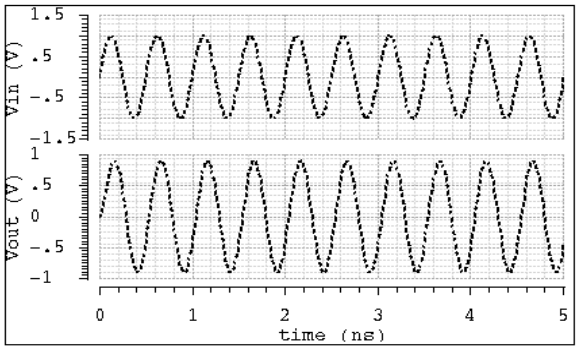

Fig. 6: Transient Analysis for T-model

In T-model, the maximum output voltage is not appreciable thus further amendments are made to obtained π-model design. On analysing the simulation results, it has been

observed that output signal is improved and the maximum output voltage appeared is 982.52mV as shown in the figure 7.

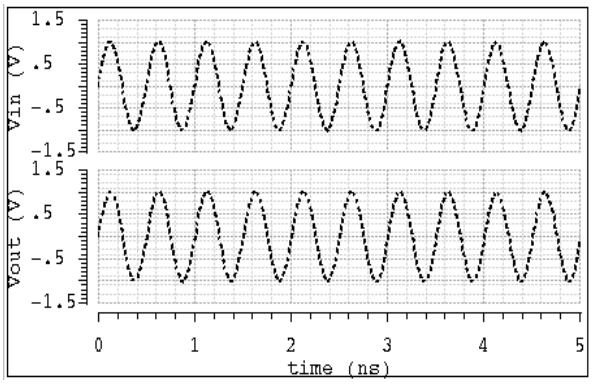

Fig. 7: Transient Analysis for π-model

From the above simulation results it has been also observed that delay is marked minimum in π-Model and power dissipation in reduced tree model for all the value of frequencies.

Table II highlights the propagation delay in the frequency range of 0.5GHz to 2GHz for all the three models. The delay is reduced by 38.424ps in π-Model as compared to reduced tree model.

Table II. Propagation Delay at different values of Frequencies

Frequency	Reduced Tree	RLC T-Model	RLC π-Model
0.1 GHz	14.2318ns	14.1896ns	14.1716ns
0.5 GHz	2.89408ns	2.85766ns	2.83723ns
1 GHz	1.47298ns	1.44146ns	1.42187ns
2 GHz	752.763ps	731.711ps	714.339ps

Table III shows the power dissipation in the frequency range of 0.5GHz to 2GHz for all the three models and it has been analysed that in reduced tree model the 7.3253a less power is dissipated as compared to the RLC π-Model.

Table III. Power Dissipation at different values of Frequencies

Frequency	Reduced Tree	RLC T-Model	RLC π-Model
0.1 GHz	55.3679zs	55.3768zs	55.4645zs
0.5 GHz	1.34023as	1.35407as	1.40897as
1 GHz	4.85656as	5.05374as	5.54207as
2 GHz	14.0653as	15.9121as	21.3906as

4. CONCLUSION

The sine wave response for different RLC VLSI interconnects delay models has been implemented. A comparative analysis for reduced tree RLC; T-model and π-model have been done. The results show that delay has been decreased with increase in frequency while there is increase in the value of power dissipated. Further π-model achieves comparatively less propagation delay as compared to the other two designs while reduced tree model attains minimum power dissipated. But for both the cases, T-model possesses moderate results. This approach can be further expanded to the different input signals like step, impulse, ramp etc.

5. REFERENCES

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