Implementation of Tunable and Non-Tunable Pseudo-Resistors using 0.18μm Technology

Kulbhushan Sharma
Department of ECE
Chitkara University
H.P, India

Lipika Gupta
Department of ECE
Chitkara University
H.P, India

ABSTRACT
This paper describes various pseudo-resistor topologies used in integrated circuits implemented to attain high value resistance. Incremental resistance for both non-tunable, tunable pseudo-resistor has been estimated in Cadence Analog Design Environment using 0.18μm technology. Pseudo-resistors make use of diode-connected MOS devices working in subthreshold region and consume less area as compared to the discrete counterpart. Different V-R curves for both non-tunable and tunable pseudo-resistors are obtained and a comparison is presented in terms of linearity and consistency. Low tuning voltages, currents and smaller W/L ratios are selected for analysis to obtain high value resistors greater than 10^{11} Ω. It also leads to the design of Low power integrated circuits

General Terms
Consistency, Linearity, Incremental Resistance.

Keywords
Tunable pseudo-resistors, topologies, integrated circuits, subthreshold region.

1. INTRODUCTION
Pseudo-resistors are MOS transistors working in subthreshold region having large value of resistance up to Tera-ohms. They are used instead of linear resistors as they consume less area for same value of resistance [1]. The pseudo-resistor was introduced by T. Delbruck as an "adaptive element" he explains that effective resistance is huge for small signals and small for large signals [2]. High performance very low frequency analog filters are required in biomedical applications, these filter circuits make use of pseudo-resistors [1].S. Hwang et al. remarked that PMOS transistor in diode configuration can be used as a tunable resistor with very low current of order of sub pA flowing through it[4]. Most of the previous works present implementation of feedback network using CMOS pseudo-resistors for attaining lower cut off frequency of Neural amplifier and for attaining range of frequencies for filter circuits[1],[3],[5],[6],[7]. Low frequency filters require large time constants, thus higher value of resistance obtained from combination of MOS devices up to Tera-Ohm range along with capacitor is desirous [7]. Pseudo-resistors can also be used in linear attenuators,R-2R network for D/A conversion, dependent linear networks etc[13].

When $V_{GS}<V_{TH}$ a very small amount of drain current flows through MOSFET. This current is called subthreshold current and the corresponding region of operation is known as weak inversion or subthreshold region. The current property has been described by EKV model. The I-V characteristics for PMOS device operating in weak inversion region is expressed as follows:

$$I_{SD} = I_{D0} \cdot e^{\frac{V_{BG}-V_{TH}}{nU_T}} \cdot \left(e^{\frac{V_{BS}}{U_T}} - e^{\frac{V_{BD}}{U_T}} \right) \quad (1)$$

Where $I_{D0} = 2n\mu Cox\ (W/Leff)\ U_T$ (n is the subthreshold slope, Cox is the gate oxide capacitance per unit area, μ is the mobility, U_T =kt/q is thermal voltage having typical value of 26mV at room temperature, $Leff$ is effective length and W is width of the transistor) and V_{TH} is the threshold voltage of the transistor[8].

The incremental resistance(r_{inc}) for MOSFET acting as pseudo-resistor is calculated by following equation[9].

$$r_{inc} = \frac{\partial V_{DS}}{\partial I_D} \quad (2)$$

Incremental resistance can be measured by taking reciprocal of the drain current derivative. In this paper various topologies of MOS-transistors as pseudo-resistors has been estimated in cadence analog design environment using standard CMOS 0.18µm technology. Incremental resistance versus resistor voltage curves for both non-tunable as well tunable resistances has been obtained.

2. NON TUNABL PSEUDO-RESISTOR IMPLEMENTATION
Non tunable pseudo-resistors were used to attain high value of resistance and consume less area as compared linear resistance. Non Tunable pseudo-resistors have incremental resistance greater than $10^{11}\Omega$ but magnitude of resistance cannot be controlled [10]. In Non tunable pseudo-resistor the body of the PMOS transistors is tied either to drain or to the source and have fixed value of resistance. Fig. 1 [10] shows various topologies of non-tunable pseudo-resistors and their corresponding V-R curves are shown Fig. 2(a)–(d).In these topologies gate and bulk terminal of the MOSFET is connected either to the source or to the drain and depending on connection topology different value of resistance is obtained. The source to drain voltage has been swept from -1V to 1V and W/L ratios for MOS pseudo-resistance is selected to be (0.6/18) μm to make them work in subthreshold region. Although higher value of resistance of the order of tera-ohms is easily achieved with the help of non tunable pseudo-resistors yet non-linearity and inconsistency in resistance exists.

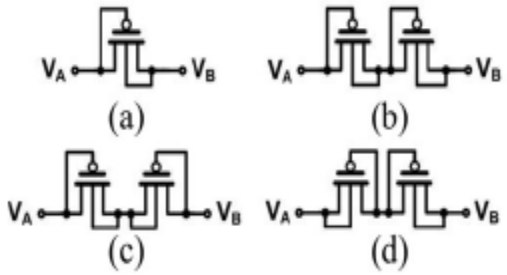


Fig. 1. Non Tunable pseudo-resistor structure: (a) Single MOS bipolar pseudo- resistor; (b)Two series connected MOS pseudo- resistors; (c) Two series connected MOS pseudo- resistor structure with outwardly connected gates; (d)Two series connected MOS pseudo- resistor structure with inwardly connected gates.[10]

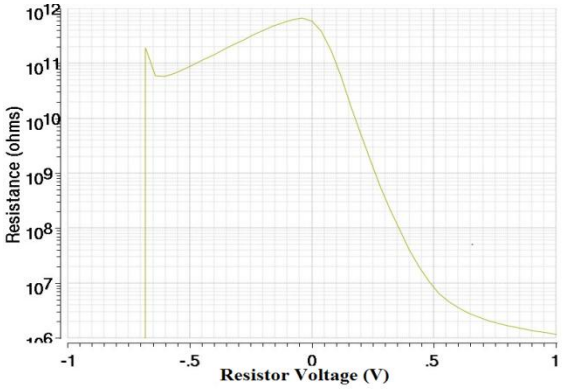


Fig. 2(a) Resistance variations versus voltage across resistor of Fig. 1(a)

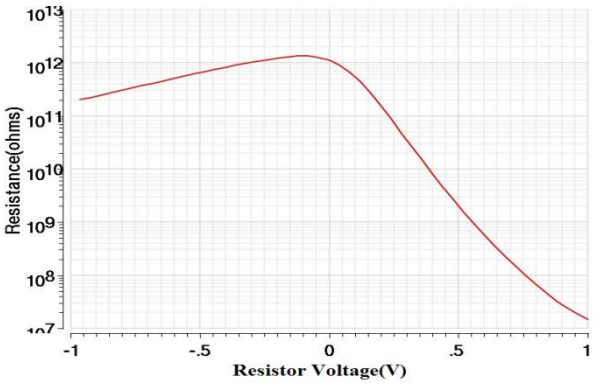


Fig. 2(b) Resistance variations versus voltage across resistor of Fig. 1(b)

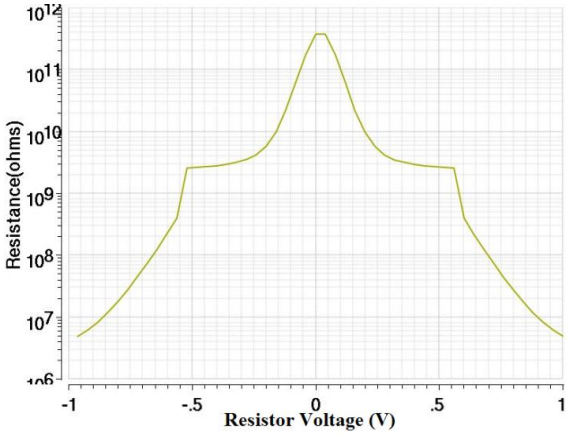


Fig. 2(c) Resistance variations versus voltage across resistor of Fig. 1(c)

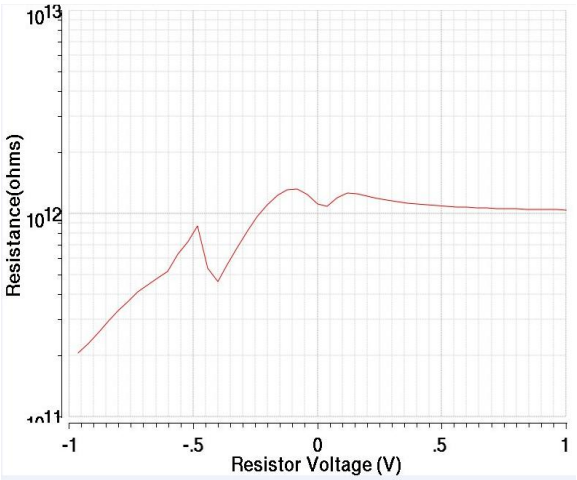
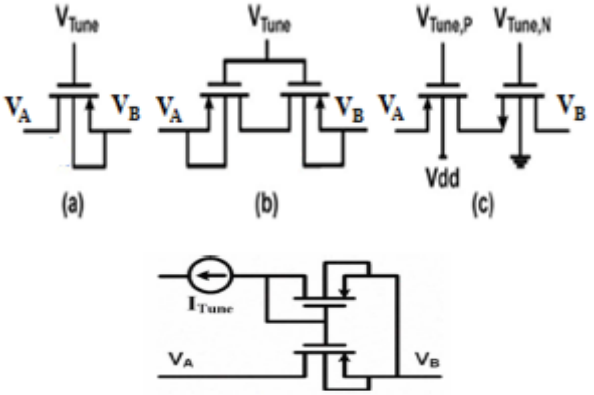


Fig. 2(d) Resistance variations versus voltage across resistor of Fig. 1(d)

3. TUNABLE PSEUDO-RESISTOR IMPLEMENTATION

Non- tunable pseudo-resistors have been replaced by tunable pseudo-resistors due to their inconsistent and nonlinear behavior. Various tunable pseudo-resistors implementation has been shown in Fig. 3. [11], [12] along with their V-R curves shown in Fig. 4(a)–(d). MOSFET biased in subthreshold region can act as a linear resistor in a circuit where the resistance is controlled by the gate voltage. The voltage between the terminals A and B of MOS pseudo-resistors is swept from −1V to +1V and corresponding variations in resistance for different gate voltages has been shown for different types of voltage controlled pseudo-resistors.One of the basic structures of voltage controlled MOS pseudo-resistor is shown in Fig. 3(a), the structure can modified to obtain higher value of resistance as shown in Fig. 3(b). The disadvantage of above mentioned pseudo-resistors is that the resistance falls precipitously for positive values of source to drain voltages, thus limiting dynamic voltage range. Complementary MOS pseudo-resistors shown in Fig. 3(c) provide wide range of tenability with higher value of resistance greater than 10^{12} Ω. For better performance PMOS and NMOS pseudo-resistors can be tuned appropriately as per requirement and application. In our work gate voltages $V_{Tune,P}$ and $V_{Tune,N}$ has been tuned to -0.1 and -0.2 respectively. NMOS pseudo-resistors consume less area than PMOS but introduce more noise.

Incremental Resistance of current-controlled MOS pseudo-resistor greater than 10^{11} Ω has been obtained shown in Fig. 4(d). The value of resistance depends on the current source; higher value of resistance can be obtained by forcing very small amount of current ranging from 0.01pA to 2μA through pseudo-resistor with the help of current source (I_{Tune}). A wider linear range of resistance is established with the help of current controlled pseudo-resistor. It can be observed that more linear and consistent curves are obtained with the tunable pseudo-resistor. Moreover current controlled pseudo-resistors introduce less noise as compared to pseudo-resistor topologies.



(d)

Fig. 3 Voltage controlled pseudo-resistor structure: (a) gate-voltage controlled single MOS bipolar pseudo-resistor structure ; (b) gate-voltage-controlled two series connected MOS pseudo-resistor structure (c) complementary MOS pseudo-resistor structure (d) current-controlled MOS pseudo-resistor structure [11] [12].

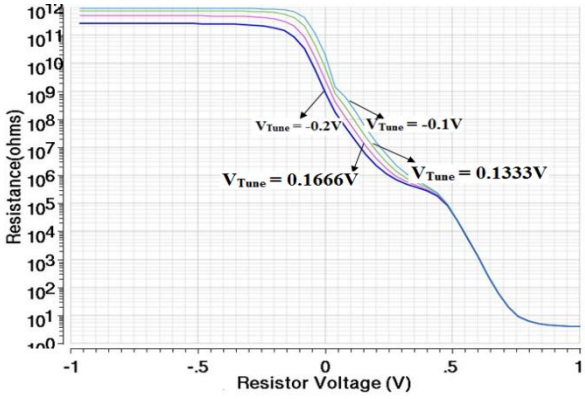


Fig. 4(a) Resistance variations versus voltage across resistor of Fig. 3(a)

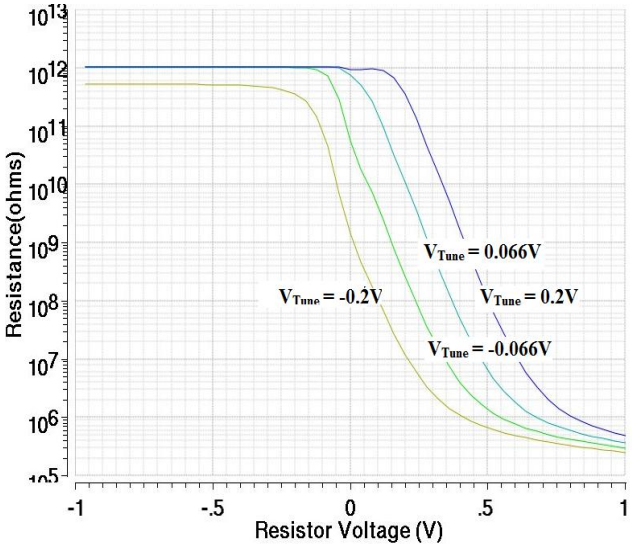


Fig. 4 (b) Resistance variations versus voltage across resistor of Fig. 3(b)

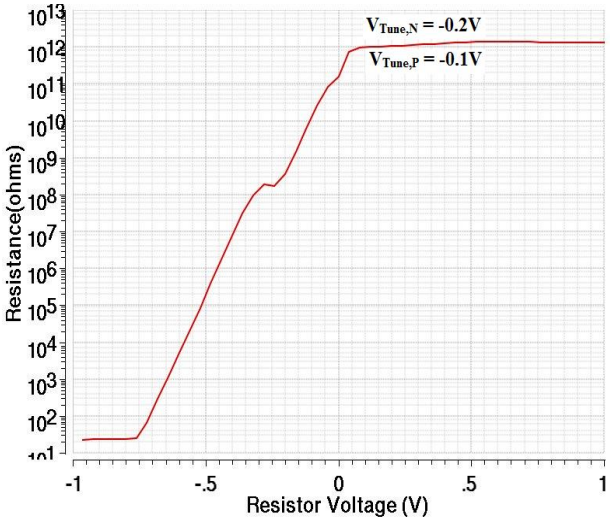


Fig. 4 (c) Resistance variations versus voltage across resistor of Fig. 3(c)

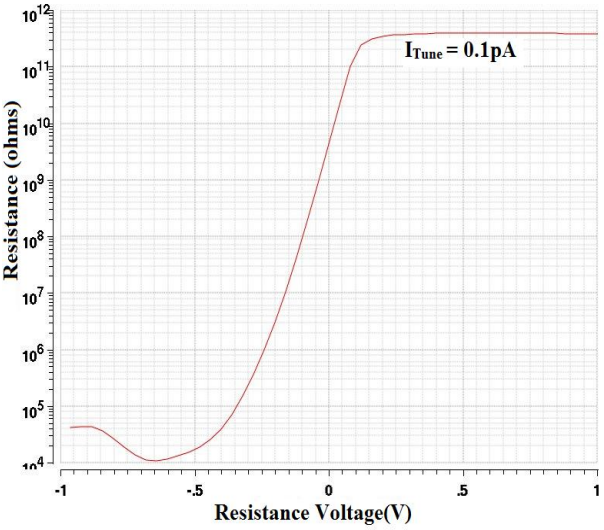


Fig. 4 (c) Resistance variations versus voltage across resistor of Fig. 3(d)

Table 1: Comparison of different pseudo-resistors.

S.NO	Pseudo-resistor Topology	Magnitude of Resistance (Ω)	Linearity of Resistor Topology
1	Single MOS bipolar pseudo- resistor	$< 10^{12}$ Ω	Highly Non-linear
2	Two series connected MOS pseudo-resistor	$< 10^{12}$ Ω	Highly Non-linear
3	Two series connected MOS pseudo-resistor structure with outwardly connected gates	$< 10^{12}$ Ω	Symmetrical but Non-linear
4	Two series connected MOS pseudo-resistor structure with inwardly connected gates	$\leq 10^{12}$ Ω	Non-linear
5	Gate-voltage controlled single MOS bipolar pseudo-resistor structure	$\leq 10^{12}$ Ω (Magnitude of resistance depends on applied gate to source voltage)	Linear for negative values of applied drain to source voltage
6	Gate-voltage-controlled two series connected MOS pseudo-resistor structure	$\leq 10^{12}$ Ω (Magnitude of resistance depends on applied gate to source voltage)	Linear for negative values of applied drain to source voltage
7	Complementary MOS pseudo-resistor structure	$\leq 10^{12}$ Ω (Magnitude of resistance depends on applied gate to source voltage)	Linear for positive values of applied drain to source voltage
8	Current-controlled MOS pseudo-resistor structure	$\leq 10^{12}$ Ω (Magnitude of resistance depends on magnitude of current)	Linear for positive values of applied drain to source voltage

4. RESULTS AND DISCUSSIONS

Table I shows comparison of different pseudo-resistor topologies on the basis of magnitude of resistance and linearity. Single MOS bipolar and two series connected MOS pseudo-resistors are able to achieve ultra high resistance, but resistance variations are highly non-linear with applied voltage. Two series connected MOS pseudo- resistor structure with outwardly connected gates has symmetrical variations of resistance for both positive and negative values of swept voltage, but still nonlinearity in resistance exists. Gate-voltage controlled single and double MOS bipolar pseudo-resistor structure shows linearity in resistance for negative values of applied drain to source voltage. Complementary MOS pseudo-resistor structure and current-controlled MOS pseudo-resistor structure shows Linear for positive values of applied drain to source voltage. In tunable voltage pseudo-resistor magnitude of resistance depends on applied gate to source voltage and can be increased up to 10^{12} Ω. In current controlled pseudo-resistor, resistance depends on the current being forced into the pseudo-resistor and small magnitude of current has to be forced into pseudo-resistor for achieving high value of resistance.

5. CONCLUSION

This work is focused on various pseudo-resistor implementations. Different V-R curves for different MOS pseudo-resistor have been obtained. Low tuning voltages and currents has been intentionally supplied to the MOS devices so that these devices can work in subthreshold region of operation. Even Smaller W/L ratios of MOS devices have been selected along with low tunable voltage and currents so that these circuits consume low power. This pseudo-resistor can be used for different application in integrated circuit such as amplifiers, filters analog to digital convertors voltage divider circuits etc where traditional resistors consume large area and power. Moreover noise analysis of all these pseudo-resistors can be done and noise introduced by them in different circuits can be reduced to optimum level. More work can be done in developing a pseudo-resistor which has high degree of linearity like traditional resistor over positive as

well as negative swept voltages by making use of switched capacitors and mixed signal circuits.

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