TCAD Assessment of Oxide Impact on Linearity and Harmonic Distortions in Gate All Around (GAA) MOSFET

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ABSTRACT
In this paper for the first time the effect of different oxides namely Hafnium Oxide (HfO_2), Silicon Oxide (SiO_2) and air have been studied and analyzed for Gate All Around (GAA) MOSFET in context of linearity and harmonic distortions and high frequency operation. Various linearity metrics such as third order derivative of transconductance (g_{m3}), V_{IP2}, V_{IP3} and IIP3 have been studied and analyzed for GAA MOSFET using different dielectrics. We have also studied Maximum Transducer Power Gain (MTPG), Unilateral Power Gain (UPG), gate capacitance (C_{GG}) and maximum cut off frequency (f_{Tmax}). Along with linearity metrics various analog metrics have been examined like drain currents (I_{ds}), ON to OFF current ratio, transconductance and output conductance. Hafnium Oxide (HfO_2) is more suitable for analog applications and air is more suitable as a dielectric for high linearity applications.

Keywords
Nanowire, Harmonic Short Channel Effects, Linearity, ATLAS 3D.

1. INTRODUCTION
The explosive growth in mobile telecommunication has created demand of high levels of integration and cost effective technologies [1-3]. It has led to a continuous need of device and CMOS technologies which can provide speed along with extended chip density at economical prices. Nowadays with the continuous advancement in CMOS technology has resulted in high speed MOS devices suitable for analog RF and wireless applications. So MOSFETs attracted huge interest for RF application [4–6]. Prerequisites for employing MOSFET for high frequency applications are high linearity and lower harmonic distortion so as to distortion free transmission of signals. Linearity is an important parameter which is desired for both analog and radio frequency circuits. By managing the linearity of the device we can somehow lower down the distortions and it simplifies the design. Non - linearity can cause intermodulation (IM) which results in frequencies other from the input ones. These signals will interfere with the desired result and may corrupt the main signal [1]. So, it highly desirable to improve the linearity of the device so as to increase the device resistance against signal interference. However, MOSFETS are inherently not quite linear. Although linearity can be improved at system-level but they all require complex circuitry [1]. While using conventional long channel MOSFET, they obey the square law, which deviates much from linear drain current versus gate voltage or I_D–V_G relation. The short channel devices show higher distortion with limited linearity along with other SCE's. SCE's are significantly reduced by employing Gate All Around (GAA) MOSFET. In GAA MOSFET the gate completely wraps the channel so as to increase the gate control multifold times and thus reducing SCE's. To improve the immunity against short channel effects SCEs, analysis are made on the conventional Gate All Around (GAA) MOSFET to study the effect of oxide on the distortions of the device. To get success in designing highly linear sophisticated circuits, this analysis will help in order to minimize the nonlinearities from MOS transistors. Since two dominant nonlinear sources i.e. trans- conductance and output conductance affects the linearity of the device [7].

The important device parameters for determining linearity and RF applications are trans-conductance (g_{m3}). Trans conductance (g_m) show the various Figure of Merits (FoM) namely V_{IP2} and V_{IP3} used to assess linearity [8-10]. In this present work, linearity and intermodulation distortion performance of the GAA MOSFET has been studied and compared for different oxides (HfO_2, SiO_2, air) in terms of V_{IP2}, V_{IP3}, IIP3, g_{m1}, g_{m2}, and g_{m3} for optimum bias point selection using an ATLAS 3-D device simulator [11]. Maximum transducer power gain, current gain, unilateral power gain, gate capacitance and cut off frequency is also compared for all the three oxides. Section II presents the device structure .Section III shows the results and discussion of the analysis. The conclusions of our study are summarized in Section IV.

2. DEVICE STRUCTURE AND DESCRIPTION
Gate All Around (GAA) MOSFET is a 3D MOSFET with a gate completely wrapped around the channel over the oxide in a cylindrical form showing improved drain current in channel by maintaining the value of supply gate voltage. Figure 1 (a) and 1 (b) shows the three dimensional and cross sectional view of GAA MOSFET respectively.

GAA MOSFET is a 2D cylindrical form with channel having a thickness of 2R, where R is the radius of the silicon film, oxide of thickness (tox) is grown over the channel with a gate completely covering the channel in cylindrical form. The oxide has been varied in our analysis with relative permittivity () of 1.0, 3.9, 22.0 for air, silicon oxide and hafnium oxide respectively.

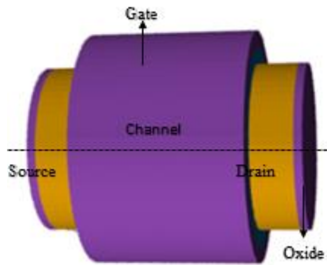

Figure 1(a). 3D view of GAA MOSFET

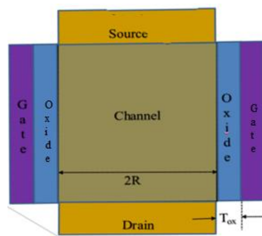

Figure 1(b).Cross sectional view of GAA MOSFET

Three-dimensional simulation of device has been carried out using ATLAS-3D device simulator using concentration dependence SRH recombination/thermal generation model (CONMOB), FLDMOB model for high electric field velocity saturation, and Boltzmann carrier statistics for electron and holes. Table I (a) shows the various device parameters. Hafnium oxide (HfO_2) with relative permittivity $\varepsilon_r = 22.0$, Silicon Oxide (SiO_2) with relative permittivity $\varepsilon_r = 3.9$ and air with relative permittivity $\varepsilon_r = 1.0$ have been taken as dielectrics for analysis. The threshold voltage of these devices has been optimized to 0.5 V by varying the metal gate work function. Table I (b) shows the metal gate work function for air, SiO_2 and HfO_2 as the gate dielectric. Molybdenum (Mo) has been used as the metal [12]. GAA MOSFET with air dielectric was recently proposed by Han et al. [13] which is resistant to radiation and stress damage due to absence of solid material.

Table 1(a) The device parameters used for simulation

Parameters	Value
Channel Length, L (nm)	40
Source/Drain Length (nm)	10
Channel Doping(/cm^3)	$1*10^{16}$
Silicon Oxide Thickness, t_{ox} (nm)	2
Silicon Film Thickness, t_{si} (nm)	20

Table 1(b) Values of gate work function at different permitivity

Parameters	Air	SiO_2	HfO_2
Work Function (eV)	4.831	4.80	4.787

3. RESULTS AND DISCUSSION

Figure 2 shows the variation of drain current with respect to applied gate bias. It shows that using HfO_2 as the gate dielectric shows the highest drain current and using air as the gate dielectric exhibits lowest drain current. It is so because HfO_2 has higher oxide permittivity than air. As the drain current is a directly dependent upon the oxide permittivity. So high k dielectrics higher drain current is obtained.

From same figure we can see low gate current is obtained in air dielectric's case and it has been already shown in [13] that even if generation of hot carrier/impact ionization occurs, it cannot damage the air gate dielectric because the injected hot-carriers are collected by the gate electrode (as no solid material is present) [13]. Thus, air dielectric has better hot carrier reliability [13].

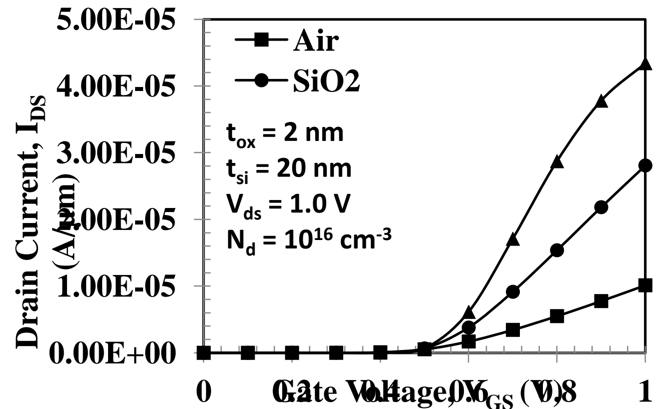

Figure 2. Variation of Drain Current with Gate to Source Voltage(Vgs)

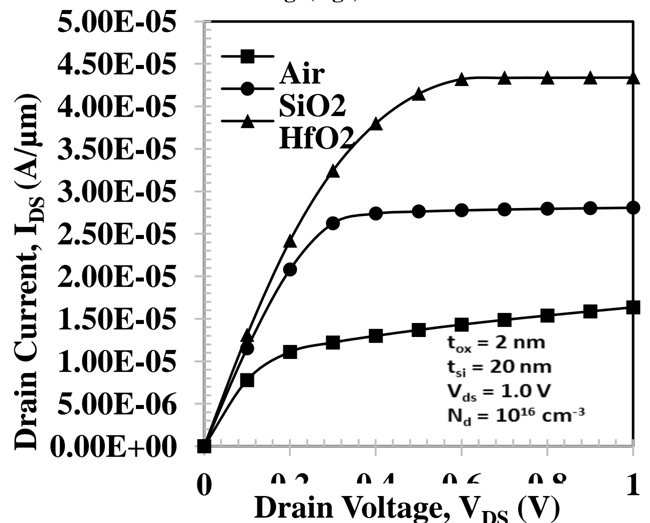

Figure 3. Variation of Drain Current with Gate to Drain Voltage (Vds).

Figure 3 shows the variation of drain current with respect to applied drain bias. It shows that using HfO_2 as the gate dielectric shows the highest drain current and using air as the gate dielectric exhibits lowest drain current. It is so because HfO_2 has higher oxide permittivity than air. As the drain current is a directly dependent upon the oxide permittivity. So high k dielectrics higher drain current is obtained. Figure 4 shows I_{on}/I_{off} ratio. It is the figure of merit (FoM) for CMOS transistor for showing high performance and low leakage power. Using HfO_2 as the gate dielectric highest I_{on}/I_{off} ratio is observed. It is so because of the higher drain currents that are observed in HfO_2.

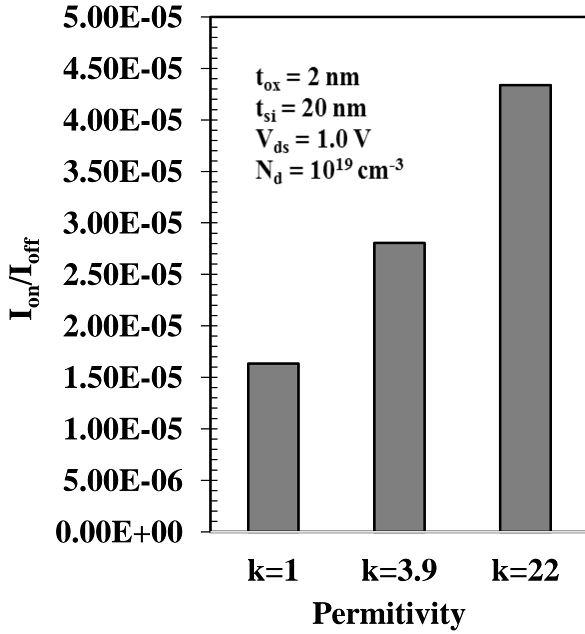

Figure 4. Variation of I_{on}/I_{off}, for all the three permittivities.

The high frequency operation of the device is directed by Transconductance (gm) [14]. Figure 5 represents the variation in transconducatnce (g_m) with the variation in the gate voltage (V_{gs}). It can observed from the figure that by using HfO_2 as a gate dielectric we can obtain higher transconductance. It is so because of the higher drain currents that are observed in HfO_2 as seen in Figure 2.

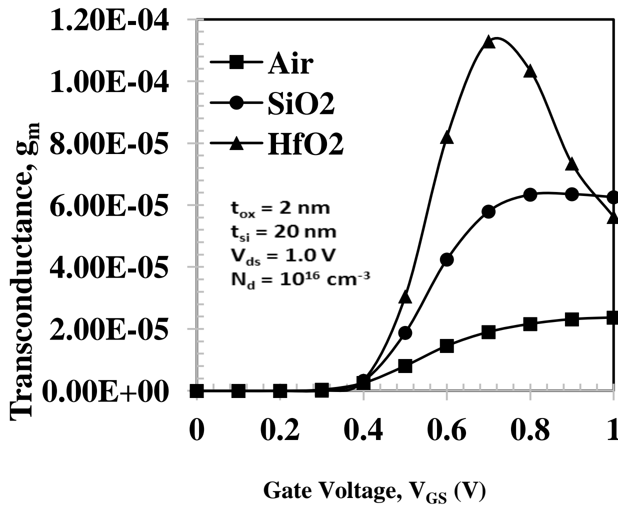

Figure 5. Variation of transconductance with Gate to Source Voltage (Vgs).

The change in the drain current with respect to change in the gate voltage explains the outputconductance (g_d) It can observed from the Figure 6 that by using HfO_2 as a gate dielectric we can obtain higher output conductance. It is so because of the higher drain currents that are observed in HfO_2 as seen in Figure 3.

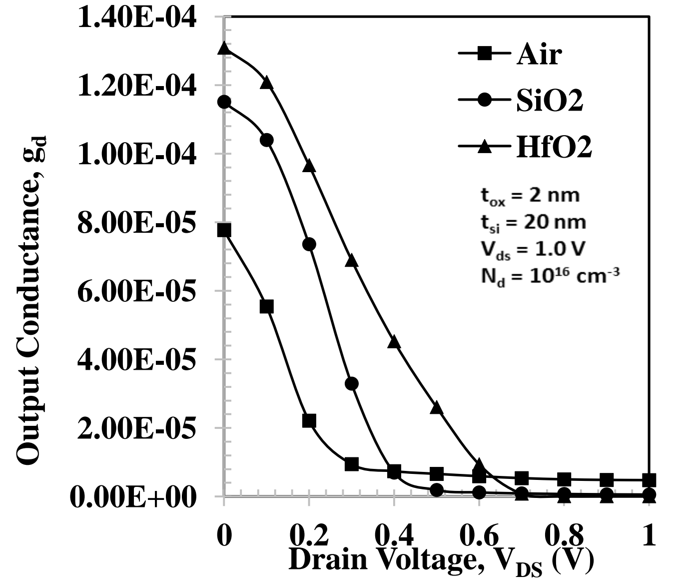

Figure 6. Variation of output conductance with Gate to Drain Voltage (Vds).

Third order derivative of transconductance (g_{m3}) is another important MOSFET parameter as it explains the linearity of the device.

$$gmn = \frac{1}{n!} * \frac{dIds}{dVgs};\ \text{n=1,2,3} \quad (1)$$

It should be as low as possible so as to ensure the non linear behaviour of the device. Figure 7 represents the change in g_{m3} with the change in the gate voltage (V_{gs}). It can observed from the figure that by using HfO_2 as a gate dielectric higher g_{m3} is obtained and by using air as dielectric lowest gm3 is obtained. So, in order to obtain higher high linearity air should be used as a gate dielectric.

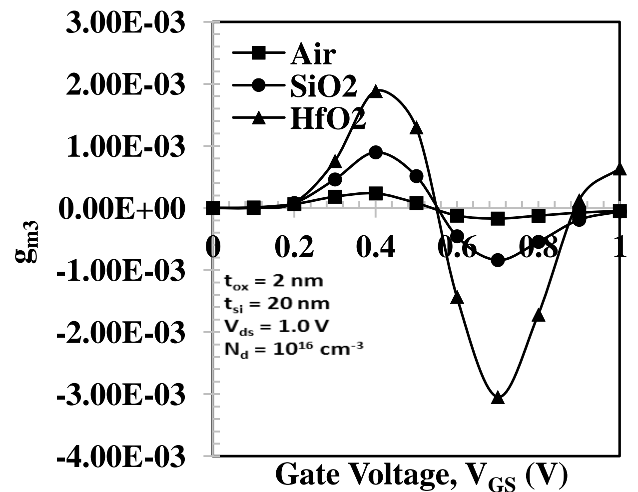

Figure 7. Variation of high order transconductance with Gate to Source Voltage (Vgs).

V_{IP2} and V_{IP3} are the extrapolated gate voltages and they are important Figure Of Merits (FOM) to determine the linearity of the device. They are formulated as:-

$$VIP2 = 4 * \frac{gm1}{gm2} \quad (2)$$

$$VIP3 = \sqrt{24 * \frac{gm1}{gm2}} \quad (3)$$

V_{IP2} and V_{IP3} should be as high as possible to ensure high linearity and low harmonic distortions in the device. Figure 8 and Figure 9 show V_{IP2} and V_{IP3} of GAA MOSFET for different gate dielectrics. As observed from Figure 8 and 9, V_{IP2} and V_{IP3} are highest when air is used as a gate dielectric and lowest when HfO_2 is used as a gate dielectric. This is so because using air as a gate dielectric leads reduction in gate leakages and increase in the carrier transport efficiency leading to an improvement in the linearity of the device.

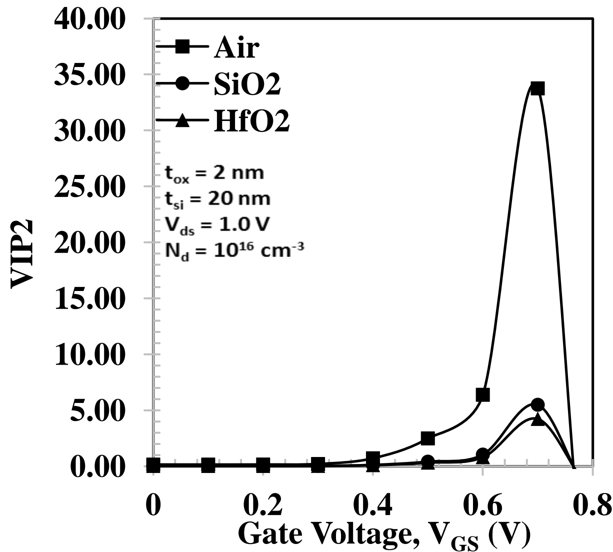

Figure 8. Variation of V_{IP2} with Gate to Source Voltage (Vgs)

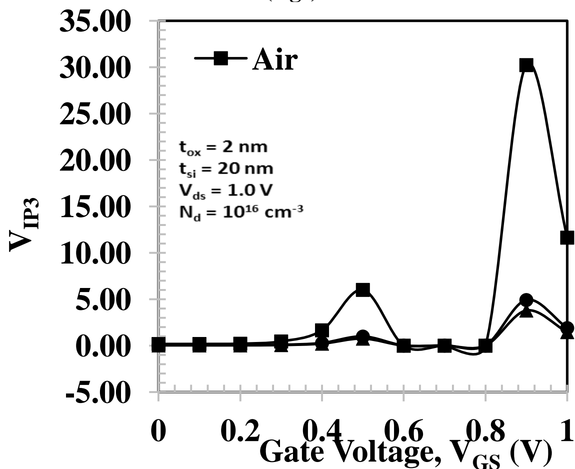

Figure 9. Variation of V_{IP3} with with Gate to Source Voltage (Vgs)

IIP3 is the third order modulation intercept. It is formulated as:-

$$IIP3 = \frac{2}{3} * \frac{gm1}{gm3 * Rs} \quad (4)$$

Where $R_s = 50\ \Omega$ for most of the RF applications.

IIP3 should be high so as to ensure high linearity and to lower harmonic distortion. Figure 10 shows the change in IIP3 with the gate voltage. It can be observed from the figure that IIP3 is maximum when air is used as a gate dielectric and lowest when HfO_2 is used as a gate dielectric. So, air as a dielectric is more suitable for high linearity applications.

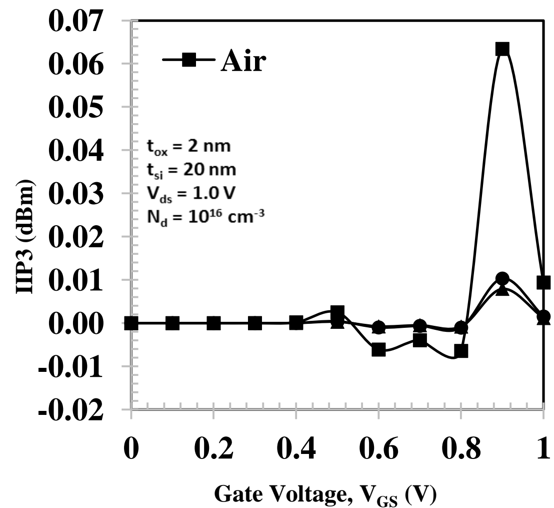

Figure 10. Variation of third-order input intercept point (IIP3) with Gate to Source Voltage (Vgs).

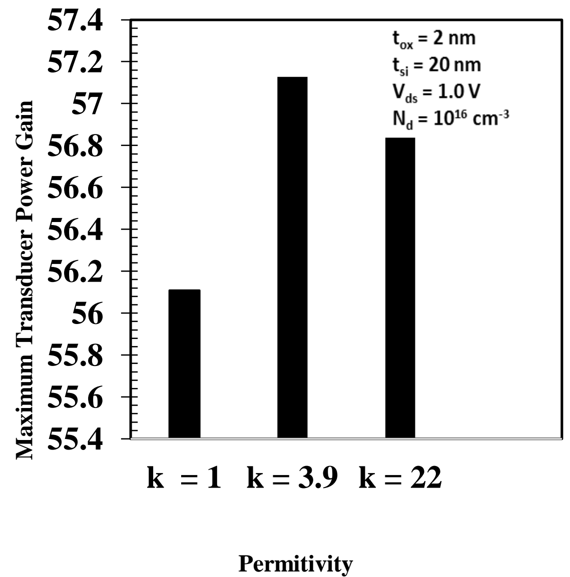

Figure 11. Variation of Maximum transducer power for all the three permittivities

Figure 11 explains the relation which shows SiO_2 has maximum transducer power gain (MTPG) from all the three permittivity. It can be seen from the figure that when silicon oxide is used as a dielectric highest MTPG has been obtained. For high power gain applications silicon oxide as a dielectric is highly applicable.

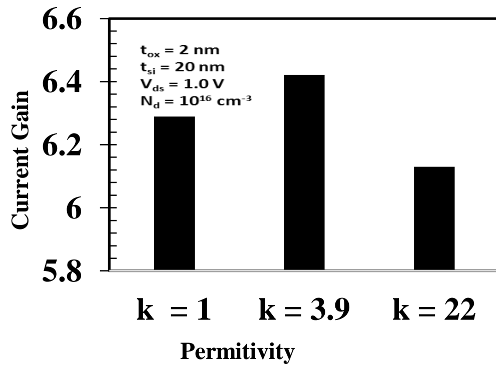

Figure 12. Variation of Current gain, for all the three permittivities

Similarly, in figure 12 the SiO_2 has maximum current gain from all the three permittivity. . It can be seen from the figure that when silicon oxide is used as a dielectric highest current gain has been obtained. So for high current gain applications silicon oxide as a dielectric is highly desirable.

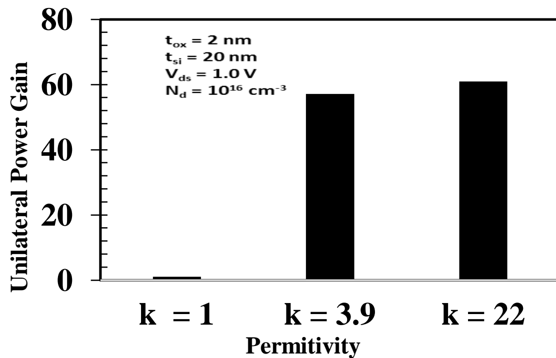

Figure 13. Variation of Unilateral power gain, for all the three permittivities

Figure 13 shows HfO_2 has relatively higher unilateral power gain among all the three permittivities. As observed from figure by employing HfO2 as a gate dielectric highest unilateral power gain is obtained, so hafnium oxide as a dielectric is desirable for high unilateral power gain applications.

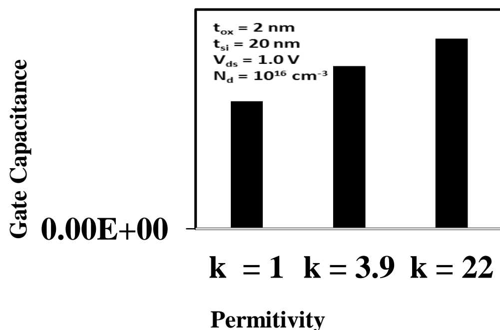

Figure 14. Variation of Gate capacitance, for all the three permittivities

From figure 14 we can conclude that gate capacitance is increasing as the permitvity is increasing so it is least for air and going high for HfO_2. Highest gate capacitance is obtained by employing hafnium oxide as a gate dielectric because of the fringing field capacitance that come into action.

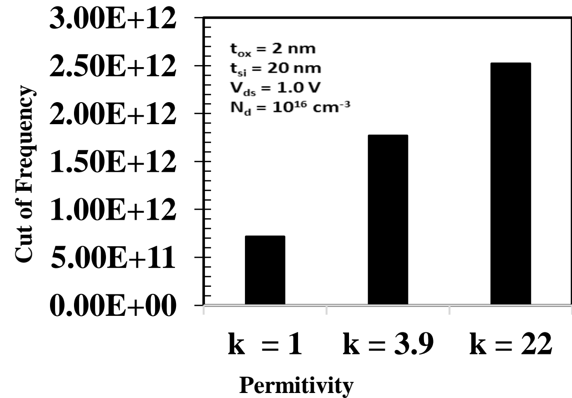

Figure 15. Variation of Cut off frequency, for all the three permittivities

Cut off frequency known as f_t can be defined as:

$$f_T = \frac{g_m}{2\pi C_{gg}}$$

And in this also it is increasing as the permitivity is rising so we observed that for air it is lowest and for HfO2 it is maximum.

Table 2. The performance parameter for the device

Performance Parameter	Air	SiO_2	HfO_2
I_{ds} (uA)	$1.02*10^{-5}$	$2.70*10^{-5}$	$4.48*10^{-4}$
Peak g_m (S)	$2.37*10^{-5}$	$6.35*10^{-5}$	$1.13*10^{-4}$
Peak g_{m3} (S)	$2.36*10^{-4}$	$8.98*10^{-4}$	$1.88*10^{-3}$
V_{IP2}	4.71	5.04	35.04
V_{IP2}	4.00	4.12	31.01
IIP3	0.062	0.01	0.0092

4. CONCLUSION

In this article we have analyzed the effect of different gate dielectrics on the Linearity and Harmonic of GAA MOSFET. It has been observed that air is more suitable as a dielectric for high linearity applications as it shows higher magnitudes of VIP2, VIP3, IIP3 along with a lower magnitude of g_{m3}. Thus, GAA MOSFET with air dielectric outperforms GAA MOSFET with SiO2 dielectric for high speed RF applications along with advantages of immunity against hot carrier/radiation damages. However SiO_2 does not show higher drain current, transconductance and other analog performance parameters. However when HfO_2 as a dielectric is more suitable for analog applications but it shows high harmonic distortions. So, the choice of the dielectric should be according to the application. For high linearity low k dielectrics are more suitable than high k gate dielectrics.

5. ACKNOWLEDGEMENT

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