Analysis of Low Leakage and High Performance 4 bit CLA Full Adder

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ABSTRACT
This paper presents implementation and analysis of ISCAS 85 74283 and various techniques minimizing the leakage current of ISCAS 85 74283, as leakage current has become a significant contributor of overall power dissipation of CMOS circuits. Various parameters such as effect of variation of supply voltage, width and threshold voltage and their impact on static power have been studied. Minimizing static power is major issue as static power has become comparable to dynamic power at sub-micron technologies. Various CLA is implemented on SPICE at 32nm technology. Leakage current reduction circuit techniques reduces considerable amount of power but may have various trade-offs in terms of delay and area

General Terms
Low power VLSI, VLSI circuit design, low power and high performance carry look ahead adder circuit,

Keywords
CLA, Full Adder, ISCAS 85 74283, leakage current mechanism, static power

1. INTRODUCTION
Historically, when first transistors were evolved, there were technologies based on BJT, NMOS to design integrated circuits. With evolution of CMOS technology it was realized that power consumption reduced considerably as static power dissipation of CMOS circuits is ideally zero reason being that there is never a complete path between Vdd and ground. But later as the technology shrink down it was realized that scaling down the technology i.e. transistor size leads to change in junction functionality that causes leakage in transistor and these leaky transistor completes the rail between Vdd and ground. The significant interest in power reduction is because of two reasons. Firstly it is associated with cooling consideration of high performance circuits. Excess heat due to power dissipation must be removed from the system on which circuit is mounted. Secondly it is associated with portability of device [1]. With goal of low power consumption circuit development above listed two demands might be addressed.

The demand for better performance integrated with sufficient functionalities drive chip makers towards nano-scale technology. CMOS transistors are scaled for more than 30 years as per Moore law to achieve high density and performance [1]. Moore law states that transistor per unit area doubles in every 18 months or area of device reduces to half of its size in every 18 months. But it should be noted that Moore's law is not only about chip density or portability; it also states about power dissipation in chip, market growth, performance enhancement and emerging applications of semiconductors [1]. As technology is scaled down delay time decreases by more than 30% per technology generation but on the other hand, power density is becoming a major concern. In 180n technology the overall power including dynamic as well as static power has been the major concern. But as per ITRS report, as technology shrinks down to 90n and below static power consumption becomes comparable to dynamic power [2].

The ITRS report projects a decrease in dynamic power per device over time due to scaling of Vdd. However, if we assume a doubling of on-chip devices every two years, total dynamic power will increase on a per-chip basis. Packaging and cooling costs as well as the limited power capacity of batteries make this trend unsustainable.

2. ANALYSIS OF CLA
CLA is a fastest adder as it is designed to calculate carry in advance i.e. it calculates the carry before performing the sum as shown in fig 1.

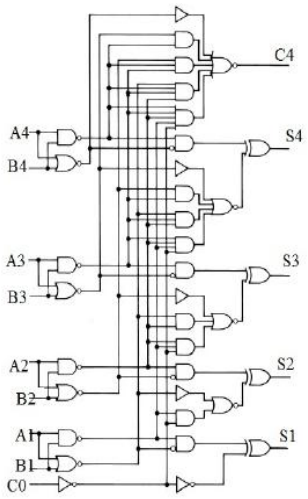

Figure 1. Circuit under test ISCAS 85 74283

CLA basically has three modules generator (M1), propagator (M2) and adder (M3). CLA reduces computation time by determining carry in advance before computation of sum and propagating it to next set of bit. Operation of CLA depends on two things firstly, bit wise operation to know if particular bit position is propagating carry and secondly, combining calculated results and quickly calculating the resultant sum [3].

As already mentioned earlier CLA work on generation and propagation of carry. Generated and propagated carry are given by Gi and Pi.

$$G_i = A_i * B_i \qquad 1$$

$$\boldsymbol{P_i = A_i \oplus B_i} \quad 2$$

By the above equations Ci at various positions can be calculated by equation above and finally when all the carries are known it takes very small time to compute sum. Sum is calculated using equation below

$$\boldsymbol{C_{i+1} = G_i + P_i C_i} \quad 3$$

$$\boldsymbol{S_i = P_i \oplus C_i} \quad 4$$

In order to apply any power minimizing technique, first of all circuit should be analyzed for minimizing its power and delay. Of the four inputs, delay for computation of carry is minimum because of the minimum propagation path. Critical path for the CLA circuit is for S1. Transistor sizing of CLA is also done to equalize rise time and fall time. Sizing ratio can be calculated using mobility provided by model file of device. In case of 32nm nominal transistor sizing ratio calculated as 9.9 and gate sizing was done accordingly.

3. LEAKAGE CURRENT MECHANISM

Leakage current flows through the conductive part of circuit to ground during static operation region of any CMOS VLSI circuit. With scaling of technology leakage current mechanism involve many components as shown in fig. 2. In old technologies such as long channel devices only subthreshold leakage was dominant but in current and future technologies gate leakage and leakage due to tunneling have also become significant. There are 6 components involved in leakage current mechanism [4].

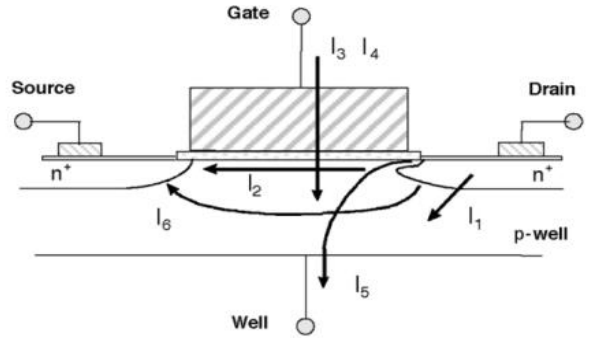

Figure 2. Leakage current mechanism of deep submicron transistor

I1-reverse-bias PN junction leakage

I2-subthreshold leakage

I3-oxide tunneling current

I4-gate current due to hot-carrier injection

I5-GIDL and

I6-Channel punch through current.

Currents I2, I5, and I6, are off-state leakage mechanisms, while I1 and I3 occur in both ON and OFF states. I4 can occur in the off state, but more typically occurs during the transistor bias states in transition.

3.1 Reverse bias PN junction

Minority carrier diffusion/drift near the edge of the depletion region and electron-hole pair generation in the depletion region of the reverse-biased junction gives rise to reverse pn junction current. It is the function of junction area and doping concentration. Band to band tunneling (BTBT) dominate pn junction current.

At junction of drain or source- n type or p type- and substrate- p type or n type- parasitic diodes are formed. At off time of MOSFET a reverse current flows through diodes, i.e. reverse diode current given by expression (7).

$$I_{rev} = A * J_s * \left(e^{(qVbias/kT)-1}\right) \quad 5$$

Reverse leakage current is function of junction area and also doping concentration. As the doping concentration increase band to band tunneling dominates the PN junction leakage. Necessary condition for band to band tunneling is when the junction voltage is more than silicon band gap. When the PN junction is in reverse bias region, a high electric field at junction causes large current to flow through junction. BTBT current density is given by equation (6)-

$$J_{b-b} = A\left(\zeta V_{in}/E_g^{1/2}\right)exp\left(-BE_g^{3/2}/\zeta\right) 6$$

ζ in above expression is electric field across junction and Eg is silicon band gap energy.

3.2 Sub threshold leakage current-

This current flows from source to drain when gate to source voltage is less than or comparable to Vth in weak inversion region **[5]**. For digital circuits, subthreshold conduction is parasitic leakage. Shrinking of transistor size caused chip density to increase that is higher power dissipation in same area. Operating the high density chip at same supply voltage causes reliability issues, solution to which is decreasing supply voltage by scaling Vth down. And because of this scaled Vth static current become limiting factor in weak inversion region which falls between linear and cut-off region. Drain to source current in weak inversion region is given by expression (9)

$$\boldsymbol{I_{sub} = I_0 exp\left(\left(V_{gs} - V_{th0} - \eta V_{ds} + \gamma V_{bs}\right)/nV_T\right)\left(1 - exp(-V_{ds}/V_T)\right)}$$

3.3 Oxide tunneling current

As the thickness of oxide layer is reduced electric field across oxide is increased. This high electric field results into the tunneling of electron from substrate to gate or from gate to substrate.

3.4 Gate current due to high carrier injection

This effect occurs in short channel devices due to high electric field at Si-SiO2 interface. Because of this high electric field electron and hole gain sufficient energy to cross interface potential barrier and enter oxide layer. This effect is called as hot carrier injection. To reduce Vth oxide thickness is reduced which increase field across oxide. This results in hot carrier injection resulting in gate oxide tunneling current. Gate induced leakage increase with channel doping.

3.5 Gate induced drain leakage

This is due to high electric field between gate and drain and is noticed in accumulation region. Consider an NMOS device which is biased at supply voltage (Vdd) and gate at negative or zero bias, a depletion region is formed in gate and drain. To produce band bending more than silicon gap VDG should be large enough.

3.6 Channel punch through current

The amount of punch through current depends on potential distribution under channel. If depletion region under drain region is extended towards source region, the potential barrier

between source and drain will be lowered and carriers will start to move from source to drain.

4. LOW POWER DESIGN TECHNIQUES

Power dissipation could be minimized at three levels device level, logic level and circuit level.

Table 1. Low Power Design techniques at various levels

Device level	Logic level	Circuit level
Retrograde/halo doping	PTL logic realization	Stacking
Oxide thickness	GDI logic realization	Power gating
Steep transistor	Adiabatic logic realization	Multi threshold
	Using sleep transistors	Dynamic threshold

The different power minimization techniques at circuit level are discussed as below:

4.1 Stacking

Stacking is replacing a single transistor with two transistors of half of its size. This technique can also be called self-reverse bias technique because the leakage current basically depends on the threshold voltage and stacking is the way of dynamically controlling threshold voltage by providing self-reverse bias. Threshold voltage of a MOSFET is given by and it clearly depends upon VT0 i.e. threshold voltage at zero substrate bias, Vsb-source-to-body substrate bias, and 2Φf, the surface potential [6].

$$V_t = V_{t0} + \gamma\left\{\left(\left|V_{sb} + 2\Phi_f\right|\right)^{1/2} - \left(\left|2\Phi_f\right|\right)^{1/2}\right\}$$

Also from equation of subthreshold leakage current it is clear that current in subthreshold region depends exponentially on the voltage on four terminals of MOSFET. When more than two transistors in stack are turned off, a positive voltage at the node between two transistors is developed, this developed positive voltage has following three effects

Due to the positive source potential, VM gate-to-source voltage of 1st transistor in stack becomes negative; hence, the sub threshold current reduces substantially.

Due to VM>0, body-to-source potential of 1st transistor in stack becomes negative, resulting in an increase in the threshold voltage (larger body effect) of mentioned transistor, and thus reducing the sub threshold leakage.

Due to VM>0 , the drain to source potential of transistor in stack decreases, resulting in an increase in the threshold voltage (less DIBL) of , and thus reducing the sub threshold leakage.

4.2 Multi threshold CMOS technique

Multi threshold implies the use of transistor in circuit with multiple threshold voltages. So that the low Vth transistor could manage the proper performance and at the same time high Vth part of circuit could bring down the leakage current. This method can be used in VLS circuit in two ways. Firstly transistors in critical path of circuit can be replaced with low threshold transistor and all the other transistors are of high threshold voltage. .i.e. this method involves analysis of different sections for delays to find out the critical path. After being known about delays and hence the critical path, the placement as per threshold of transistor is done. The major advantage of this method is that the performance and leakage power minimization are achieved simultaneously [7].

Secondly this is popularly used with power gating technique. Power gating circuitry used high threshold transistor and the circuit is maintained at low threshold. Using power gating incorporated with multi threshold makes power gating technique even more efficient. The computational unit that is circuit is designed with low threshold to provide high performance operation. And the high threshold power gated transistor is sufficient for power reduction.

If using multi threshold CMOS with power gating (consider sleep transistor) only one of the two i.e. footer and header is sufficient to minimize power. NMOS insertion is preferred over PMOS insertion since size of NMOS is small than that of PMOS.

4.3 Power gating technique

Power gating is isolating supply or ground or both from main circuit. This is method of introducing an additional circuitry between supply and circuit or circuit and ground. There are many power gating technique such as single mode power gating or sleep transistor technique, sleepy keeper power gating, sleepy stack power gating, diode connected sleepy stack, tri-mode power gating, multiple threshold CMOS technique, multiple sleep mode power gating, hybrid multiple mode power gating etc. [8].

4.3. 1 Sleep transistor technique

Basically it is a power gating technique in which additional transistor of high threshold voltage are placed as header and footer. These transistors are called sleep transistors. When this method is applied to the circuit a signal (called sleep signal) is given to the circuit when circuit reaches static state. In practical application this sleep signal is given externally by some hardware. Such circuits operate in two modes i.e. dynamic and static mode [9]. This method reduces power by creating a virtual power supply.

4.3. 2 Sleepy stack:

This method is combination of sleep transistor and stacking technique as it introduces sleep transistor in parallel to stack transistor. Since sleep transistor is on only during active operation mode whereas stacked transistor placed in parallel are always kept on thus switching speed is improved considerably and also low power can be achieved as already known from stacking and sleep transistor method.

In this method the sleep PMOS and sleep NMOS are placed parallel to pull up and pull down network respectively. The sleep transistors action is same as in sleep transistor technique. To get faster switching time than stack approach in active mode the sleep transistors are always on so there is continuous current flow in the circuit.

4.3. 3 Diode connected sleepy stack:

In this method NMOS is stacked and one of the two MOSes is connected as diode that is gate is shorted with drain. When both the transistors are off the stacking effect reduces the power. For the transistor connected as diode Vds=Vgs from equation (11) drain current related to Vds in quadratic manner. So as the Vds will drop Id will also be reduced in quadratic manner.

$$I_d = \mu C_{ox} W/L \left((V_{gs} - V_t)V_{ds} - V_{ds}^2/2\right) \quad (11)$$

4.3. 4 Variable body biasing for real time threshold voltage

Variable body biasing can be used to change threshold voltage in real time. In normal operation substrate of transistor is connected to source and in standby mode substrate potential is kept positive for PMOS while negative for NMOS. This method overcomes the drawbacks of multi threshold voltage method as all transistor used are of same threshold just their threshold is varied in real time as per the requirement [10].

5. SIMULATION RESULTS

All the above methods are applied on ISCAS 85 74283 and net list for the circuit is written and simulated using HSPICE simulator. Various parameters and their impact on circuit designs are studied. The analysis is done at 1V, Vdd and 270C.

Conventional circuit is designed using CMOS logic at 32nm technology. In forced stacking technique, all the transistor in circuit are replaced by stacked transistors and the Power in stacking is reduced by 56.29% but at the same time delay is increased by 96.6%. Sleep transistor technique make use of only two additional transistors operating according to mode of operation of circuit. Static power is reduced because the path of rail connecting Vdd to ground is cut.

Table 2. Comparison of various methods

Method	Parameters	
	Static power	Delay
Conventional	5.0419E-06	4.0171E-11
Force Stacked transistor	2.1535E-06	1.3303E-10
Sleepy transistor	5.0829E-09	5.0992E-13
Multi-threshold transistor	3.9260E-09	4.3315E-13
Dual mode stacked power gating	2.8094E-09	5.5199E-13
Variable Vth	7.2850E-11	6.7279E-13

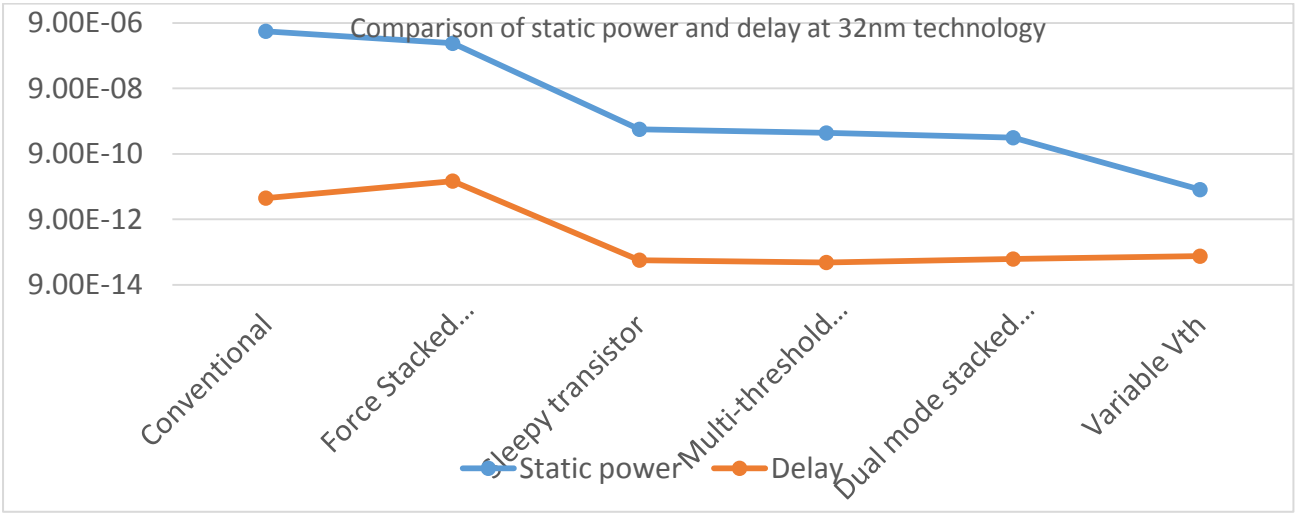

Figure 3. Comparison of static power and delay at 32nm

Compared to normal sleep transistor method Dual threshold sleep transistor or multi threshold power is reduced by 23% and delay is also reduced by 15%. In Dual mode stacked power gating 45% power is reduced and compared to stacking the delay is reduced considerably. In variable threshold the threshold voltage of sleep transistor is varied according to mode of operation. In static mode of operation the threshold voltage of power gated MOS is increased by applying body bias to the transistor. Power is reduced considerably compared to fixed Vth method.

6. CONCLUSION AND FUTURE SCOPE

One of the biggest concerns of electronics industry is power dissipation. It has been reviewed from work of various researchers that by merging advantages of any two or more conventional concepts of power minimization like sacking, power gating and multi threshold new power minimization methods can be evolved.

Newer methods have been developed for better performance utilizing the advantages of existing techniques. Like sleepy stack method utilizes the advantages of stacking and sleep transistor and the new method comes out to be a perfect integration of advantage of two methods. In same manner many other methods can also be developed with some trade-offs to minimize leakage power.

Study and analysis of applying various power minimization techniques reveals that although each of the method works well for circuits with small number of transistors but for circuits like CLA or combinational circuit with large number of sub circuits, the performance is degraded.

Thus in future rather than applying method on entire circuit, methods can be applied module wise to minimize power. Method such as stacking that increases delay when applied to entire circuit causes glitches as delay in various paths is different so stacking is applied in final module adder.

Also hybrid circuits can be developed that utilizes advantages of two logic styles. Complete CLA is applied with power gating of sleep transistor to make it operate in dual mode.

Also dynamic Vdd is applied to circuit. From equation (9) sub-threshold leakage depends on Vgs- ηVds value of η is greater than zero for MOSFET thus this difference reduces causing considerable reduction in sub threshold leakage current.

7. REFERENCE

[1] Wolfgang Arden, Michel Brillouet, partrick Graef, Bert Huizing, Reinhard Mahnkoph, "More than Moore, White Paper," Semiconductor Industry Association, Update 2012. [Online]. Available: http://www.itrs.net/Links/2010ITRS/IRC-ITRS-MtM-v2%203.pdf.

[2] "International Technology Roadmap for Semiconductors,," Semiconductor Industry Assoc., 2013. [Online]. Available: http://public.itrs.net.

[3] M. Hansen, H. Yalcin, and J. P. Hayes,, "Unveiling the ISCAS-85 Benchmarks: A Case Study in Reverse Engineering,," IEEE Design and Test,, Vols. 16, no. 3, pp. 72-80, July-Sept 1999.

[4] kausik roy, saibal mukhopadhyay hamid mahmoodi-meimand, "leakage current mechanism and leakage reduction techniques in deep submicrometer CMOS circuits," proceedings of IEEE, vol. 91, february 2003.

[5] Nam Sung Kim, Todd Austin, David Blaauv and Trevor Mudge, Leakage Current: Moore's Law Meets Static Power, IEEE Computer Society, December 2003.

[6] Mark c Johnson, Dinesh Somasekar, Lin Yin Chou, Kausik Roy , "Leakage control with efficient use of transistor stack in single threshold CMOS," in Proceeding of 36th annual IEEE Design automation Conference, 2002.

[7] S. Shigemastu, S. mutoh Y. matsua,J. yamada, "1V high speed MTCMOS circuit scheme for power down application," in IEEE Journal of Solid State Circuits, 1995.

[8] Se Hun Kim, Vincent J. Mooney, "sleepy keeper- a new appproach to low leakage power VLSI Design," in International Conference onVery Large Scale Integration, IEEE 2006.

[9] Kaijian Shi, David Howard, "Sleep Transistor Design and Implementation – Simple Concepts Yet Challenges," 2007. [Online]. Available: http://blogs.synopsys.com.

[10] T. Sakurai, "Reducing power consumption of CMOS VLSI's through VDD and VTH control," quality electonic design,2000. ISQED 2000. proceedings. IEEE 2000 firstenational symposium, pp. 417-423, 2000.