Comparative Analysis of Delay and Variability of D Flip-Flops

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ABSTRACT
Low power device design has become a significant field of research due to increase used of portable devices. In this paper, various D flip-flop topologies have been scrutinized for estimation of propagation delay (t_p) and power dissipation (P_{dis}) and delay variability for portable applications. High level triggered D flip-flops have been considered for analysis. Today's electronic devices require high speed design feature with minimum power dissipation. Design for variability has become vital as relative level of parameter and device variability has been increasing with device density scaling. In this paper, delay variability of the flip-flops has been investigated at 16-nanometer CMOS process on SPICE.

Keywords
Delay variability, Energy-Delay tradeoff, Flip-flops, Differential logic families

1. INTRODUCTION
Evolution in VLSI designs has offered the development of several compact devices. Such devices need high speed as well as low power consumption and therefore the estimation of propagation delay and power dissipation plays a very important role in designing of the portable devices [1]. Among the various building blocks of the digital design, the flip-flop design is the most power consuming and complicated. Around 30%-60% of the total system power is consumed in the clocking networks and the flip-flops. Various D-flip flops circuits have been discussed so far in the literature but require more number of transistors thereby enlarging the area.

Data storage elements or Flip-Flops are indispensable timing components in every digital circuit. Edge-triggered flip-flops are required in designing synchronous counters, registers, specifically in deeper pipelined designs. The most commonly used flip-flop is D flip-flop. A D flip-flop holds the value of D input at particular predefined level of clock pulse (high or low level) if the flip-flop is level triggered or a particular portion of the clock pulse (rising or falling edge) if the flip-flop is edge-triggered without affecting the output at any other instance of the clock pulse.

CMOS (Complementary Metal Oxide Semiconductor) technology has faced radical scaling during the last four decades for achieving higher integration density, higher speed of operation and lower power dissipation. The supply voltage (V_{DD}) has also been scaled down to minimize the power dissipation and maintain device reliability (to prevent oxide breakdown). The performance of the CMOS circuit relies upon the propagation delay (t_p) and the propagation delay further depends on threshold voltage, and supply voltage.

One of the major obstacles to the CMOS circuits in nano-scale regime is variability. As it is well known, the threshold voltage of MOSFET is given by

$$V_t = V_{t0} + \gamma\left(\sqrt{2|\varphi_F| + V_{SB}} - \sqrt{2|\varphi_F|}\right) \quad (1)$$

where V_{t0} is the threshold voltage at V_{SB} = 0 V and is mostly a function of the manufacturing process, difference in work-function between gate and substrate material, oxide thickness, Fermi voltage, charge of impurities trapped at the surface, dosage of implanted ions, etc; V_{SB} is the source-bulk voltage; $\phi_F = V_T\, ln(N_A/n_i)$ is the bulk Fermi potential (where $V_T = kT/q$ = 26 mV at 300 K is the thermal voltage, N_A is the acceptor doping concentration, n_i is the intrinsic carrier concentration in pure silicon); $\gamma = \sqrt{(2qN_A\varepsilon_{si})}/C_{ox}$ is the body-effect coefficient (where ε_{si} is the relative permittivity of silicon, C_{ox} is the gate oxide capacitance).

This equation is suitable for predicting the threshold voltage for ultralong-channel devices (> 1 μm). It fails to model threshold voltage of nano-scaled devices. To model threshold voltage for nano-scaled devices, many factors are to be considered such as short-channel effect (SCE), narrow-width effect (NWE), DIBL (drain induced barrier lowering), reverse short-channel effect (RSCE) etc. In short-channel devices, the depletion region around the drain increases as V_{DS} increases and it penetrates deep into the middle of channel region, which lowers the potential barrier between the source and drain and shifts the point of maximum barrier toward the source end causing a substantial decrease in threshold voltage. The DIBL effect can be modeled as

$$V_t = V_{t0} - \eta_{DIBL} V_{DS} \quad (2)$$

where V_{t0} is the threshold voltage at V_{DS} = 0 V, and η_{DIBL} is the DIBL coefficient.

Since variability is a big issue in nano-scale regime, this paper performs variability analysis of D flip-flop circuits based on different CMOS logic families and remarks about the robustness of logic family. The considered logic families are CVSL (Cascode voltage switch logic), CPL (Complementary pass gate logic), SCMOS (Static CMOS logic), Pseudo NMOS (n-channel MOSFET) logic and Depletion NMOS logic.

2. SIMULATION SET-UP AND DEVICE SIZING
In this paper, several design specifications such as P_{dis} (power dissipation), and t_p (propagation delay) of D flip-flop circuits designed with several CMOS single ended and differential logic families are evaluated. The ITRS (International Technology Roadmap for Semiconductors) considers an acceptable ±10 % variation in device specifications (L, W, N_{DEP}, t_{ox}, V_t, μ_0) [2]. In order to achieve better correctness,

5000 cases of Monte-carlo simulations are carried out by altering device specifications. Each case sets-up a distinct SPICE (Simulation Program with Integrated Circuit Emphasis) model file for each case of specifications at 16-nanometer CMOS process. All simulations are performed at a supply voltage of 0.7 V@ 1 Hz frequency using predictive technology model (PTM) [3]. The listed specifications are estimated with independent Gaussian distributions with a 3σ variation of 10% [4].

3. ANALYSIS OF CMOS LOGIC FAMILIES

3.1 Cascode Voltage Switch Logic (CVSL)

CVSL is a differential logic family. The benefit of differential CMOS logic family is that both complementary output and actual output can be evaluated concurrently without needing an extra inverter. The time-differential problems which are introduced by the use of additional inverters are nullified by this approach. In CVSL logic (see Fig. 1), differential pair are cascaded to achieve the desired function. Here two pull-down networks, PDN_1 and PDN_2 employ N-MOSFETs. Both PDN_1 and PDN_2 conduct exclusively i.e. when is PDN_1 on, PDN_2 is off and when is PDN_1 off, PDN_2 is on. The basic working of CVSL logic includes two principles: positive feedback logic and differential logic. In differential logic, input is provided in both true and complementary signals and consequently both the true and complementary outputs are obtained (dual rail logic).

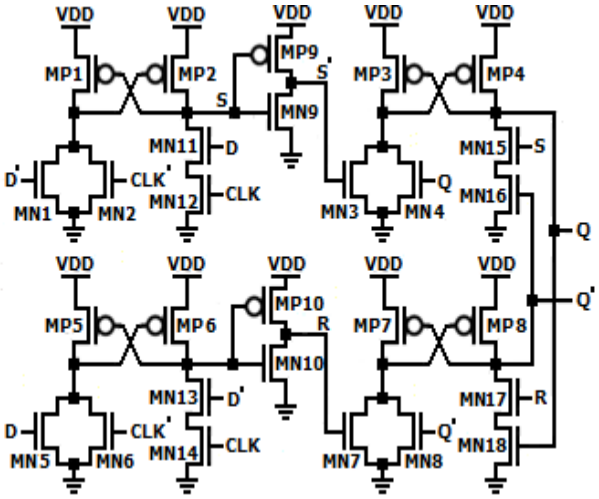

Fig 1: D flip-flop implementation using CVSL technology.

3.2 Complementary Pass Transistor Logic (CPL)

Contrary to CVSL differential logic, in CPL logic, the one half of the gate pulls up and the other half pulls down (Fig. 2). The cross-coupled connection of pull-up P-MOSFETS offers fast differential stage and very good driving capability. CPL logic has better delay variability than CVSL logic but it has worse device counts and power dissipation. Among all differential logic families, CPL logic has the highest robustness and least delay variability. The disadvantage is, the CPL logic needs all inputs and their complements which increases the routing complexity and the large overhead structure. [6][7].

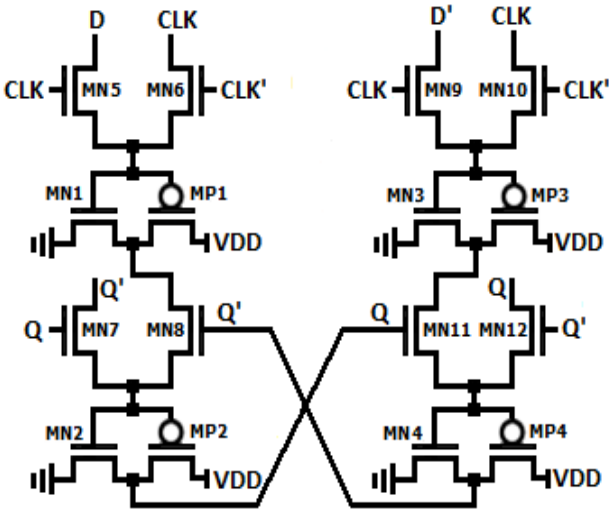

Fig 2: D flip-flop implementation using CPL technology.

3.3 Static CMOS (SCMOS)

Static CMOS is a single-ended logic family. In Static-CMOS, each logic stage contains pull-up networks (PUNs) and pull-down networks (PDNs) and is controlled by input signals. As shown in Fig. 3, the PUNs comprise P-MOSFET and PDNs comprise N-MOSFET. These two networks, connected in between the power lines and the gate output can be used to realize any logic function.

The main advantage of SCMOS is ratio-less logic design (minimum transistor sizes) and its robustness against transistor sizing and voltage scaling. Hence, these circuits can be operated reliably at low voltages. SCMOS design consumes no static power because the PDNs and PUNs do not conduct simultaneously. Table I shows that lowest power dissipation is achieved in SCMOS logic. The only problem of SCMOS logic design is the requirement of more count of wide P-MOSFET in PUNs, which results in high load at the input terminals [8],[9].

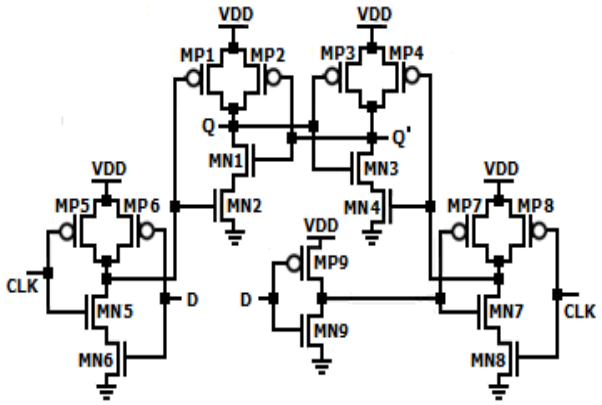

Fig 3: D flip-flop implementation using SCMOS technology

3.4 Pseudo-NMOS logic

In Pseudo NMOS logic (see Fig. 4.), the pull-up network consists of a single P-MOSFET which is always kept on by keeping its gate terminal grounded. The pull-down network is similar to the Static-CMOS logic. This circuit has higher speed compared to SCMOS logic due to less number of pull-up transistors (less load capacitance on input signals) but it

offers higher noise margin and significant static power dissipation because the pull-up is always on [1],[8].

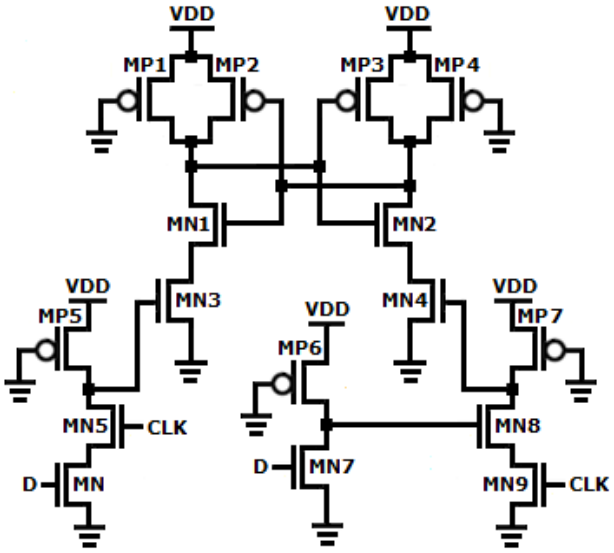

Fig 4: D flip-flop implementation using Pseudo-NMOS technology

3.5 Depletion-Load NMOS Logic

Fig. 5 shows the D flip-flop implementation using Depletion-load NMOS technology. In this logic, only NMOS transistors are used to create logic circuits [8]. The depletion load is used as pull-up network in this logic. Depletion mode NMOS allow single voltage operation and are able to achieve great speeds. The advantages of depletion mode are higher circuit density, significantly less power and analog and digital circuits can be made side by side on the same chip.

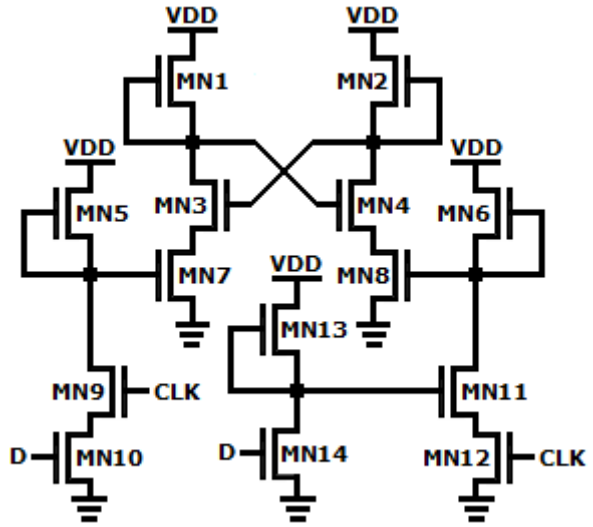

Fig 5: D flip-flop implementation using Depletion-Load NMOS technology

4. RESULTS AND DISCUSSION

This section presents simulation results of various design metrics which are measured during simulation on HSPICE using 16-nanometer CMOS process. Monte Carlo simulations are performed for the measurements. During Monte Carlo simulation, process parameters such as L (channel length), W (width), t_{ox} (oxide thickness), μ_0 (zero bias carrier mobility) and R (sheet resistance of source/drain diffusion) are varied by ±10% with Gaussian distribution. Simulation measurements are taken for both the designs applying variation. Monte Carlo simulation is a method for iteratively evaluating a design. The goal is to determine how random variation on process parameters, voltage and temperature affects the performance and reliability of a design. As the Std. Dev. (standard deviation) is a measure of dispersion (or variability) that states numerically the extent to which individual observations vary on an average, it is used as a measure of variation in cell parameters.

D-flip flops are characterized by design metrics such as propagation delay (t_p) and power dissipation (P_{dis}). The propagation delay is given by

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} \quad (3)$$

where t_{pHL} and t_{pLH} are the high-to-low and low-to-high transition time respectively.

Metrics like mean delay (μ), its standard deviation (σ), variability (σ /μ), and power dissipation (P_{dis}) have been evaluated and listed in Table 1. By comparing all CMOS families, the power dissipated by SCMOS is the lowest as it consumes negligible static power. It shows higher delay variability compared to CPL logic. Pseudo-nMOS logic consumes the maximum power as its pull-up network is always on but has least delay. CVSL has both higher variability and power dissipation. Among all logic families, CPL logic provides the optimum performance as it has the least variability.

Table 1. Comparison among CMOS Differential Logic gates

Logic Family	Standard deviation of propagation delay (σ)(s)	Mean of propagation delay (μ)(s)	Variability (σ/μ) (a.u.)	P_{dis} (nW)
CVSL	3.762e-1	2.534e-1	1.484	61.62
CPL	1.702e-1	2.535	0.067	38.27
SCMOS	4.457e-1	1.727e-1	2.580	20.03
Pseudo-nMOS	1.937e-1	2.938e-2	65.929	2547
Depletion	2.580e-1	1.818e-1	4.483	311.9

5. CONCLUSION

In this paper, several differential and single-ended CMOS logic families (CVSL, CPL, SCMOS. Pseudo NMOS and Depletion-mode) have been evaluated using D flip-flops. CVSL logic style offers potential speed advantage as all the operations are performed with N-MOSFETs, thus reducing the input capacitance. In CPL logic style, only half of the gate pulls up and the other half pulls down thereby resulting in lowest delay variability than all other logic styles. SCMOS logic style provides the lowest power consumption among all logic styles and is also robust against voltage and device dimension variations. Pseudo NMOS logic family performs poorly in terms of power dissipation as the pull-up network is always kept on. The advantages of depletion mode are higher circuit density, significantly less power and analog and digital circuits can be made side by side on the same chip. By

comparing various logical gates, D flip-flop realized using CPL logic is the most ideal one because it provides longer delay, lower variability, and moderate power dissipation. CPL logic style is suitable for low power and high performance applications. These circuits can be employed for designing several complex memory and sequential circuits. Future scope of this works is to estimate power-delay product (PDP) and energy-delay product (EDP). Variability estimation of power dissipation, PDP and EDP can be performed as future work to identify the robust logic family in terms of these parameters.

6. REFERENCES

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