Ultra Wideband Low Noise Amplifier Design and Optimization for Next Generation RF Receiver using 0.18µm CMOS

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ABSTRACT
In 2002 Federal Communication Committee (FCC) has released an unlicensed 3.1 - 10.6 GHz Ultra Wideband (UWB) for commercial applications. The UWB technology has desirable features such as accurate timing in range resolution, less multi path fading, high data rate transmission and easier material penetration due to 7.5 GHz wideband. The FCC has put restriction on transmission power (EIPR must less than -41.3 dBm/MHz) and bandwidth (not less than 500 MHz) for UWB use in commercial applications. UWB receiver require high power gain, low noise figure and wideband matching due to FCC restriction on transmission power. The most critical part to design in UWB receiver is Low Noise Amplifier (LNA). The designing of LNA for UWB receiver is still challenging task.

In this paper proposed multistage LNA topology for UWB receiver. The proposed LNA topology has Common Gate (CG) in first stage for wideband matching. The proposed LNA achieved more than 20 dB power gain, average 3.3 dB noise figure and good input matching (S_{11}<-9 dB) in wideband (3.1 – 10.6 GHz), while consuming total 19 mA current from 1.8V supply including bias circuit current. The LNA design achieved good linearity, average IIP3 is -5.5 dBm by proper biasing of the all amplifier stages. The standard 0.18µm CMOS technology is used to design the LNA.

Keywords
CMOS, LNA, Next Generation, Radio Frequency, Frontend, UWB

1. INTRODUCTION
UWB system has opened new frontier for wireless communication users due to extremely wide bandwidth. UWB is widely used in high data rate wireless communication, penetration imaging and high accuracy locating applications.

Despite of all the favourable features and applications of the UWB technology, still serious challenges exist to implementation 3.1-10.6 GHz ultra wideband receiver. UWB received signal has weak in amplitude due to FCC's restriction in transmitted power and another additional path loss. UWB receiver necessitate high power gain, low noise figure and good impedance match wideband for to process received wideband weak signal. Overall performance of the receiver decide by the First block of receiver, Low Noise Amplifier (LNA).

1.1 Performance Parameters of LNA
1) Noise Figure (NF)
2) Power Gain (S_{21}) and Input matching (S_{11})
3) Linearity (IIP3)
4) Power consumption
5) Stability

1.1.1 Noise Figure
The Noise performance of two port network is measure using Noise Factor (F). The signal to noise ratio (SNR) is define as ration of signal to noise power. The noise factor is define as the ratio of input signal SNR to output signal SNR. If the Noise Factor is expressed in decibels it is called the Noise Figure (NF).

$$\mathrm{SNR} = \frac{\mathrm{P_{signal}}}{\mathrm{P_{noise}}} \quad (1)$$

$$\mathrm{F} = \frac{{}^{\mathrm{P_{si}}}/_{\mathrm{P_{ni}}}}{{}^{\mathrm{P_{so}}}/_{\mathrm{P_{no}}}} \quad (2)$$

$$NF = 10\log(F) \quad (3)$$

A Low Noise Amplifier (LNA) is the first amplifier stage of a receiver. Overall noise figure of the multistage amplifier receiver is express as

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + .. + \frac{NF_m - 1}{A_{p1} \ldots A_{p(m-1)}} \quad (4)$$

Equation (4) is also known as friis formula which is named after the Danish-American electrical engineer Harald T. Friis. Total receiver noise figure is dominated by the first few stages, especially the very first stage (namely the LNA). This is the reasoning behind why the first stage amplifier should have low noise figure as possible.

1.1.2 Power gain and input matching
Other design performance parameter of the LNA is Power gain (S_{21}).The power gain of LNA should have as high as possible to increase strength of weak received signals from antenna. Input impedance matching in design is another important parameter to maximize power transfer from antenna to amplifier. Reflection coefficient (S_{11}) measure the quality of the input impedance matching.S_{11} defines as the ratio of reflected signal power to incident signal power at input of amplifier. The magnitude of S_{11} normally expressed in decibel (dB) unit and the perfect input impedance matching system have S_{11} is -∞. It is desired to have value of S_{11} as low as possible.

1.1.3 Linearity
In the LNA design linearity is another importance parameter has to be considered when weak input signal with strong interfering signal. Due to Strong interference signals in poor

linear design produce cross modulation and blocking undesired inter modulation distortion.

1 dB compression point (P1dB) and third order intercept (IIP3) are uses to measure linearity of system. IP3 shows at what power level the third order intermodulation product is equal to the first order output power. Third orders input intercept point (IIP3) and output intercept point (OIP3) are the input power and output power respectively at IP3. P1dB defines as input power level when output power drops 1 dB from its theoretical linear value. IIP3 and P1dB have an approximation relation IIP3=P1dBm+10dBm. By knowing one other can be finding using this relationship.

1.1.4 Power consumption

For battery operated device design power consumption is very importance design parameter. Low power dissipation design is not only increase battery life but also decrease cost of cooling system and allow increase complexity of chip to incorporate more functionality.

1.1.5 Stability

In feedback amplifier certain combination values of input and output impedance make amplifier unstable. The stability factor in terms of S parameter is define as

$$K = \frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{21}||S_{12}|} \quad (5)$$

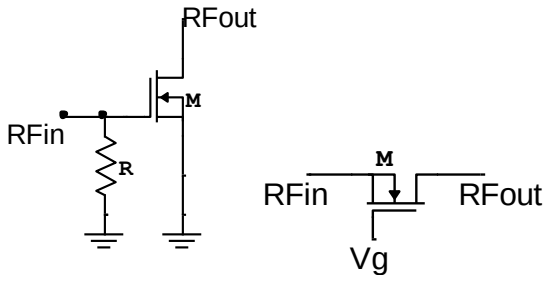
Where, Δ is determinant of S parameter matrix. Value of K greater than unity and value of Δ less unity make system unconditionally stable.

As we can see, the design of an LNA is a multi-dimensional optimization problem. There are lots of trade-offs involved because the optimization of each individual specification does not arrive at the same sizing or biasing solution. This requires that the designer consider what is the best combination of performance specifications for the intended application of the LNA.

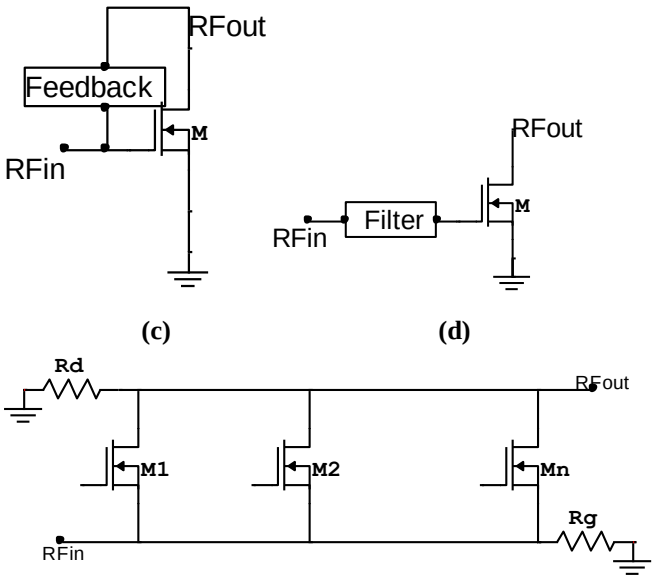
In this research work authors have designed and optimized UWB high power gain LNA for UWB RF frontend receiver. In Section 2 of this paper discuses literature survey of wideband LNA and in section 3 describe proposed high power gain UWB LNA analysis, designing and optimization. Section 4 has simulation results discussion and comparison with published work. In section 5, 6 and 7 have conclusion, acknowledgement and references respectively.

2. LITERATURE REVIEW

Various LNA topologies have been used in the literature to achieve wideband input matching. Reported topologies in open literature are (a) common source with resistive termination, (b) common gate, (c) Feedback, (d) input filter and (e) distributed as shown in fig.1.



(a) **(b)**



(c) **(d)**

(e)

Fig. 1 Wideband LNA topologies a) resistive termination, b) common gate, c) feedback, d)filter and e) distributed

2.1 Common source with resistive termination LNA topology

Researcher achieves wideband impedance matching by the adding a 50Ω shunt resistor at the input of common source LNA [1] as shown in fig. 1(a). This topology has tradeoff between Noise Figure (NF) and input impedance matching. Resistive termination topology attenuates signal and add thermal noise due to shunt resistor. Minimum NF achieve in this topology is [1]:

$$F \geq 2 + 4(\gamma/\alpha)(\frac{1}{g_m R}) \quad (6)$$

Where, γ is a noise parameter and α is the ratio of transistor's transconductance (g_m) to drain-source conductance (g_{ds}) at zero bias and R is shunt resistor value.

2.2 Common Gate (CG) Topology

The CG provides wideband input impedance matching and input impedance express as shown in eq. (7) [2].

$$Z_{in} = 1/(g_m + g_{mb}) \quad (7)$$

Where, Z_{in} is the input impedance, g_m and g_{mb} are transconductance of the input and cascode transistors respectively. Major drawbacks of this topology are its higher NF, low gain and high power consumption. The NF of a CG transistor can be express as:

$$NF = 10 \log (1 + \frac{\gamma}{\alpha R_s g_m}) \quad (8)$$

Where, γ is a noise parameter and α is the ratio of transistor's transconductance (g_m) to drain-source conductance (g_{ds}) at zero bias, R_s is the source resistance, $g_m$is the trasconductance of transistor. The NF in CG topology is enhanced by increasing $g_m$but it degrades input impedance matching. Here is the tradeoff between NF and matching of CG topology. Generally feedbacks techniques are used with CG topology to relax tradeoff.

2.3 Feedback LNA topology

The tradeoff between NF and input impedance matching in common gate topology can be broken through the use of various negative feedback in common source as shown in fig. 2. Lossless transformer as a feedback offers best performance

but it require larger silicon area. Therefore, a feedback including a resistor, resistor–capacitor [3], reactive element or transistor is a more proficient solution to break this tradeoff. Feedbacks provide wideband input matching without reducing the signal as in common source with resistive termination.

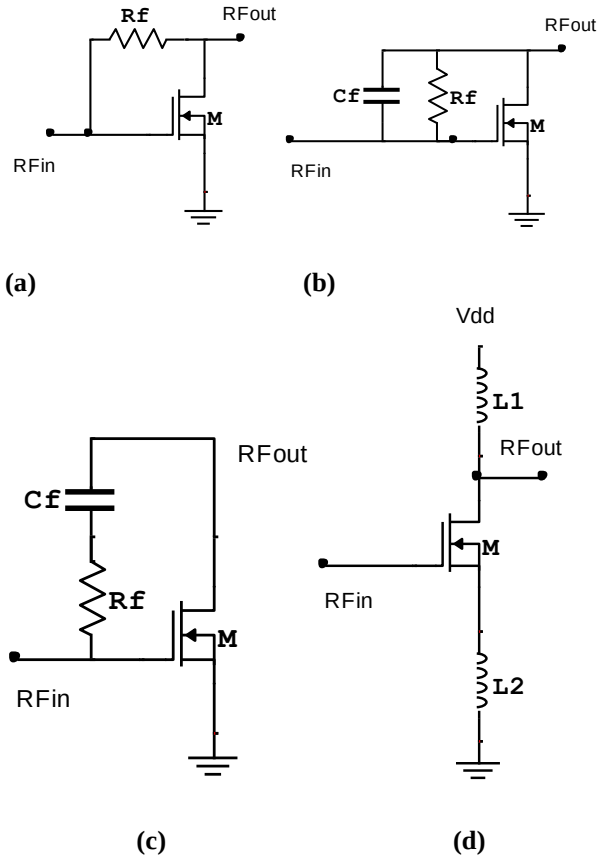


Fig. 2 Feedback topologies a) resistive b) series RC c) parallel RC and d) transformer.

2.4 Filter LNA topology

The band pass filter is used at input of LNA which resonant at entire band to provide wideband matching [4]. This LNA topology has good performance while dissipating low power but it requires large value of inductors and to fabricate inductors require larger silicon area. Various types of filters have used in literature like dual RLC, LC, Chebyshev, three-section band pass, Miller effect input matching filter [5], a π-matching LC filter [6], high pass filter [7] and transformer based input matching network to wideband LNA design.

This topology is implemented with CS inductive degeneration stage to achieve good NF, Low power consumption, high gain and wideband input matching [4]. Due to larger value of inductors in filter require off chip components.

2.5 Distributed topology

The schematic of Distributed Amplifier (DA) is shown in fig. 1(e). In DA topology is used parallel transistors with inductors to achieve wide input matching by reducing parasitic capacitance [8], while this topology require larger silicon area and consuming more power.The DA provides wideband flat gain, wideband matching and good linearity but having inherently poor NF [8].

The high power consumption in DA can be reduced by using current reuse or low voltage technique. Various NF improvement techniques used in DAs to improve NF performance. In some DA replaces resistive termination with resistive-inductive network to reduce the noise generated by the terminating resistor but it requires dual power supply, consuming more power and degrade input matching.

Due to need for high Q inductors or transmission lines require larger silicon area and high power consumption make DAs less gorgeous for compact and portable receivers. DAs have vast applications in medical imaging and high frequency instrumentation [9] due to wideband.

Frist and most importance in UWB receiver is require wideband matching for maximum power transfer from antenna output to input of the LNA. Among the reported wideband matching topologies CG has inherent wideband matching property and it's widely used in wideband matching design. In the proposed UWB LNA design used CG for wideband matching.

3. HIGH POWER GAIN ULTRA WIDEBAND LNA DESIGN AND OPTIMIZATION

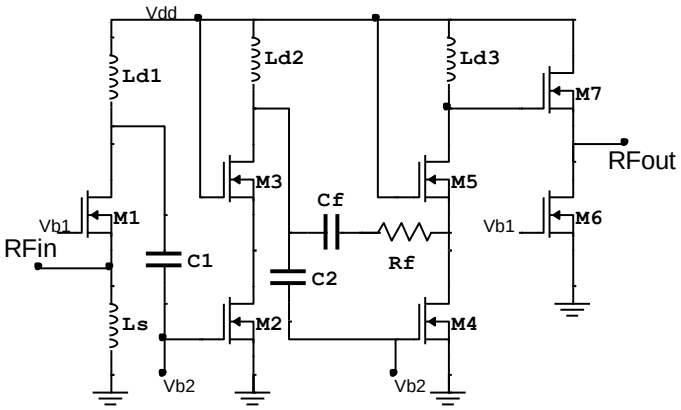


Fig. 3 Schematic of proposed UWB LNA

3.1 Circuit description

Fig. 3 demonstrates the schematic of proposed LNA. The LNA consist four cascaded amplifier stages. First stage of the LNA is common gate for wideband input matching. The inductor connected between the source of the M_1 and ground form LC tune circuit with C_{gs1}.The values of L_s and C_{gs1} select such that it resonant at centre frequency of interested band which provides good impedance matching. The design gain is improved by using cascode common source (CS) amplifier stages. Last stage in the LNA is Common Drain (CD) for to drive high capacitive load of the next stage.

The large value capacitor between the M_1 gate and ground ensures better AC grounding and also bypasses the biasing circuit noise. The noise figure of the design is improved by using inductive load in each stage instead of commonly used resistive load in wideband LNA design. The first stage load inductor (L_{d1}) must be chosen such that it will resonate with $C_{d1} + C_{gs2}$ around the center frequency of interested band.All the load inductors form LC tune circuit with next stage input capacitance. Wideband flat gain achieves by designing such that each tune circuit resonate at different frequencies.

The design use cascode transistor to reduce miller effect and the cascode transistor also improve gain and reverse isolation without consuming extra power.

3.2 Input and output impedance analysis

The input impedance of the proposed LNA is nothing but the input impedance of common gate first stage.

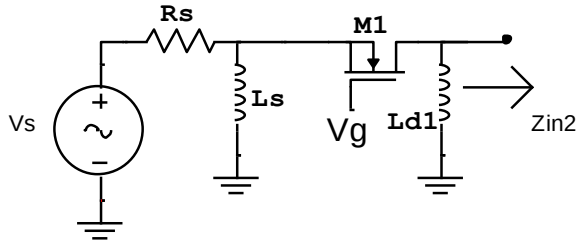


Fig. 4. Common gatefirst stage

AC equivalent circuit of the common gate first stage is shown in fig. 5.

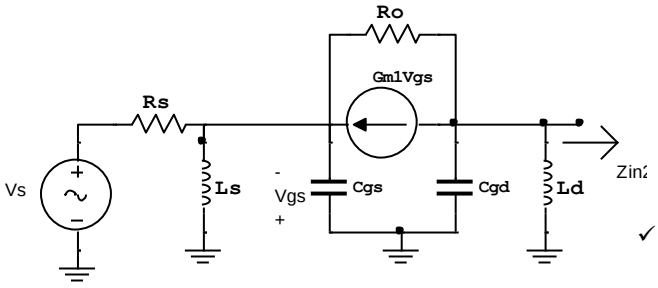


Fig. 5. AC equivalent circuit of CG

The input impedance is find by applying KCL at input node and it is expresses as

$$Z_{in} = \frac{1}{g_{m1}+\frac{1}{Z_S(\omega)}+\frac{1-G_{m1}Z_O(\omega)}{R_O+Z_O(\omega)}} \quad (9)$$

Where, $Z_s(\omega) = j\omega L_s // \frac{1}{j\omega C_{gs}}$ and

$$Z_o(\omega) = \frac{1}{j\omega C_{gd}} // j\omega L_d // Z_{in2}$$

Assume that $Z_s(\omega)$ and $Z_o(\omega)$ are having high Q inductor and capacitor, so it represent using only imaginary part $Z_s(\omega) = jX_s(\omega)$and $Z_o(\omega) = jX_o(\omega)$.Substituting thesevalues of $Z_s(\omega)$ and $Z_o(\omega)$in eq. (9) and simplified by neglecting $G_{m1}R_oX_o(\omega)$ and $G_{m1}X_o^2(\omega)$ compare to $R_o^2 + X_o^2(\omega)Z_{in}$ expressed as below

$$Z_{in} = \frac{1}{\left(G_{m1}-\frac{R_O}{R_O^2+X_O^2(\omega)}\right)-j\left(\frac{1}{X_S(\omega)}\right)} \quad (10)$$

$G_{m1}$is should be set slightly greater than 20ms for better matching due to effect of output resistor (R_o).

For good input matching over the wideband L_s and C_{gs1} should be selected such that they resonate at the center frequency leaving only 50Ω real impedance.

Last stage source follower output impedance is express as

$$Z_{out}(\omega) = \frac{1+j\omega Z_3(\omega).C_{gs6}}{g_{m6}+j\omega C_{gs6}} //r_{06}//r_{07} \quad (11)$$

Where, g_{m6} is transconductance of source follower transistor, $Z_3(\omega)$ is the third stage output impedance and forth stage input impedance, C_{gs6} is the gate of source capacitance of the source follower transistor, r_{06} is the drain to source resistance of M_6 and r_{07} is the drain to source resistance of M_7. Value of the r_{06} and r_{07} is very large compare to other terms in eq. (11) neglecting these resistance eq. (11) simplified as

$$Z_{out}(\omega) = \frac{1+j\omega Z_3(\omega).C_{gs6}}{g_{m6}+j\omega C_{gs}6} \quad (12)$$

3.3 Noise figure analysis and optimization

As per friss formula first stage noise figure contribute major in overall noise figure of the multistage amplifier. Here analyzed noise figure of the first common gate stage and it express as

$$NF1 = 1 + \frac{V_n^2}{\alpha^2 A_v^2} X \frac{1}{4KTR_s} \quad (13)$$

Where,

$$\alpha = \frac{Z_{in}}{R_s+Z_{in}} \quad (14)$$

$$Z_{in} = SL_s//(\frac{1}{SC_{gs}}) \quad (15)$$

$$A_v = G_mZ_{out} \quad (16)$$

Substituting eq. (14), (15) and (16) in eq. (13) NF1 is simplified as

$$NF1 = 1 + \frac{\gamma}{G_m}\left[\frac{(S^2L_sC_{gs1}+1)^2R_s}{L_s} + \frac{2(S^2L_sC_{gs}+1)}{L_s} + \frac{1}{R_s}\right] \quad (17)$$

From the eq. (17) shows the first stage noise figure(NF1) isinversely proposal to transconductance (G_m) of M_1, input and output impedance and directly proposal to C_{gs1}. The noise figure is optimized by

- ✓ Setting value of the L_s and C_{gs1} such that it resonant at center of interested band which minimized NF1 at center frequency of the interested band and hence overall NF minimized in interested band.
- ✓ Increasing G_{m1}will reduce NF1 but it degrade input matching. Another way to reduce noise figure is reducing C_{gs1} by reducing W of M_1. On the other hand, scaling down the width of M_1 means more current is required to maintain the same tranconductance and will increase power consumption. The W_1 should be chose such that will improve noise performance at given power budget.

3.4 Layout of design

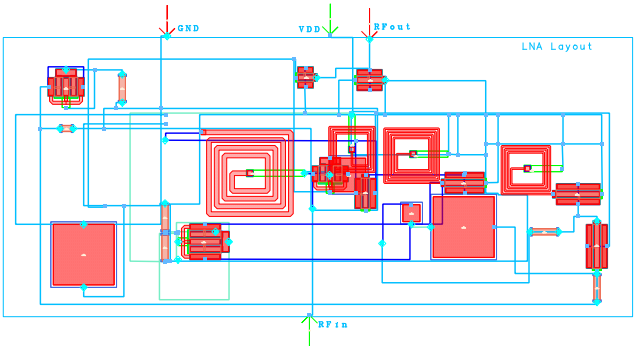


Fig. 6 Layout of wideband LNA

Table : 1 Design Varaible

Component	Value	Component	Value
W_1	5.6x64 µm	Ls	1.71 nH
W_2	5.0x64 µm	Ld1	1.04 nH
W_3	5.0x64 µm	Ld2	2.50 nH

W_4	4.0x64 µm	Ld3	0.69 nH
W_5	4.0x64 µm	Vb1	0.57 V
W_6	2.0x64 µm	Vb2	0.61V
W_7	1.5x40 µm	Vdd	1.8V
Rf	6.0 kΩ	C1,C2,C3	1.0 pf

4. SIMULATION RESULTS AND DISCUSSION

The proposed LNA is design using standard TSMC 0.18µm CMOS technology. The design is simulate using Advanced Design System RF circuit simulator. The fig. 7 shows simulation results of the power gain (S_{21}) and input matching (S_{11}).The simulation results shows designed achieved S_{21} and S_{11} are > 20 dB and < -9 dB respectively in interested band (3.1 – 10.6 GHz). Simulation results of the input isolation (S_{12}) and output matching (S_{22}) are shown in fig. 8. The results shows design having good isolation and matching. Fig 9 shows simulation result of noise figure and the design achieved minimum noise figure 2.7 dB with average NF 4 dB in interested wideband. Harmonic simulation is performed to find linearity of the design. Fig. 10 is the harmonic simulation result at 6 GHz frequency; it shows achieved IIP3 is-3.5 dBm. We have performed harmonic simulation at different frequencies of the 3.1 -10.6 GHz band. Achieved average IIP3 of the LNA design in frequency range 3.1 - 10.6GHz is -5.5 dBm. Fig. 11 shows DC simulation of the design, which shows the design consuming total 19 mA current from 1.8 V supply including bias circuit current. The design stability factor is greater than 1 for interested band as shown in fig. 12, which state design is unconditionally stable.

Various wideband topologies have been used to implement LNA for UWB. Some of the designs mention in literature achieved very good gain but suffer from poor linearity and high noise figure. Simulation results shows proposed LNA design has high power gain, good input matching, low NF and good linearity in the 3.1 – 10.6 GHz wideband with tolerable power consumption. The proposed LNA design will improve the performance of the future UWB receiver and open new frontier for the wireless communication users.

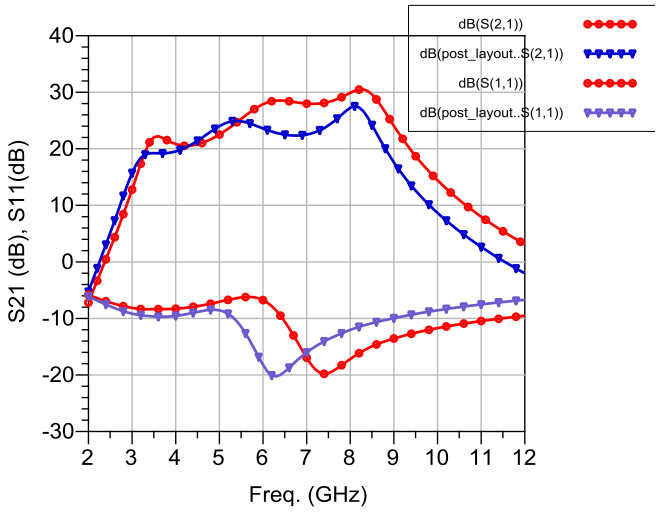


Fig. 7 Power gain simulation

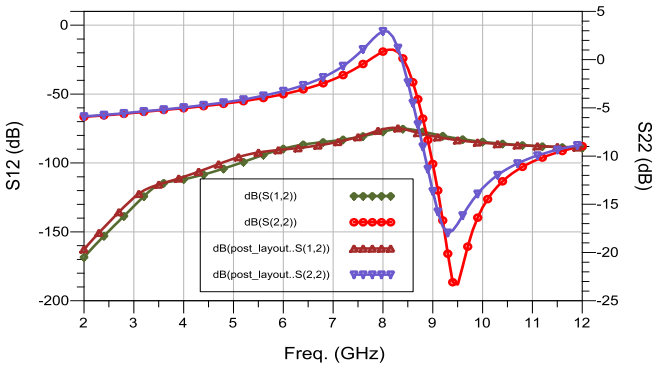


Fig. 8 Input matching simulation

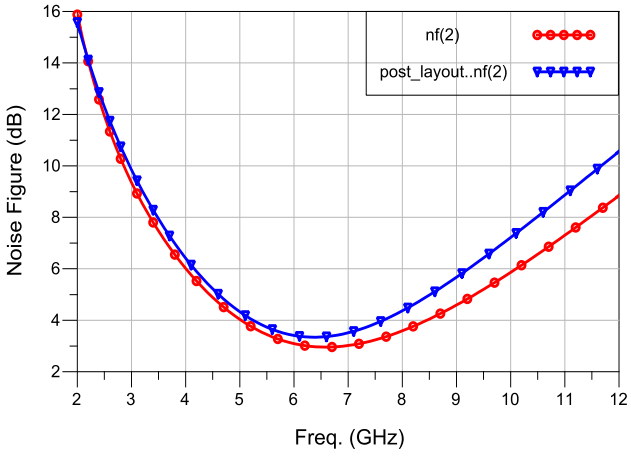


Fig. 9 Noise figure simulation

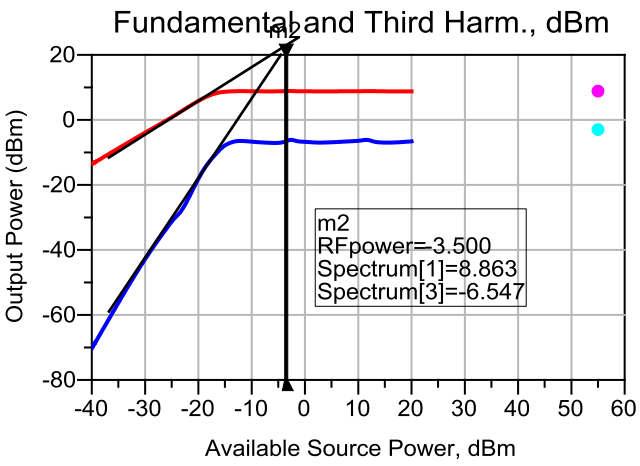


Fig. 10 IIP3 simulation

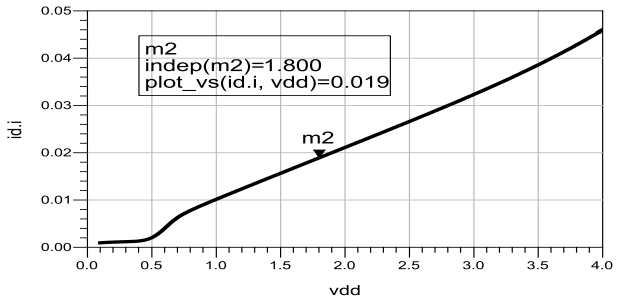


Fig. 11 DC simulation

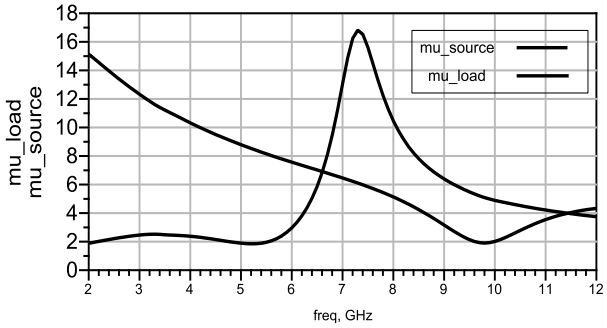


Fig. 12 Stability simulation

Table II. compare results with published Wideband Low Noise Amplifier

Source	**CMOS Technology (µm)**	**BW (GHz)**	**S21 (dB)**	**NF (dB)**	**IIP3 (dBm)**	**Power Consumption (mW)**	**Topology**
JSSC-2004 [10]	0.25	0.002-1.6	13.7	2.4	0	35	R FB +NMOS/PMOS
JSSC-2004 [11]	0.18	2.3-9.2	9.3	4	-6.7	9	CS + degeneration and input BPF
JSSC-2005 [3]	0.18	2-4.6	9.8	2.3	-7	12.6	CS + series RC FB
ICAT-2005 [7]	0.18	2.7-9.3	10	3.3	-0.3	14	Cascode + input HPF
JSSE-2008 [4]	0.18	3.1-10.6	9.5	5-5.6	-13	9.4	Cascode + input filter
JSSCC-2006 [5]	0.18	3-5	<16	2.2	-9	7.68	CS + miller effect input matching filter
JSSC-2006 [8]	0.18	0.04-7	8.6	4.2	+3	9	Distributed cascode
JSSC-2007 [12]	0.13	3.1-10.6	15.1	2.5	-8.5	9	CS + reactive FB
JSSC-2007 [13]	0.18	1.2-11.9	9.7	4.7	-6.2	20	CG + noise cancellation
JSSC-2007 [9]	0.18 SiGe	0.1-11	8	2.9	-3.55	21.6	Distributed cascode + BW enhancement
ISSCC-2007 [14]	0.13	1-7	17	2.4	-4.1	25	Cascode + CD FB
JSSC-2008 [15]	0.13	0.8-2	14.5	2.6	16	17.4	CG + noise and distortion cancellation
MJ-2008 [16]	0.18	5-6	20.5	1.8-2.6	-6.2	2	Cascode + inter stage LC network
ISSCC-2009 [17]	0.18	0.3-0.92	21	2	-3.2	3.6	Differential CG + C Cross coupling
ISSCC-2009 [18]	0.13	3.1-10.6	15	<4.5	-12.5	26	Weighted distributed cascode
TCAS-II2010[19]	0.18	3.1-10.6	13.9	4.7	-8.5	14.4	Parallel RC FB
MTT-s 2010 [6]	0.09	3.1-10.6	10.5	3.2	4	21.6	Cs + Π input filter
MTT-S 2010 [20]	0.18	31.-10.6	13	4.68	-12	10.34	CS + RLC input filter
RFIC 2010 [21]	0.09	21	15.4	6	-6.6	12.5	Distributed CS + tapered transmission line
MTT-2011 [22]	0.09	0.01-1.77	23	2	-2.85	2.8	Differential CG + multiple feedback
IETMAP2012 [23]	0.18	2.4-11.2	14.8	3.9	-11.5	3.4	CG + current reuse
MTT-2012 [24]	0.13	0.6-3	42	3	-14	30	Pseudo differential + resistive FB
IJEC-2012 [25]	0.18	3.1-10.6	15	3.5-3.9	6.4	16.2	Inverter with FB
MWCL-2012[26]	0.065	0.01-2.8	32	1	-13.6	40	Cascode + active –C element
TCAS-II-2013 [27]	0.18	0-1.3	10	3	+7.5	18	Cascode + active feedback
IJMST-2013 [28]	0.18	2.5-16	11	3.3	-5	20	RC FB CS + current reuse
IJEC-2015 [29]	0.13	2.35-9.37	10.3	3.68	-4	9.97	CG current resue + noise cancelling
MJ-2015[30]	0.13	3.5-5	14	3.5-3.9	4	21	Differential + active FB + Noise cancelling
VDAT 2015[31]	0.18	1-7	16-30	4-6	-8	24	CG+ multistage cascoded CS
High power gain UWB LNA	**0.18**	**3.1-10.6**	**20-30**	**2.7-6**	**-5.5**	**34**	**CG + Cascode CS**

5. CONCLUSION

In this research work presented detailed design, analysis and implementation of high power gain 3.1- 10.6 GHz LNA for UWB receiver. The proposed UWB LNA design optimized for specifically high power gain for UWB RF frontend receiver. Due to FCC restriction, low power transmission for commercial UWB wireless applications require low noise high power gain receiver to amplify and process received weak signals. CG first stage provided wideband input impedance matching in the proposed multistage UWB LNA design. The CG has low power gain. The power gain of proposed LNA design has improved by using two cascade CS stages after CG. NF and gain of the design have improved due to inductive load used instead of resistive in the design. Inductive load and next stage input capacitor were formed parallel tune circuit. Bandwidth of the design has improved by resonant each parallel tune circuit at different frequencies in interested band.

Simulation results show that our design achieved power gain (S_{21}) is >20dB and S_{11} is less than -9 dB in interested band (3.1 - 10.6 GHz). The achieved NF of the design is various 2.7 to 6dB in interested band. Our LNA design is consuming 34mW power including bias circuit power consumption. Comparison of the proposed LNA results with recent published literature work is shown in table II. The comparison shows the design achieved very high power gain in wideband with good matching, noise figure and linearity. Due to wideband high power gain the design is most suitable for low power received signals UWB receiver RFIC and it will open new frontier for UWB wireless communication users. The LNA is design using TSMC 0.18µm CMOS technology and simulate the design using Advanced Design System RF circuit simulation tool.

In the design use passive inductors which requires larger silicon area and it is not scalable as technology scale. Silicon area of the design can be reduce using active inductors design instead of passive inductors. Active inductor based LNA design requires less silicon area and design is scalable but it adds more noise and consumes more power compared to passive inductor design. The NF and power consumption of active inductor based LNA cab be reduce by using noise cancelling and low power LNA topology.

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