200 kS/s, 10-Bit Low Power SAR ADC for Biomedical Applications

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ABSTRACT
In this paper, an Ultra-low power 10-bit 200kS/s Successive Approximation Register (SAR) Analog-to-Digital converter is presented. A Split-array charge distribution capacitive DAC is proposed. Spectre simulation results of single-ended 10-bit 200kS/s for supply voltage 1.8V SAR-ADC in a 0.18µm CMOS technology employing the proposed architecture show that the SAR ADC consumes 1.502uW and ADC achieves SNDR of 57.4dB. The ENOB 9.24 resulting in a figure of merit (FOM) of 160fJ/conversion-step.

Keywords: Successive Approximation Register (SAR), Low power, Analog-to-Digital Converter (ADC), Low Supply Voltage, DAC, Biomedical Applications

1. INTRODUCTION
Power Consumption is one of the main design constraints in today ICs. Low power design has become the main concern for battery-powered portable applications[7]. From biomedical Application point of view Implantable devices must consume minimum power, so that it can last up to 10 yrs (for i.e. Pacemaker) which mandate low power consumption per operation[7].

Analog-to-Digital Converters (ADCs) are important building blocks in lots of applications, i.e. biomedical applications. To achieve power savings, the Successive Approximation register (SAR) architecture is often adopted because it has been most power-effective due to minimal active analog circuit requirements [5].

As biomedical signal are very low frequency signal within the range of 10kHz, so here we can make a trade-off between speed and power-consumption. Low power ADC with moderate resolution and low sampling frequency is suited for biomedical applications[5].

The ADC is the crucial part of implantable devices, i.e. pacemaker, since it consume a large amount of power as the interface between sensed analog signal and digital signal processor block[7].

The Comparator, charge/discharge of the capacitive DAC and SAR control logic are primary source of power consumption in a SAR-ADC. The power consumption of a capacitive DAC is proportional to the number of unit capacitors and the charge/discharge of the capacitor array by switching sequence, so power efficiency can be achieved by reducing the total capacitance of the DAC and speed of operation (kHz range)[1]. A comparator used for high resolution ADC consists of preamplifier and Latch is proposed in this paper.

2. PACEMAKER OPERATION
Pacemaker directly controls the pattern and speed of the heartbeat. When the heart stops beating or it beats too slowly, pacemaker provides weak electrical signal with approximately 70 beats/minute to correct the timing of the heart beat. The medical device contains a battery, a generator and pacing leads. The leads connect the pacemaker[7].

Figure shows the block diagram of a pacemaker. The main blocks fall into four parts

1) At the input, there are sensing system, amplifier, filter and ADC.
2) The digital output of ADC is fed to the logic block. This consist of a programmable logic, timing control, system and therapy algorithms.
3) Current and voltage reference generatot and battery power management.
4) At the output of the pacemaker, high voltage pulse generator and multiplier exist.

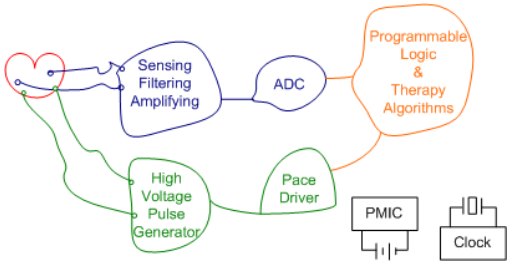


Fig 1: Functional Blocks of Pacemaker

3. SUCCESSIVE APPROXIMATION ADC (FUNCTIONAL BLOCKS OF SAR ADC)
This section describes different component of SAR ADC. The main components of SAR ADC are a Sample and Hold, a Digital to Analog Converter (DAC), a Comparator and a SAR Logic.

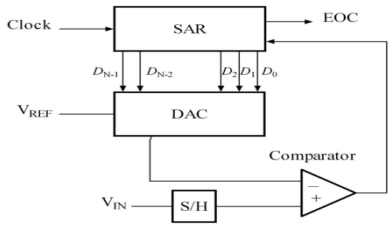


Fig 2: Block diagram of SAR ADC

3.1 Sample and Hold

The Sample and Hold uses a capacitor and an analog switch to connect or isolate from the input. In sampling mode the switch is "on", creating the signal path that allows the capacitor to track the input voltage. When the switch is "off", an open circuit is created that isolates the capacitor from the input, hence changing the the circuit from sampling mode into holding mode.

3.2 Digital to Analog Converter

The DAC has a resolution of 10 bits. The DAC has been divided into two 5 bit DAC to reduce the total area. Also by choosing sufficiently (minimum) value of unit capacitor, the dynamic power of DAC can be reduced. Here, the value of the unit capacitor chosen such that the capacitance should not affected by the Noise (i.e. thermal noise)[2].

3.3 Comparator

The Comparator is an essential part in the SAR ADC to perform the binary search algorithm. Comparator in the SAR ADC takes more power consumption than the other blocks. A comparator generates a logic output high or low based on the comparison of the analog input with the reference voltage.

In an ideal comparator, with infinite gain, for input voltages higher than the reference voltage, the comparator outputs logical one and for the input voltages lower than the reference voltage it produces zero at the output.

Pre-amplifier and buffer stage is used to improve the gain of the comparator and Latch acts as a decision circuit.

3.4 SAR LOGIC

Successive Approximated Register (SAR) control logic determines each bit successively. The SA Register contains N bit for N-bit ADC. The logic block is combinations of D-Flip Flops and timing control circuit.

There are three possibilities for each bit, it can be set to '1', reset to '0'or keeps its value (latch at that value)

In the first step, MSB is set to '1' and other bits are reset to '0', the digital word is converted to the analog equivalent value through DAC. The analog output is referred.

Based on the comparator result, the SAR controller defines the MSB value. If the input is higher than the output voltage of DAC, the MSB remains at '1', otherwise it is reset to '0'. The rest of the bits are determined in the same manner.

In the last cycle of conversion, the converted digital word is stored. Therefore, an N-bit SAR ADC takes N+ 1 cycle to perform a conversion. Here 22 D-Flip Flops are employed in the SAR Logic[5].

4. THE CIRCUITS AND EXPERIMENTAL RESULTS

Here all the building block circuits and their output results are shown.

4.1 Sample and Hold

In the figure below, sample and hold circuit is shown. It comprises of a switch, a dummy switch (to avoid Charge leakage and clock Feed-through).

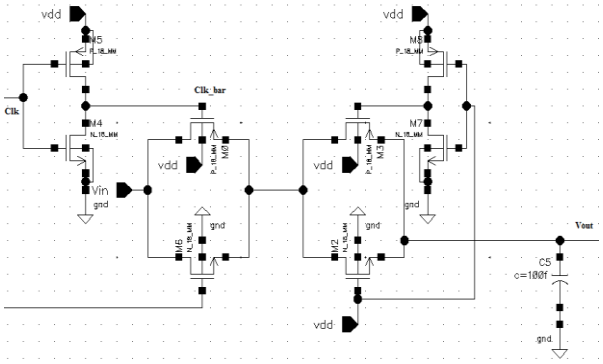


Fig 3 : Sample & Hold Circuit

When the switch is closed (clk='1'), the capacitor C charges that it samples and tracks the input signal. When the switch is open (clk='0'), the output is held at the voltage that the capacitor is charged to at Vout, until the next sampling pulse arrives (clk='1').

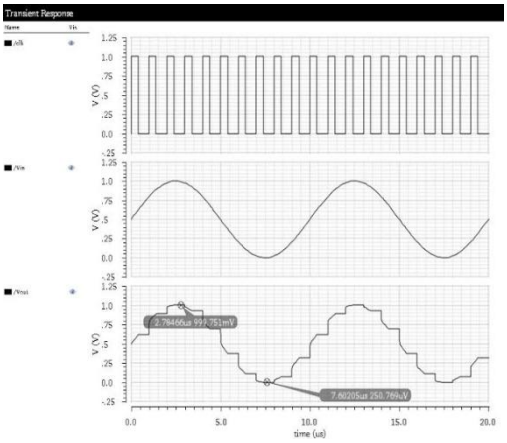


Fig 4: Sample & Hold Waveform

4.2 Comparator

A comparator generates a logic output high or low based on the comparison of analog input with the reference voltage. The comparator in SAR ADC takes more power consumption than the other blocks. In SAR ADC we must design comparator such that it consumes very less power.

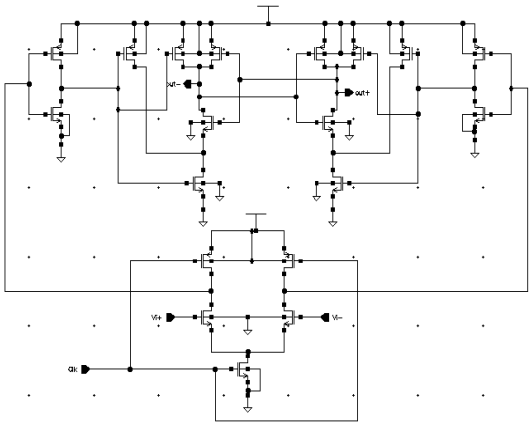


Fig 5: Comparator Latch

The Gain of comparator designed is 73 dB so that, we can get higher resolution and Bandwidth of 1Mhz to accomplish the moderate speed operation.

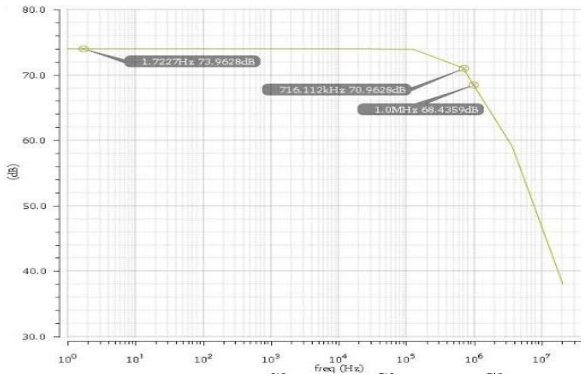


Fig 6: Gain and Bandwidth of Comparator

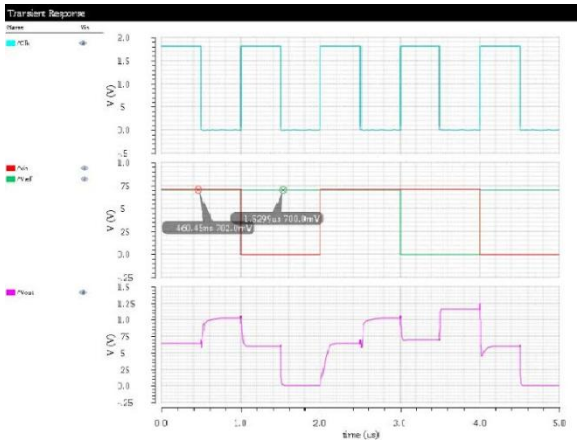


Fig 7: Comparator output for two signals (702mV Vs 700mV)

4.3 SAR Logic

The control logic encompasses a ring counter and a code register. The ring counter is in fact a shift register. In each clock cycle, one of the outputs in the ring counter sets a Flip Flop in the code register. The output of this Flip Flop which is set by ring counter is used as a clock signal for the previous Flip Flop.

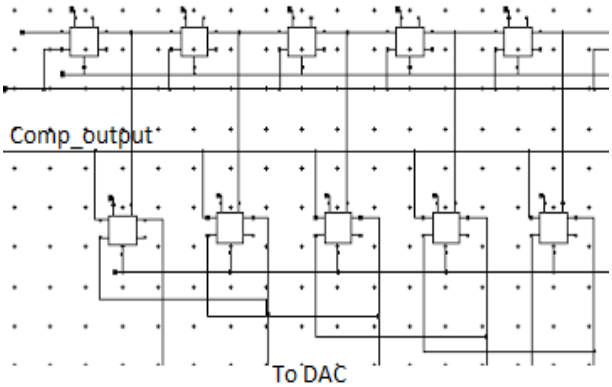


Fig 8: SAR Logic (22 Flip Flops)

Here only a few of D-Flip Flop are show. We employ the SAR Logic by 22 D-Flip Flops. The figure below shows the output for SAR LOGIC where every bit is set one by one.

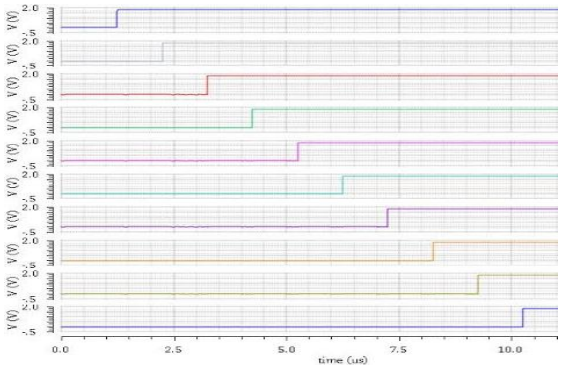


Fig 9: SAR output (all bits are being set one by one)

4.4 DAC

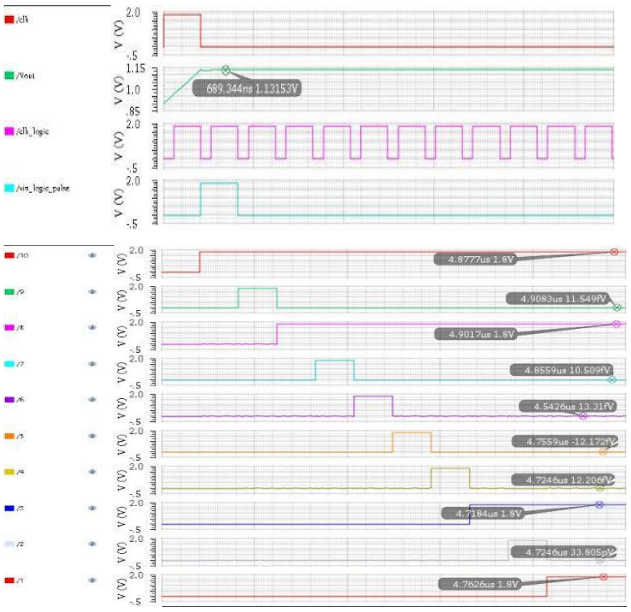
The DAC is implemented using Split array capacitive charge redistribution architecture. The value of unit capacitor of 30fF is chosen to minimizes area and dynamic power consumption.

Fig 10: DAC output(from All bit Reset to All bits Set)

5. EXPERIMENTAL RESULT

The SAR ADC was designed in 0.18um technology. The measured SNR and SNDR are 61.6 dB and 57.4dB respectively. It corresponds to an effective number of bits (ENOB) of 9.24 bits.

The performance of the designed SAR ADC is summarized in Table I and compared with other state-of-art design.



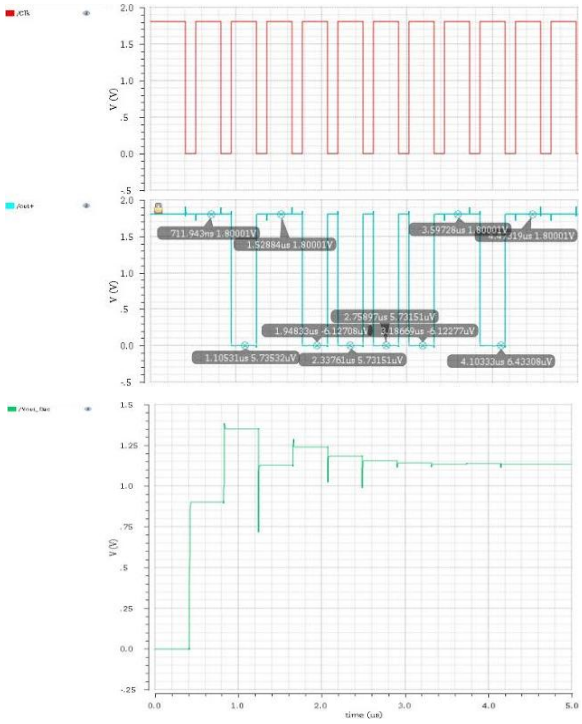


Fig. 11 Final output of SAR ADC for Vin 1.132V

Table I Summary of Performance

S. No.	Comparison b/w this work and reference work.		
	Parameters	**This work**	**Previous work**
1	Process technology	0.18um CMOS Technology	0.18um CMOS Technology
2	Supply Voltage	1.8 V	1.8 V
3	Input range	0 – 1.8 V	2 Vpp Differential
4	Sampling rate	200kS/s	200kS/s
5	Resolution(bit)	12	10
6	Power	1.502uW	72uW
7	SNR @ 97kHz	61.6 dB	62.5 dB
8	SNDR @ 97kHz	57.4 dB	59.3 dB
9	ENoB	9.24	9.56 bits
10	FOM	16fJ/conversion-step	477fJ/conversion-step

6. CONCLUSIONS

An energy-efficient 10-bit 200kS/s SAR ADC was presented in this paper. The designed achieves a peak SNDR of 57.4, dissipating only1.502uW, corresponding to an FOM of 160fJ/conversion-step. Such low power SAR ADC is well suited for biomedical applications. Although the SAR ADC was designed for biopotential acquisition system, it can also be used in other low speed, high resolution applications.

7. ACKNOWLEDGMENT

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