Parametric Variation with Doping Concentration in a FinFET using 3D TCAD

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ABSTRACT
The parametric variations of FinFET in 22 nm due to doping concentrations are presented. In this paper different parameters of FinFET such as subthreshold slope, DIBL, threshold voltage, transconductance and Ioff are analysed using Synopsys Sentaurus 3D TCAD. From the results, it can be concluded that, optimized doping leads to better characteristics for the FinFET.

Keywords: subthreshold Slope, DIBL, transconductance, Ioff, Doping Concentration, FinFET.

1. INTRODUCTION
Down scaling of CMOS bulk transistors, the close proximity between the source and drain lead to the poor gate control on the potential distribution and the flow of current in the channel region, where undesirable effects, called the short channel effects start plaguing MOSFETS. Hence Thin-body MuGFETs (Multi Gate Field Effect Transistors) are strong candidates for replacing their bulk-planar counter parts in deep submicron regime CMOS nodes due to their proven robustness over Short-Channel Effects(SCE).A multi-gate self-aligned bulk FinFET (Fin Field Effect Transistor) transistor resolves these issues because of its processing simplicity and compatibility with standard conventional CMOS process. Where FinFET (Fin Field Effect Transistor) is a most viable implementation of MOSFET in terms of fabrication and layout [1].These FinFETs are mostly fabricated on SOI (Silicon on Insulator) wafers and has shown excellent performance [2]. However SOI FinFETs have disadvantages with respect to their self-heating issues, cost, defect density, etc., when compared to bulk Si (Silicon) wafers [3-4]. Body-tied or bulk FinFETs which are made on standard bulk wafers have attracted attention due to its ability to be easily integrated with conventional CMOS in various applications [5]. Due to their advent usage, the bulks FinFETs are one of the promising candidates to be characterized.

The paper is organized as follows: Section II briefly summarizes the challenges faced in FinFET process technology. Section III briefly discusses the device structure and design constraints considered of a FinFET. Section IV elaborates the results obtained using Synopsys Sentaurus 3D TCAD. Section V concludes the paper.

2. CHALLENGES OF FINFET TECHNOLOGY
The importance of FinFET lies in realization of self-aligned double-gate devices with a standard CMOS method. This permit extending the scaling of gate dimensions beyond the two-dimensional semiconductor device limits, maintaining a steep subthreshold slope, higher performance with bias voltage scaling because of low doping concentration within the channel. Many challenges that FinFET technology face to be competitive are the integration challenges, threshold voltage tuning, junction formation, strain engineering, patterning of the fin (FinFET active area) and also the gate need tighter process management than for its two-dimensional counterpart. Since the FinFET channel is totally depleted, the threshold voltage adjustment is restricted to the gate work function determined by the metal gate conductor. FinFETs with un-doped channels show a benefit over two dimensional transistors in random doping fluctuations [6].

The high performance sensitivity to fin dimensions (width, height) sets up terribly tight restrictions for the process management which can produce an enormous challenge to demonstrate process manufacturability. Challenges in junction formation in bulk relates to the positioning of the junctions with reference to the gate patterning. Owing to the absence of the buried oxide, that forms a natural barrier for dopant diffusion, junction’s area deeper than the fin height leading to degradation of the short channel effect management and the next risk of bulk punch-through [6].

Above 1000^0C temperature, the doping profiles begin to smudge out considerably into the channel. It's fascinating to notice that whereas this reduces the effective channel length, the source/drain profiles tend to fall sharply. The shortest devices are more sensitive to the annealing temperature; however has still a suitable subthreshold slope in the orders of 100 mV/decade. Increasing the implantation dose reduces the off-currents by a pair of orders of magnitude; however this comes at the expense of a 17% reduction of the on-currents. Decreasing source/drain gap size will increase the source drain resistance therefore decreasing drive current. In addition, decreasing gate pitch decreases the stress enhancement for each NMOS and PMOS therefore decreasing mobility and drive [7].

3. DEVICE STRUCTURE AND DESIGN
The Fig. 1 shows the schematic view of FinFET structure. The structure has been considered in dimensions at a 22nm technology. In the Fig 1, the silicon layer is treated as the substrate layer. The raised silicon layer is treated as fin that acts as the device channel, with source and drain regions on either side of the channel [8]. The device has gate length of 22nm, Fin height of 30nm, fin width of 10nm and uniform gate dielectric thickness of 1.5nm over the channel. Even the top oxide thickness is taken as 1.5 nm, since the top gate is left unbiased and has no influence on the device (where as other users consider top gate biasing with higher top oxide thickness). The device has n+ source and n+ drain doping concentrations varied from 10^{17} atoms/cm^3 to 10^{20} atoms/cm^3 and with un-doped channel region. The substrate is uniformly doped with p-type boron atoms of 10^{15} atoms/cm^3. The electrical characteristics are simulated by Drift-Diffusion conduction model.

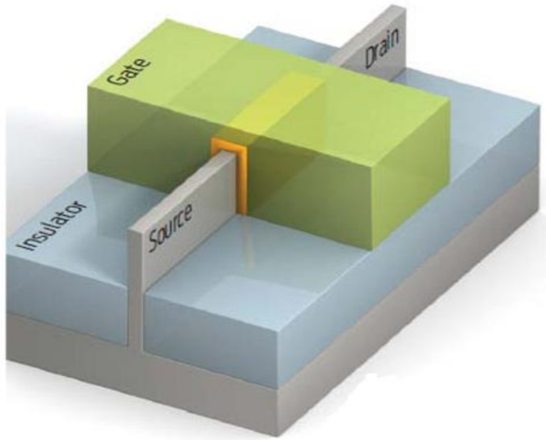

Fig. 1 Structure of 3D FinFET

4. SIMULATION RESULTS AND DISCUSSIONS

The simulation results are obtained for various parameters that influence the device performance such as Ioff (off current), subthreshold slope, DIBL (Drain Induced Barrier Lowering), transconductance, threshold voltage versus variations in the doping concentrations. For studying every parameter mentioned the doping concentration of source and drain is varied from 10^{17} atoms/cm^3 to 10^{20} atoms/cm^3.

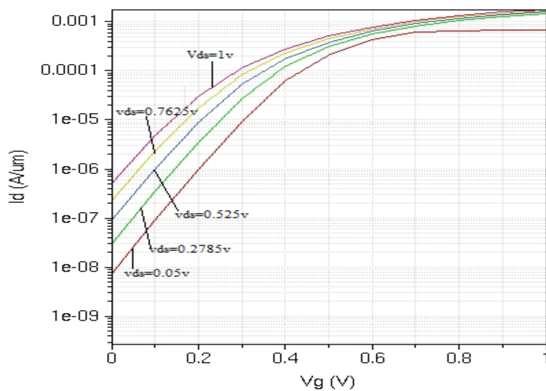

Fig. 2 Vg vs Id characteristics of a bulk FinFET

Fig. 2 shows the Id vs Vg (Drain current vs Gate Voltage) of a 3D bulk FinFET. The curves are taken for different drain biases. From Fig. 2 it can be observed that the leakage current is being increased as the drain bias increases.

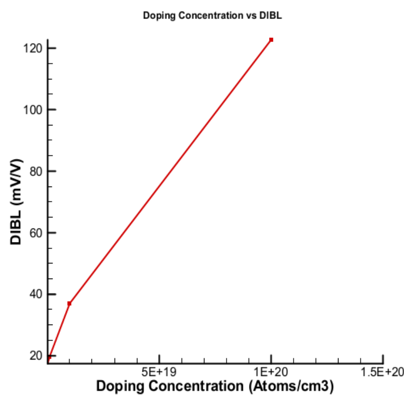

Fig. 3 Doping concentration vs DIBL

Fig. 3 shows the variation of DIBL with respect to doping concentrations of source and drain. As it is already known that DIBL is dependent on doping, the characteristics suggest that more DIBL is encountered when source and drain regions are doped analytically in random. The junction depths should be made shallower, since smaller fin widths are considered for better gate control. Hence the optimum values of analytical function should be given which in turn make an optimum doping and consequently reduce the DIBL. From Fig. 3 it can be observed that the DIBL increases if the doping concentrations of the source and drain regions are increased.

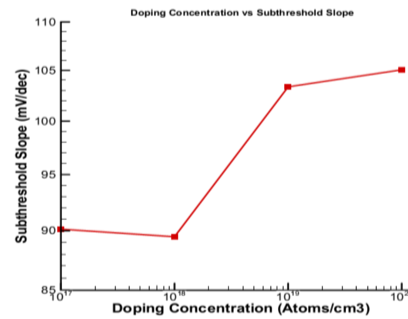

Fig. 4 Doping concentration vs Subthreshold Slope

Fig. 4 shows the variation of Subthreshold Slope with respect to doping concentration of source and drain. As doping increases the subthreshold slope decreases which is due to the increase in carriers in respective source and drain regions.

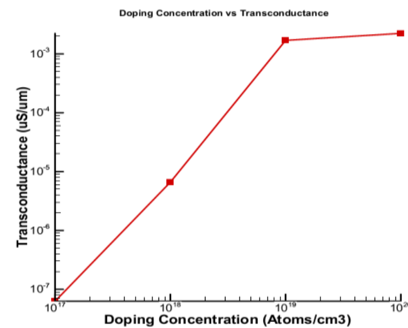

Fig. 5 Doping concentration vs Transconductance

Fig. 5 shows the variation of transonductance with respect to doping concentrations of source and drain regions. With increase in doping concentrations transconductance increases as more number of carriers constitute the flow of current in the formed channel region. This indirectly depicts the increase in the short channel effects.

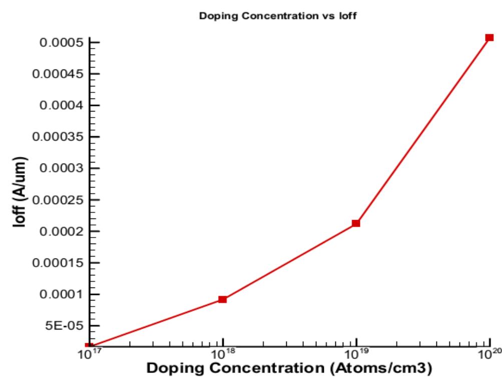

Fig. 6 Doping concentration vs Ioff

Fig. 6 shows the variation of off current with respect to doping concentrations of source and drain regions. As doping increases we can see that the Ioff current increases because the charge carrier concentration increases with the increase in doping concentration. And also Ioff increases due to the band to band tunneling during the operation of the FinFET.

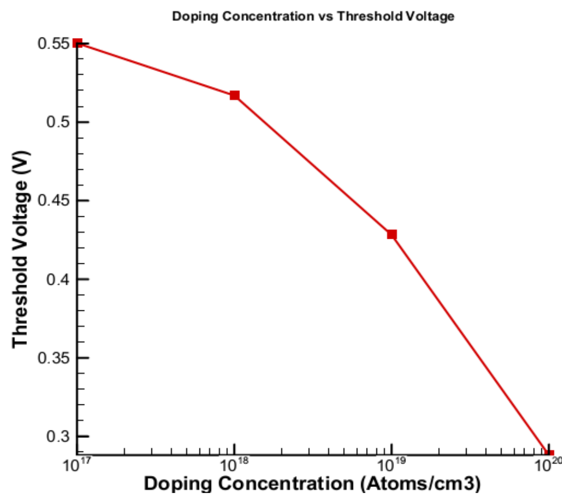

Fig. 7 Doping concentration vs threshold voltage

Fig. 7 shows the variation of threshold voltage of the FinFET with respect to increase in the doping concentration of source and drain regions. As doping increases the threshold voltage of the FinFET decreases. And the threshold voltage is more at the doping value of 10^{17} atoms/cm^3.This is in generally is due to body tied structure of the FinFET.

5. CONCLUSIONS

In this paper the variation of parameters like DIBL, subthreshold slope, off current, transconductance and threshold voltage with respect to the doping concentrations of source and drain regions of a FinFET are studied. The results show that the doping variations deceases the threshold voltage of FinFET and increases all the other parameters studied. A better optimized doping is necessary for the device to attain the better characteristics. Hence always a better optimized doping should be done, else better optimized models usage of doping are to be concentrated to use the Bulk FinFET to be a promising candidate for remaining bulk FETs (Field Effect Transistor).

6. REFERENCES

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