# Planar Monopole Ultra Wide Band Antenna on Silicon with Notched Characteristics

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# ABSTRACT

The design and development of Ultra Wide Band (UWB) antenna on silicon substrate is presented in this article. Planar monopole antenna having circular radiating patch, excited with 50  $\Omega$  co-planar waveguide transmission line is chosen here. Slots are incorporated in the radiation patch to achieve bandnotch characteristics at two distinct bands for WiMAX (3-4 GHz) and WLAN (5-6 GHz) applications. Both single and dual-notch banding concepts are presented. A close analogy is achieved between measured and simulated results after fabricating the finalized topologies on high resistive silicon substrate. Effects of fabrication/assembly on performance of the final device are also discussed in this article.

**Index Terms:** Band-notching, High resistive silicon, Monopole antenna, Ultra wide band antenna.

## **1. INTRODUCTION**

Ultra Wide Band (UWB) systems are gaining popularity in modern communication era and in future such systems need to be developed for space, defense and ground applications [1]. Main passive components of UWB systems are antennas and filters. Inherent challenges of designing these building blocks are to cater wide range of frequencies (3.1 GHz- 10.6 GHz) and rejection of undesired frequencies. Till date various configurations of UWB antenna have been reported. Among these, most popular is the planar one due to its compact size, low profile and light weight features [2]. In addition to that, it can be easily accommodated into various systems encompassing ground as well as airborne. Conventional patch antennas are inherently narrow-band (5 -10%) [3] & various techniques adopted by researchers to enhance the bandwidth [4]. Using monopole configuration in the planar topology gives the best suited performance in achieving ultra-wideband[5]. Recently, several broadband monopole configurations, such as circular, square, elliptical, pentagonal and hexagonal have been reported for designing patch. Another important feature to be incorporated in modern system is band-notch behavior as to frequency of avoid interference already existing communication systems, falling in this frequency range. Bluetooth (2.45 GHz), WiMAX (3.5 GHz), WLAN (5.5 GHz) and satellite communication (8.2 GHz) are the major interferences. Various strategies were adopted to obtain bandnotching, like- open loop resonator, electromagnetic band gap, slot incorporation, filter insertion [6-12], etc. Out of these, slot embedded design is chosen due to simpler configuration and realization. The main feature of the present article is realization of this topology on high-resistivity silicon ( $\rho > 8 \text{ k}\Omega\text{-cm}$ ). In future, integration of multiple building blocks of the UWB system is possible on silicon.

Different configurations are simulated and optimum ones are chosen to realize single and dual notch topologies. Measured results show close analogy with predicted values for the realized topologies in the full band and is detailed in this article.

#### 2. ANTENNA DESIGNING

The Antenna design can be broadly categorized into two parts: Patch design and Slot Design.

#### 2.1 Patch Design

The geometry of the proposed structure is shown in Figure. 1. Main design parameters of this are: input impedance, diameter, gap between excitation and disk and width of the ground plane

The ground plane serves as an impedance matching circuit. Consequently, it tunes the input impedance and hence the 10 dB return loss bandwidth by changing the feed gap and the height of the ground plane. Another important design parameter is the diameter of the disc. Current distributions have indicated that the first resonance frequency is associated with the disc dimension [2]. Simulation results shows, first resonance frequency decreases with the increase of diameter of the disc. At 25 mm, it shows optimum results.

In this configuration, the 50 $\Omega$  coplanar wave guide line of dimension 0.4/0.92/0.4 (mm) is used for feeding/exciting the radiating patch. The overall cross-sectional area of the antenna is 47 mm  $\times$  47 mm. It is designed for standard 675  $\pm$  25  $\mu m$ thick high resistive silicon substrate ( $\rho > 8 \text{ k}\Omega\text{-cm}$ ). Sparameters of the antenna have been extracted in the FEM based simulation environment, shown in Fig.2. HFSS [13] is used for analyzing the return loss characteristics and computing far-field radiation pattern. The same design is verified on 25 mil Alumina substrate. The comparative results are cited in Table-I. Same design concept is validated for other microwave substrates also. It can be inferred from these data that, radiation efficiency and the front-to-back ratio of the proposed antenna is superior in case of Silicon than Alumina. It is because of high permittivity of the substrate, which reduces the radiation loss toward the undesired direction.

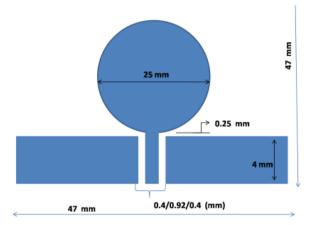


Fig.1: Geometry of the prototype circular disc monopole antenna

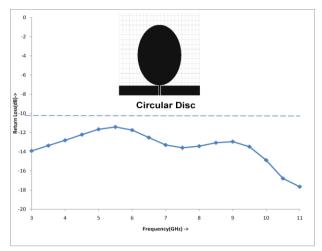


Fig.2: Simulated return loss of the circular geometry UWB Antenna

Table-I: Comparative Study of the Antenna Parameters on various substrates

| Antenna Parameters   | Alumina | High Res.<br>Silicon |
|----------------------|---------|----------------------|
| Radiation Efficiency | 97.73 % | 99.79 %              |
| Front to Back Ratio  | 145.63  | 506.13               |

# 2.2 Slot Design

In this work, various shaped slots are considered to realize notch at 3.4 GHz & 5.5 GHz. Slot provides strong radiation attenuation at the corresponding notch frequency. Basically, it acts as a band-stop filter, which filters out the desired notch frequency. Dimensions of the slots are calculated using eqn. (1) [11].

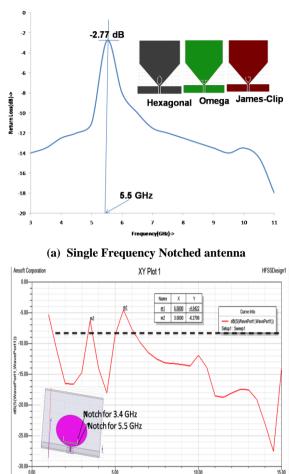
$$\lambda_g = \lambda \sqrt{\frac{2}{\varepsilon_r + 1}}$$
 .....(1)

Where,  $\lambda_g$  = Guided wavelength,

 $\lambda$  = Free-space wavelength

 $\epsilon_{\rm r}~=$  Dielectric constant of the substrate.

Using the Eqn. (1), the length of the slots for 5.5 GHz and 3.4 GHz are coming as 10.8 mm and 11.4 mm, respectively. The width of the slot is optimized as per the required bandwidth at notched frequency, which in present case is arrived at 500 µm. Slots are placed at the vicinity of the feed line, where electric field or magnetic current vectors are densely populated. Basically, slot changes the direction of E-field/magnetic current resulting in notch at desired frequencies. Five different shaped slots (Omega, James Clip, Hexagonal, U and I) have been studied in this work. Out of these, simplest configuration rectangular shaped topologies were chosen for fabrication purposes. Fig.3 depicts the simulated performance of the single and dual band-notched antenna. And, the distribution of the surface current is shown in Fig.4. It can be inferred that, electric field vectors concentrate more at the open ends of the slots at the notch frequencies.



(b) Dual-band notch antenna Fig.3: Various slot-shapes for band-notch characteristics

Freq (GHz

Table-II depicts a comparative notching behavior for different slot shapes for the same notch frequency of 5.5GHz. And, the surface current densities for the different shapes of slots are summarized in Table-III. From the above data, it is clear that, the surface current distribution at the open-end of the Omega shaped slot is ten times more than other slots mentioned here. These current vectors are mainly responsible for providing strong radiation attenuation at the corresponding notch frequency. It reveals that the Omega –shaped slot is best suited for notching.

| Slot Shape      | Loss @Notching<br>frequency(dB) |  |
|-----------------|---------------------------------|--|
| $Omega(\Omega)$ | -2.77                           |  |
| Hexagonal       | -3.72                           |  |
| James Clip      | -7.31                           |  |

Table-II: Comparative analysis of various slot shapes for band notch characteristics

# 2.3 Antenna Parameters

Simulated far-field radiation of the designed CPW-fed UWB antenna with band-notch feature is shown in Fig5. An overall stable radiation pattern throughout the band except the desired notched bands has been observed for the proposed antenna.

Table-III: Current density plot of various slot-shaped antennas

| Shape of the Slot | Max. Surface current<br>density[A/m] |
|-------------------|--------------------------------------|
| Hexagonal         | $1.10 \times 10^{3}$                 |
| Rectangular       | $3.3 \times 10^{2}$                  |
| James Clip        | $2.0 \times 10^{2}$                  |
| Omega             | $1.174 \times 10^{3}$                |

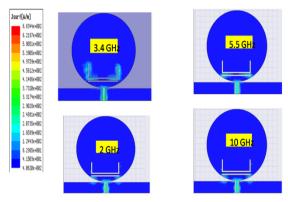


Fig.4: Current distribution of notched antenna

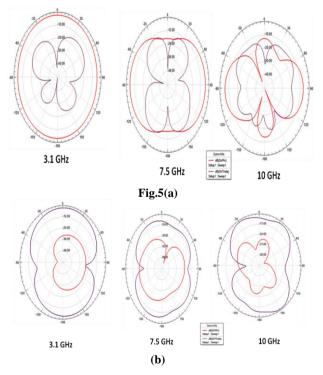
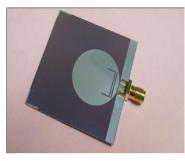


Fig 5: Simulated radiation pattern of the antenna in (a) H plane/XZ plane. (b) E plane/YZ plane

# **3. FABRICATION AND MEASURED RESULTS**

Fabrication of the structure is carried out using standard CMOS process on 6" high resistive Si ( $\rho > 8 \ k\Omega$ -cm) wafer (FZ processed, tan $\delta = 0.01$ ). Initially oxide/nitride layers have been deposited as a buffer layer over Silicon. Metallization of 2.5  $\mu$ m is done using DC sputtering and standard wet chemistry is employed for etching purpose. Critical dimension of the structure is around 0.25 mm.

Standard dicing tool with diamond cutter is used for dicing purpose and RF connectors is integrated in the antenna structure using conductive epoxy (H70E), as shown in Fig.6.

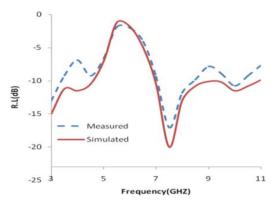


(a) Dual-band notch embedded antenna

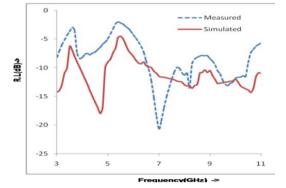


(b) UWB Antenna with single-band notch Fig.6: Fabricated Prototype antenna structures with connectors at feeding point

The prototype structure realized in an overall dimension of 47 mm × 47 mm and performance parameters are measured using Vector Network Analyzer. Input return loss is better than 10 dB throughout the entire frequency band. The return loss measurement of the antenna shows a clear signature of bandnotching at the desired frequency bands. Fig.7 compares the measured data for these band-notched antennas, where a close relevance is observed. Slight variation in the return loss values for the fabricated structure is attributed to the tolerances in resistivity and fabrication. The fabrication point includes nonnegligible tolerance values (~ 1 mil) associated with film masks as compared to CMOS photolithography masks. This amount of tolerances can result in significant deviation of antenna performances. During assembly of the RF connector at the feed portion of the antenna, unexpected spreading of conductive epoxy occurs as the whole process is done manually. It can lead to change in gap dimension of the actual CPW line. It further degrades the characteristic impedance of the line, which may randomly affect in mismatching of impedance at any arbitrary frequency. Simulation results show that, the characteristic impedance can even fall in the range of 30-40  $\Omega$  instead of 50  $\Omega$  due to above practical reason. The effect of epoxy has been analyzed in electromagnetic solver, as shown in Fig.8. It reveals that, the return loss value can degrade up to 8 dB for the asymmetrical spreading of conductive epoxy at the feed portion of the antenna.



(a) Single-band notching (I-slot)



(b) Dual-band notching (U and I shaped slots) Fig.7: Comparative data Analysis

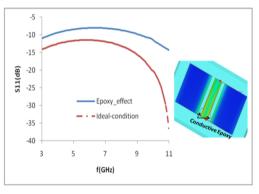


Fig.8: Effect of epoxy spreading on RF performance

### **4. CONCLUSIION**

This article demonstrates a planar, monopole UWB antenna on Silicon with band-notch characteristics. It has frequency band notches centered at 3.5 GHz and 5.5 GHz. Two prototypes of the antenna were fabricated and verified experimentally. Measured results show a close agreement with the simulated performances. A low cost alternative is adopted for realizing the structure using CMOS foundry. Simple layout, without any fabrication intricacy is the main attraction of this design. As per authors' knowledge, this kind of antenna topology is not been reported on silicon till date. Moreover, siliconisation of the antenna establishes the new way for integration of all building blocks of UWB system on a single chip. Further, batch processing is possible for silicon wafer using CMOS foundry, which also cut down the cost of the overall system realization.

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