A Low Jitter Phase Locked Loop for High Speed Serial Interfaces

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ABSTRACT
This paper presents a new circuit for clock generation. A new phase frequency detector is designed in 130nm CMOS process technology. The phase locked loop is designed to meet the 10BaseKR wire line communication standards. All the circuits are designed in current mode logic for high speed operation. The designed circuit dissipates mW. The voltage controlled oscillator has phase noise of -182.2dBc/Hz at 1 MHz offset from center frequency. The designed phase locked loop has rms phase jitter of 44.17fs.

Keywords: Wire line communication, Phase locked loop , phase noise, current mode logic.

1. INTRODUCTION
The data transfer rate has increased tremendously over the past few years. Phase locked loop (PLL) plays a vital role in many applications such as clock generation, clock and data recovery circuits, memory circuits, high speed digital systems to generate very low jitter for on-chip clocks. Jitter analysis is has been part of literature which analyze the different kinds of jitter. Many factors such as loop bandwidth , damping ratio affect the jitter and stability of the phase locked loop(PLL).Very low bandwidth and high damping ratio are very frequently used in obtaining clean reference clock By understanding the parameter dependability a low jitter PLL can be designed[1]-[4]. Section I starts with block diagram of PLL. Section II describes the design of phase frequency detector (PFD) . Section III presents the design of reference based charge pump. Section IV describes loop filter and voltage controlled oscillator (VCO). Section V describes discusses the simulated results.

2. PHASE LOCKED LOOP
The performance of high speed systems are limited severely by clock skew, clock jitter and noise generated by various noise sources in circuits. There are various blocks in phase locked loop such as phase frequency detector(PFD), charge pump, loop filter, voltage controlled oscillator(VCO) and frequency divider. The block diagram of PLL is shown in Fig 1. A PLL is a feedback system that compares the phase of feedback signal. The comparison is performed by phase detector (PD). There are different kinds of PLL such as charge pump PLL and delay –locked loops (DLL).

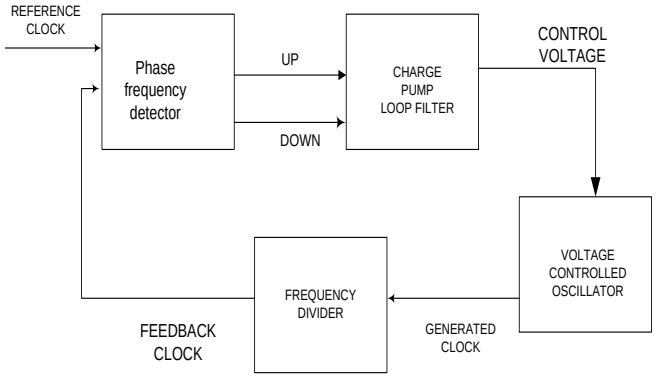

Fig.1. Block diagram of Phase locked loop

3. PHASE FREQUENCY DETECTOR
There are two types of phase detectors (PD) such as XOR PD and phase frequency detectors (PFD)[5]. The XOR PD has good noise rejection but locks onto harmonics of the clock thereby generating ripple even when loop is locked. This modulates the clock frequency which is an unwanted characteristic of PD. XOR PD has problems locking if the VCO duty cycle dithers around 50%. The block diagram of modified PFD is shown in Fig.2

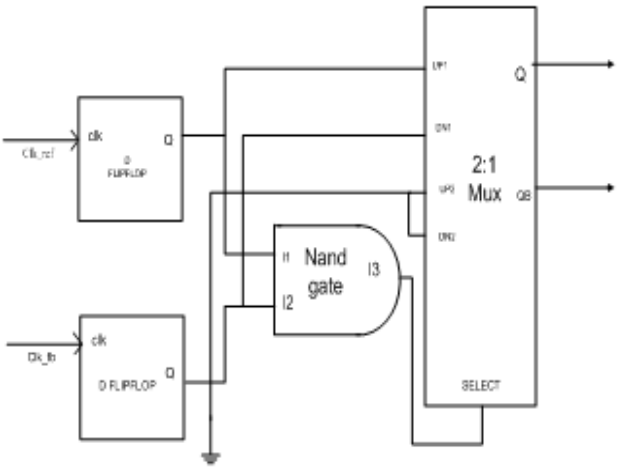

Fig.2 Modified Phase frequency detector

It compares the leading edges of reference and feedback clock from the frequency divider. The rising edge of reference clock and feedback clock must be present to make a phase comparison. PFD does not lock onto harmonics. The up signal is high when the feedback clock lags the reference clock and down signal is high when reference clock leads the reference clock as shown in Fig.3.

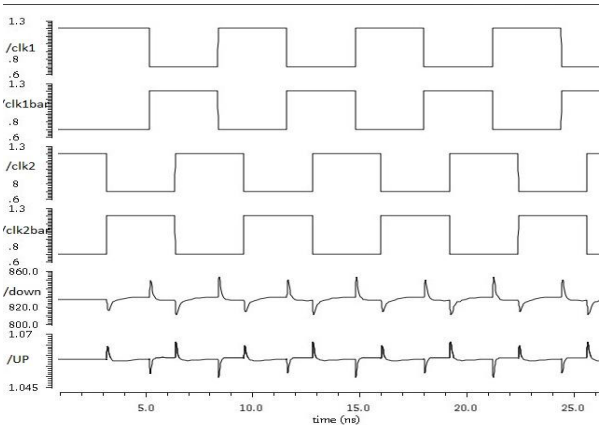

Fig.3 Output of Phase frequency detector

4. CHARGE PUMP

The output of PFD needed to be combined into a single output for driving loop filter. This can be done in two methods as shown in Fig 4. The main problem is that present in Fig 4.a is the output of charge pump is dependent on supply and that affects the output of charge pump. The effect of variation of charge pump output can be reduced by adding a current source as shown in Fig.4.b. Let I_{pump} represent the charge pump current. If the output of PFD uses the charge pump configuration of Fig4.b then the output current is given by I_{PDI} . $\Delta\Phi$ represents the phase difference between the reference clock and feedback clock and K_{PDI} is the gain of PFD.

$$I_{PDI} = (2I_{pump} / 4\pi)*\Delta\Phi = K_{PDI} *\Delta\Phi. \qquad (1)$$

It is assumed equal current flows in the pull up and pull down structure. To increase the current matching capability of charge pump there many methods. The second order effects such as channel length modulation can be reduced by increasing the output impedance. The output impedance can be increased by cascade current mirror and by using gain boosting technique. One more of reducing the current mismatch is reference charge pump method. The circuit schematic of charge pump is shown in Fig.5. The error of PFD amplifier compares the voltages at its input and generates an error voltage to minimize the current mismatch.

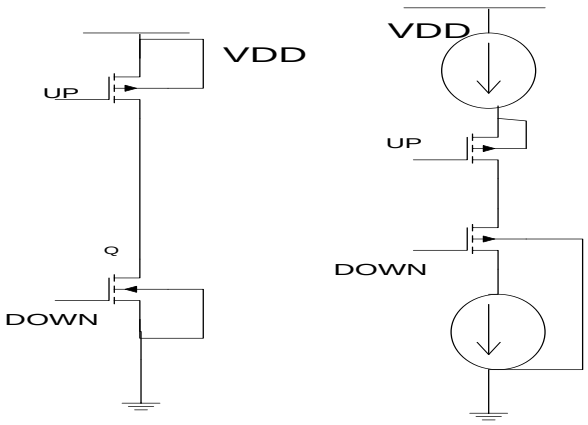

Fig 4. (a) Tri-state (b) Charge pump outputs

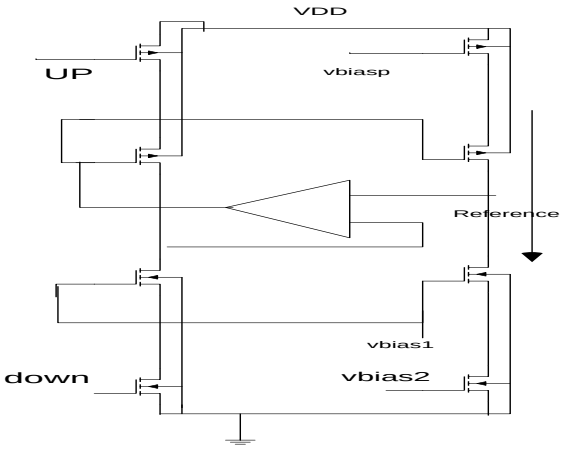

Fig.5. Reference based charge pump

5. LOOP FILTER AND VOLTAGE CONTROLLED OSCILLATOR

The output of charge pump is given to loop filter (LPF). The schematic of loop filter is shown in Fig.6. For slow variation in the output of charge pump the loop filter acts as integrator[6].

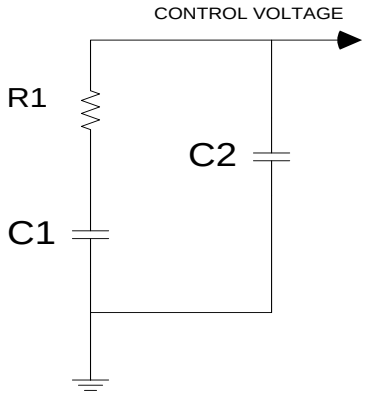

Fig.6. Loop filter

For fast variations the LPF acts as resistive divider and allows the loop to track fast variations. The output of LPF is shown in Fig.7.

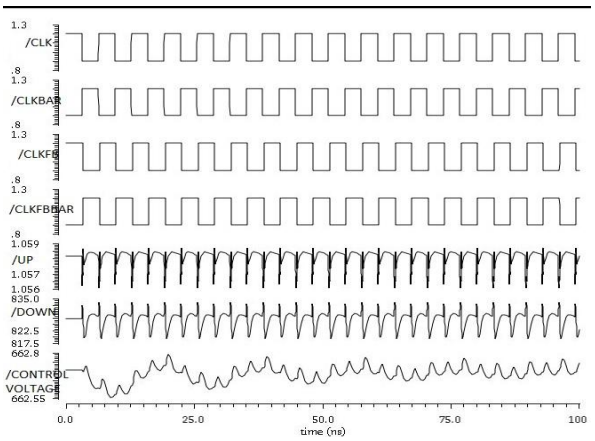

Fig.7. Output of Loop filter

There are two types of voltage controlled oscillators such as ring oscillator and LC oscillator. The output of ring oscillator is sensitive to supply voltage variations and noise in the circuit. LC oscillator is chosen as its phase noise is less compared to ring oscillator. For oscillations to begin a loop gain of greater than unity even in the presence of temperature and process variations along with meeting the barkhausen criteria. The schematic of LC oscillator is shown in Fig.8. The skin effect plays a vital role in design of the oscillator as the metal loss increases at higher frequency. Let R_s represent the series resistance of inductor. Let R_p be parallel equivalent of series resistance of the inductor.

$$R_p = Q^2 R_s. \quad (2)$$

$$V_{swing} = I_{bias} * R_{tank} \quad (3)$$

$$R_{tank} = 1/gm_{n,p} \quad (4)$$

$$gm_{n,p} = -2/R_p \quad (5)$$

Where Q is the quality factor of the inductor, $gm_{n,p}$ are the effective transconductance of N and P cross coupled transistors. The voltage sensitivity curve of VCO is shown in Fig.9. Voltage controlled oscillators has gain of 1020Hz/V and phase noise of -182.4dBc/Hz as shown in Fig.10. There are various constraints are imposed on the clock generator for meeting the wire line communication standard. The simulated eye diagram of a backplane is shown in Fig.11. The simulated results indicate a timing margin of 0.15 unit interval (UI) for receiving peak voltage at the input of transceiver. Eye patterns are used vastly for measuring the quality of received data. The eye opening measures the additive noise of the signal, the eye overshoot over shoot or under shoot gives the peak distortion due to interruptions in the signal path, the eye width gives the timing synchronization and jitter effects and the eye closure gives the ISI , additive noise. All the real oscillators have phase modulated (PM) noise components.

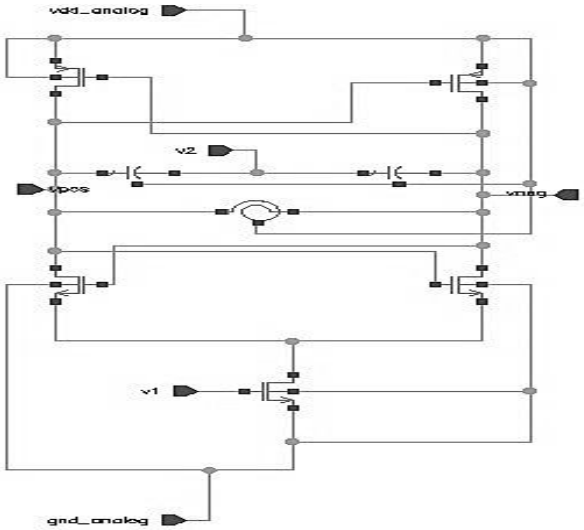

Fig.8. LC oscillator

The phase noise components reduce the power of a signal to nearby frequencies which are translated to noise sidebands.

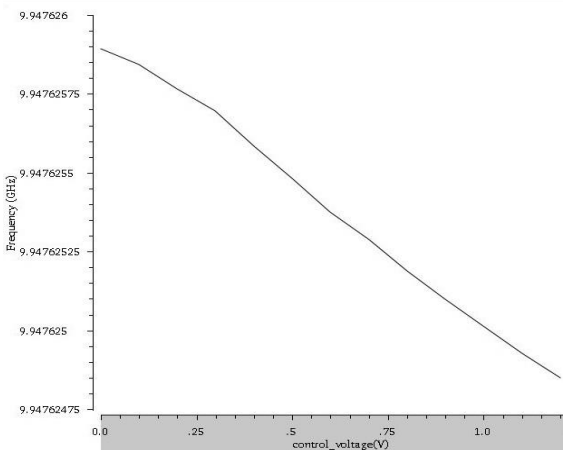

Fig.9. Tuning range characteristics of VCO

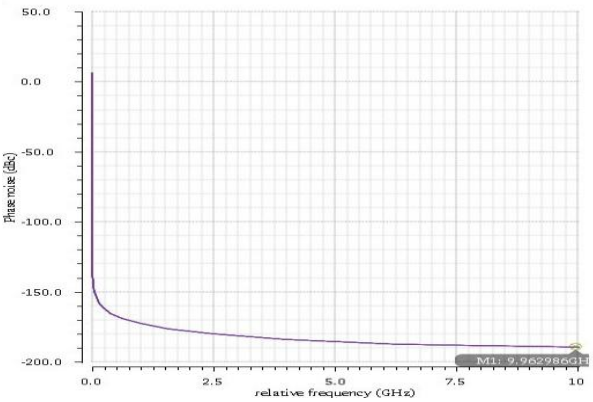

Fig.10. Phase noise plot of VCO

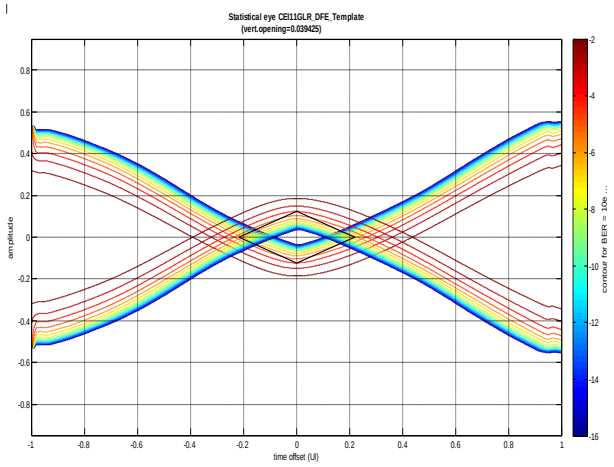

Fig.11.Simulated eye diagram of backplane

The figure of merit(FOM) of LC oscillator [] is used to performance of two VCOs[7].

$$\mathrm{FOM}_T = L\{\Delta f\} - 20\log\left(\frac{f_0}{\Delta f}\cdot\frac{\mathrm{TR}}{10}\right) + 10\log\left(\frac{P}{1\,\mathrm{mW}}\right) \quad (6)$$

Where L(Δf) is the phase noise , Δf is an offset frequency from center frequency f_0 , TR is the tuning range and P is the power dissipation. Table 1 shows the comparison among various LC oscillators designed.

Table.1

Reference	Process	Freq (GHz)	Phase Noise (dBc/Hz)	Power (mW)	FOM_T
[8]	130nm	59	-89@1Mhz	9.8	-174.5
[9]	130nm	40	-110@1MHz	11	-183.1
This Work	130nm	10GHz	-114@1Mhz	6.64	-192.4

6. CONCLUSION

A low phase jitter is designed for high speed serializer electrical interfaces. The designed PLL has phase jitter of 44.17fs and phase noise of -182.47dBc/Hz. The designed VCO consumes 4.6mW.

7. REFERENCES

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