A Novel Design of QPSK Modulator for High Data Rate Transmission

Eleena Mohapatra
Eastern Academy of Science
and Technology
Odisha
India

ABSTRACT
This article proposes a new approach to digital modulation techniques. A novel design for a QPSK VHDL modulator to convey a high data rate transmission is demonstrated. Basically CPLD or FPGA technology is used to generate hardware and the hardware generation is possible from VHDL code. The implementation of the device is done to perform the modulation. Then the data transmission rate also increases. This types of modulator provides digital synthesis and the flexibility to reconfigure and upgrade with the two most often languages used being VHDL and Verilog (IEEE Standard) being used as hardware structure description languages.

Keywords
BPSK ; QPSK ;VHDL

1. INTRODUCTION
Demand for a high data rate is increasing, and require an efficient modulator to achieve both high data rate [1] and low power consumption. In such applications, the QPSK modulation has advantages over other schemes, and double symbol rate with respect to the BPSK [2] over the same spectrum band. This is contrast to analogue modulators for generating the QPSK signals, where the circuit complexity is very high and the power dissipation is very less, basically unsuitable for medical purposes. This type of modulator provides a digital synthesis and the flexibility to be re-configured and upgraded with two of the most often used languages, VHDL and Verilog (IEEE standard), based as hardware structure languages described in [3] [4]. All analogue or hybrid analogue/digital QPSK modulators work with the phase shift of the carrier (φ), as the key of the modulation [5] [6]. The phase shifter is the most important element in the modulator to acquire two discrete signals i.e. sin ($\omega_c t$) and cos ($\omega_c t$) where f_c is the frequency carrier. Practically, it uses a direct digital synthesizer (DDS) or numerical control oscillator (NCO) to generate the carrier signal [9]. However, in analogue modulation it is essential to use the NRZ format to map I and Q, that produces analogue QPSK signal, which can be represented mathematically in equation 1 is given by [7]

$$\mathrm{QPSK}(t) = \mathrm{I}(t)\cos(\omega_c t) - \mathrm{Q}(t)\sin(\omega_c t)$$

Where I and Q are defined in equations 2 and 3 respectively:

$$I(t) = \sqrt{\frac{2E}{T}}\cos\left[(2i-1)\pi/4\right]$$

$$Q(t) = \sqrt{\frac{2E}{T}}\sin\left[(2i-1)\pi/4\right]$$

Where I (t) is the in phase of data

Q (t) is the quadrature of data

i is the number of M (M=4 for QPSK)

E is the transmitted signal energy per symbol

And T is the symbol duration.

2. METHOD MODULATOR DESIGN
2.1 Digital VHDL QPSK Modulator
The proposed QPSK VHDL modulator was programmed to generate a carrier phase shifter to acquire four discrete states (0º, 90º, 180º, and 270º), where the input data was split into two separate streams in-phase I and quadrature phase Q to map the carrier signal, which was interfaced to the multiplexer. The output is selected by multiplexer to provide a digital QPSK signal. This signal passes through a passive filter before being transmitted that eliminates the high frequencies. The Figure 1 demonstrates the proposed VHDL QPSK modulator compared to an analogue modulator. The digital QPSK signal of the multiplexer output can be represented in equation 4 below:

$$MUXout = \bar{I}\bar{Q}C0 + \bar{I}QC90 + I\bar{Q}C180 + IQC270$$

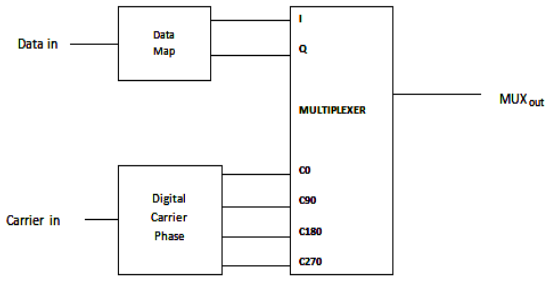

Figure1: Block diagram of proposed digital VHDL QPSK modulator

However, in analogue modulation when generating the QPSK signal and data are in NRZ signal format, it is essential to map the data into I and Q streams, which are influence the carrier signal according to the transition of the input data. To convert the carrier, it is synthesized with

a periodic pulse signal, which generates four discrete states (0°, 90°, 180°, and 270°), while the data mapping is described in different concepts. The direct digital Modulator is controlled by two streams I and Q of the carrier (0°, 270°) and inverted data is the controlling carrier (90°, 180°), then two carriers are combined together and subtracted in order to produce the QPSK signal. Figure 2 which shows how the carrier signals and data are generated individually; each phase of carrier signal is controlled by a single mapping of data then combined by multiplexer, to generate the desired digital QPSK signal.

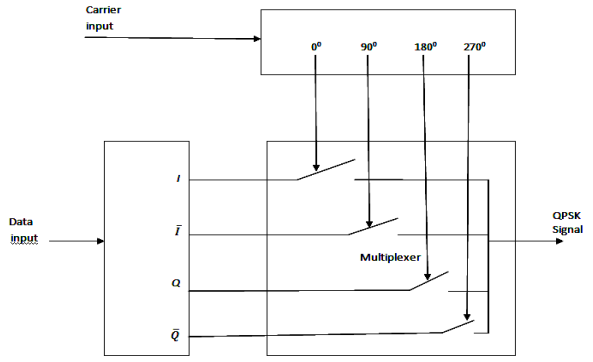

Figure 2: Concept of generating QPSK digital modulator

The simulation from 2 to 12 GHz gives return loss (S11) is shown in figure 2 with dual band performance at 7.2 GHz (6.922-7.51 GHz) and 10.37 GHz (10.01-10.72 GHz).

The structural design of the proposed digital modulator is shown in figure 2, demonstrating the output signals that indicate the carrier phase shifter (0°, 90°, 180°, and 270°). While the data source was generated with PN_ sequence generator [8], it feeds to data mapping to generate I and Q signals to influence the four different phase carriers. The output was selected by multiplexer, which provides a digital QPSK signal.

2.2 Carrier Phase Shifter

The carrier signal is the critical element in the design of the digital modulator, which affects the efficiency and the performance of the modulator. For a robust modulator design in digital techniques, the errors [9]and delay in carrier signals are most important in the design. The carrier phase shifter was programmed with VHDL code in structural design. The carrier phase acquires four discrete states (0°, 90°, 180°, and 270°).This corresponds to mapping of I and Q data source generated with VHDL code. The RTL for the carrier phase shifter are shown in Figure 4.1.

2.3 RTL Schematic and Simulation Results

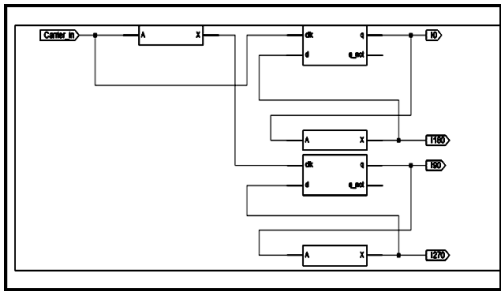

Figure 2.1: RTL schematic for carrier shifter

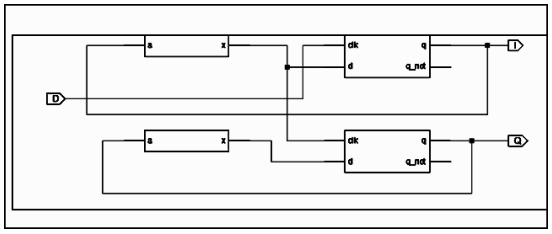

Figure 2.2: RTL schematic for data mapping

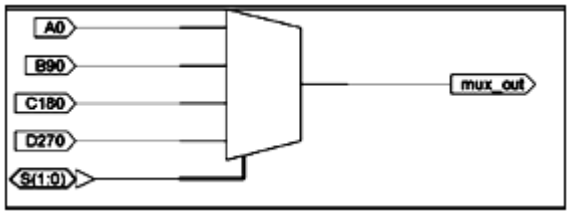

Figure 2.3: RTL Schematic for multiplexer

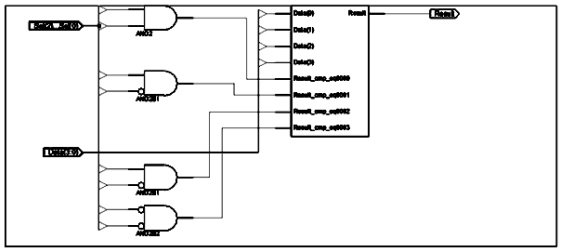

Figure 2.4 : Detail RTL schematic for multiplexer

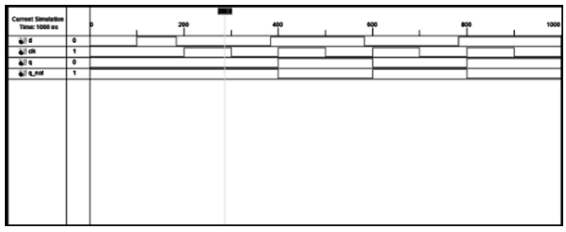

Figure 2.5: Simulation results for D-flip-flop

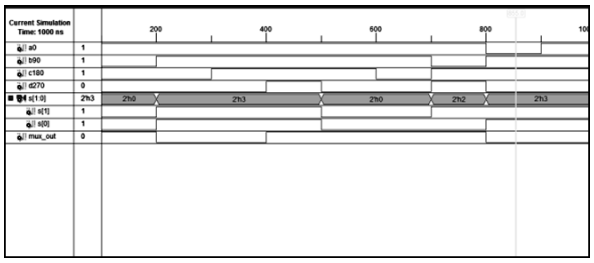

Figure 2.6: Simulation result for 4:1 multiplexer

3. CONCLUSION

In this paper, the modulator generate QPSK signal directly from binary digital data using VHDL programming. For test purpose it was generated with VHDL code, mapped for I and Q to control the carrier signal using VHDL multiplexer code. The implementation of QPSK digital modulator in VHDL its corresponding RTL has been studied. The simulation results for the synthesis of the carrier shifters suffer from the delay in signals. However, the delay time is critical in the inverted shift signals (180º) and (270º), as this delay affects the transition of the output signal for the modulator. This delay was due to the use of two discrete inverters of the carrier in the waveforms. In the future works, the proposed QPSK modulator will be implemented on the Spartan 3E Starter Kit.

It can also be designed by FPGA/CPLD and Altera development kit. The design has been written in the VHDL programming code by Xilinx software. After implementing the QPSK modulator, I want to realize a QPSK system. The system will consist of a modulator and demodulator and the signal from the modulator to demodulator will pass through a channel affected by AWGN. The modulated and demodulated signals will be also routed to VGA monitors, but also to oscilloscopes. This technique also offers high transfer rate for biomedical devices requiring a high demand rate, such as electrodes information measured in real-time, where the acquisitions data from electrodes are increasing from the neural system. Also this technique can be used for biomedical telemetry applications for increasing the data rate with low noise and size reduced.

4. ACKNOWLEDGMENTS

First of all, I would like to express my deep sense of respect and gratitude towards my advisor and guide Prof.(Dr)Aruna Tripathy who has been the guiding force behind this work.. For timely guidance I would like to express my gratitude towards Prof.(Dr.)P.KabiSatpathy and Er.Ananya Dastidar for their kind encouragement and cooperation and moral Support. I would like to thank all faculty members and staff of the Department who have willingly helped me out with their abilities and also for their generous help in various ways for the completion of this thesis.

5. REFERENCES

[1] D. a. G. u. N. b. Arogyaswami j. Paulraj, "An Overview of MIMO Communications—A," in PROCEEDINGS OF THE IEEE invited paper, A. Paulraj, D. Gore, R. Nabar and H. Bolcskei.

[2] Y. Z. a. C. E. Saavedra, 2007 IEEE "Coherent BPSK Demodulator MMIC Using an Anti-Parallel," in Radio Frequency Integrated Circuits (RFIC) Symposium, Honolulu, HI.

[3] V. A.Pedroni,2010 Circuit Design with VHDL, Massachusetts, MIT press.

[4] S. palnitkar, 1996 Verilog-HDL A guide To Digital Design and snthesise, pearson.

[5] Y. H. ,. S. M. Shihong Deng, 2006 IEEE"A high data rate QPSK demodulator for inductively powered electronics implants," in ISCAS, Island of Kos .

[6] G. C. J. N. Gihad Elamary, 2009 "A Simple Digital VHDL QPSK Modulator Designed Using CPLD/FPGAs for Biomedical Devices Applications," in World Congress on Engineering, London, U.K..

[7] G. wade, 2006 Coding Techniques: An Introduction to Compression and Error Control, Palgrave Macmillan.

[8] I. J. a. B. H. Meuth, 2002 "Numerically controlled oscillators with hybrid function generators," Ultrasonics, Ferroelectrics and Frequency Control .

[9] S. K. Kaul, 2005 "QPSK, OQPSK, CPM probability of error for AWGN and Flat Fading Channels," in Wireless Communication Technologies.