Low Power High Speed 64 Bit SRAM Architecture using SCCMOS and Drowsy Cache Concept

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ABSTRACT
With the development of technology with each passing days, the demand for low power, high speed, high density memory for portable devices is increasing proportionally. The power consumption and battery life has become the major concerns for VLSI industry. But as the technology scales down it gives rise to an unwanted parameter i.e., the leakage power which according to International technology roadmap of semiconductors (ITRS) will dominate the majority part of the total power consumption .In this paper a complete 64 bits SRAM array is designed using the leakage power reduction techniques .2 techniques are being combined which are sleep stack with keeper and other is the drowsy cache including the SCCMOS concept .The array is designed and simulated using cadence gpdk 180nm technology .The results show that the total power consumption has reduced by nearly 40% for 1 bit SRAM along with its peripherals

Keywords: Sleep Stack With Keeper, Drowsy Cache, SCCMOS, Data Retention Voltage, low power SRAM

1. INTRODUCTION
Low power is gaining its importance in today's VLSI industry since battery life has become the subject of concern .The demand for high density, high speed low power memory has lead to integration of large number of CMOS transistors/functional blocks on a single SOI. All the blocks are not active all the time if active only for small fraction of time. Observing this ,for reducing the standby/idle power dissipation , static power & total power consumption the supply voltage is scaled down .Leakage occurs even if the functional block is not operating. In submicron technologies, this phenomenon is becoming prominent by the threshold voltage reduction due to scaling. Total power consumption is comprised of nearly 50% leakage power in today's high performance devices and this leakage power dominance percentage increases with technology scaling .Hence reducing the leakage power is directly related to low power design .But reducing the supply voltage alone is not just enough to reduce the power consumption .While scaling down the supply voltage it should be kept in mind that the output or logic state of the circuit is not disturbed & the stability of the circuit is maintained.

In this paper SCCMOS sleep stack with keeper approach along with the drowsy cache scheme is being implemented to reduce the total power including the leakage power & achieve high speed performance. SCCMOS sleep transistors are used instead of high threshold voltage sleep transistors to overcome the delay overhead problem caused by high threshold voltage sleep transistors .

Section 2 contains a gist of the techniques used in the paper & their advantages over other available low power techniques. Section 3 describes the operation of the proposed SRAM cell along with all the other peripherals required for its proper working. Section 4 presents the simulation & comparision results and Section 5 ends up with the conclusion part.

2. LITERATURE SURVEY
2.1 Survey on Standby Mode Leakage Reduction Technique
Battery life remains idle for long period except when in use and drains off most of the power, which in turn reduces the battery life. Thus battery life can be saved by shutting it down from the supply rails when it is not in use .There are various techniques to adjust the threshold voltage of a transistor in order to control its operation & hence the total power consumption [1-3].

1) ***MultiThreshold CMOS Technique(MTCMOS)*** *:*
MTCMOS technique uses high threshold voltage transistors that are connected in series between the supply power and the circuit. During the active mode the sleep transistors are ON, allowing the normal operation to take place by creating a direct path between the power supply and ground. During the standby mode, Sleep transistors are OFF, generating a virtual path between the power supply and the ground. [4]

2) ***Super Cut-off CMOS (SCCMOS) [12]:***
The concept of SCCMOS is similar to MTCMOS power gating but the only difference is that the sleep transistor used have the same standard low Vth like the transistors used in the logic circuit .In standby mode the SCCMOS sleep transistors are either over driven or under driven which maintains the standby leakage mechanism. This concept helps to reduce the additional delay introduced by the high transistors threshold voltage sleep transistors in the active mode. [5]

2.2 Survey on Active Mode Leakage Reduction Technique
Various design approaches for reducing the sub-threshold leakage power reduction are being proposed in the past.Among them the most well known approaches are [7 - 12]:-

1) ***Sleep approach :***
Here both an extra "PMOS sleep" transistor is placed between VDD and the pull-up network and a "NMOS sleep" transistor is placed between the pull-down network and GND. The role of these sleep transistors is to cutoff the power supply to turn off the circuit during standby/idle

mode. The sleep transistors turn on during active mode to provide power supply for normal operation .As power supply is cutoff leakage power is reduced effectively .However, after the sleep mode ,the output will be in floating state so the technique resulting in destruction/instability of state .

2) ***Stack technique*** : This is the approach, which forces a stack effect by breaking down an existing transistor into two half size transistors. When the two transistors are turned off together ,the generated reverse bias between the two transistors results in sub-threshold leakage current reduction.

3) ***Sleepy stack technique*** **:** This approach fuses both the methods of sleep and stack [6-7]. It breaks the original transistors, like the stack approach, into 2 half size transistors. Sleep transistors are then parallelely added to one of the divided transistors. During idle mode, sleep transistors are off and the stacked transistors reduce the leakage current while saving the state. The sleep transistor, parallelely placed along with stack transistors, helps in reducing the path resistance, resulting decrease in delay in active mode. But, area penalty is a significant matter for this approach since every transistor is replaced by three transistors

4) **Sleepy keeper approach** – As it is known that PMOS can't pass good '0' & NMOS can't pass good ' 1 'But to maintain a stored value/data during standby mode when the traditional PMOS & NMOS sleep transistors are turned off a keeper circuit is required .The role of keeper is being played by a NMOS /PMOS transistor connected to VDD/GND& placed parallel to the PMOS/NMOS sleep transistors respectively. Depending upon the stored value, additional NMOS & PMOS transistors placed in parallel to the pull-up & pull down sleep transistors connects the logic circuit to the requisite power rail i.e., NMOS to VDD & PMOS to GND respectively as they act as the only source of power rails to the circuit.

5) **Drowsy Cache -** SRAM cell has 2 modes of operation namely active & standby/idle modes. Active mode includes both read & write operation. Whereas during the standby mode the data preservation is performed by the 2 back to back connected inverters in the SRAM cell .It is found that low Vdd is enough for preserving the data/information in a SRAM memory cell during the standby mode [8]. This method of drowsy cache provides a low Vdd to the memory cell during standby mode for preserving/holding the data . This method utilises multiple Vdd sources .High Vdd is supplied only during active mode of operation. As supply voltage is scaled down it results in reduced leakage current & hence reduced leakage power [8]. Hence the memory cell is put in the low-power drowsy mode when the information preservation is required and in the high-power mode before the access of the contents [9].

The goal of this paper is to achieve the benefit of all the above described techniques. So "sleep stack with keeper" along with the ' drowsy cache ' approach is being considered for designing the SRAM cell which reduces leakage current which in turn helps to reduce the total power consumption while saving exact logic state.

3. PROPOSED SRAM CIRCUIT

3.1 Conventional SRAM

Conventional SRAM cell has 6 transistors [5-6] as shown in the figure- 4 NMOS & 2 PMOS transistors. P1, N1, & P2, N2 form a pair of cross-coupled inverters that store a value by positive feedback loop. Transistors N3 and N4 are the 2 access transistors that helps to access the storage nodes to read from /write into the memory cell only during the active mode. The bit line pair of a memory cell has to be previously precharged to VDD by the precharge circuit before any write or read operation. Data is written into the cell through the write- drive circuit when WE signal alongwith WL signals are high .Similarly data is read only when WE is low, SE/RE & WL signals are high. The bit line capacitances play a major role in determining the data stored in a memory cell. If data '1' is written into the cell then BL will remain close to VDD while BLB will discharge & similarly during data '0' BL discharges while BLB remains near VDD. This differential voltage generated on the bit lines will be sensed by the sense amplifier whose role is to convert the small voltage difference generated on either of the bit line that discharged to appropriate full logic level during the read mode.

During the stand-by mode WL is disabled & the access transistors are denied access for any data transmission. Hence during the idle mode the data is only stored/ preserved for future needs.

SRAM transistors must be sized carefully for its proper operation keeping in mind-

Cell Ratio = (W1/L1) / (W3/L3) (At Read Mode)

Pull up Ratio = (W2/L2)/(W4/L4)(At Write Mode)

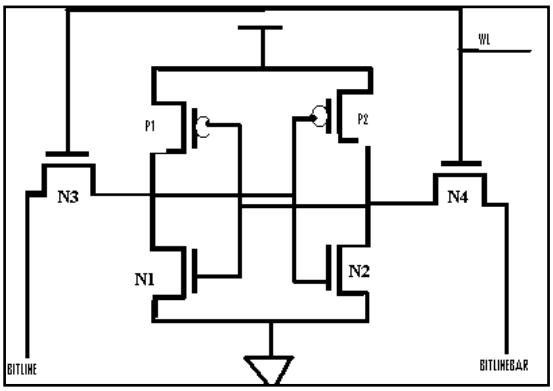

Fig. 1 Conventional 6t SRAM Cell Schematic

3.2 Proposed Circuit

The proposed circuit is being shown in Fig.2.

Here the original P1,P2 transistors of width W are broken down into 3 transistors each of width W/2 namely P1, PS1, PS2 P2, PS3, PS4 respectively. Similarly the NMOS transistors N1 & N2 are also stacked. Stacking results in the increased reverse bias between the transistors in off state thus reducing the sub-threshold leakage power. The transistors named NK1, NK2 are the NMOS keeper & PK1, PK2 are the PMOS keeper transistors. During the stand-by mode, NK1 & NK2 serve as the ultimate source to connect VDD with the logic circuit while PK1, PK2 connect logic circuit to GND thus the stored values will remain enact without distortion .Hence using keeper transistors help to preserve the data in idle/hold mode. Instead of high threshold voltage sleep transistors,

SCCMOS sleep transistors are being used so as to simultaneously better speed & low power consumption can be achieved. Drowsy cache concept comes into role when we provide power supply to the memory cell. During active mode P3 in on & provides full VDD supply to the circuit for read & write operation but during standby mode N5 is on & P3 is off. P4 & P5 are stacked & used to divide the VDD supply into half instead of using multiple supply voltages. The near ½ VDD provided by the drains of P4 & P5 is transmitted to the circuit by N5 during the stand-by mode .Since retention of data can be done with low VDD so data will be preserved even at ½ VDD supply in the idle mode.

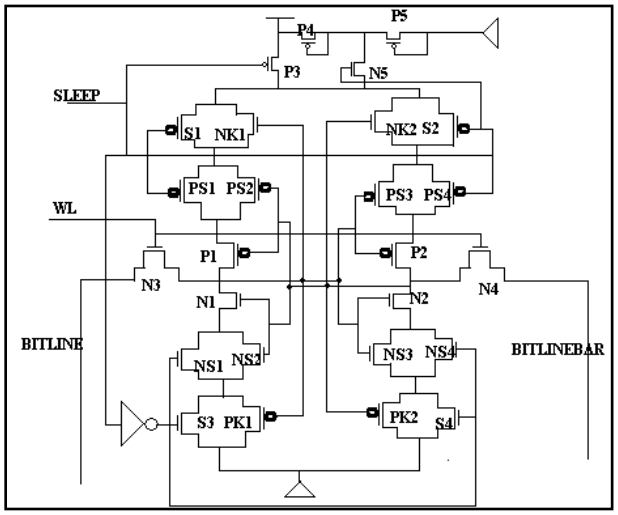

Fig. 2 Proposed SRAM schematic

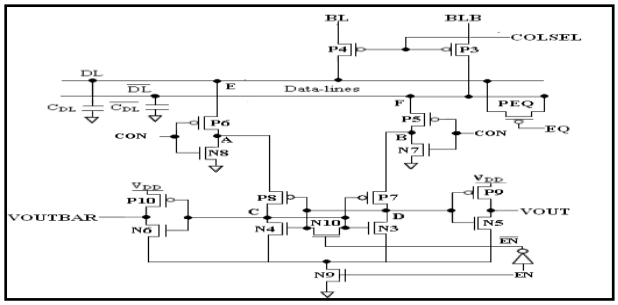

Fig. 3 Shows The Modified Sense Amplifier used with the proposed SRAM

4. SIMULATION & RESULTS

The conventional SRAM, modified SRAM & the 8x8 SRAM array are being designed & simulated using cadence gpdk 180nm technology. The comprising conditions for all the 3 designs are the same with VDD = 1.8V, temperature = 25^0C, $C_{BL} = C_{DL}$= 1pF,C_L = 0.1pF.

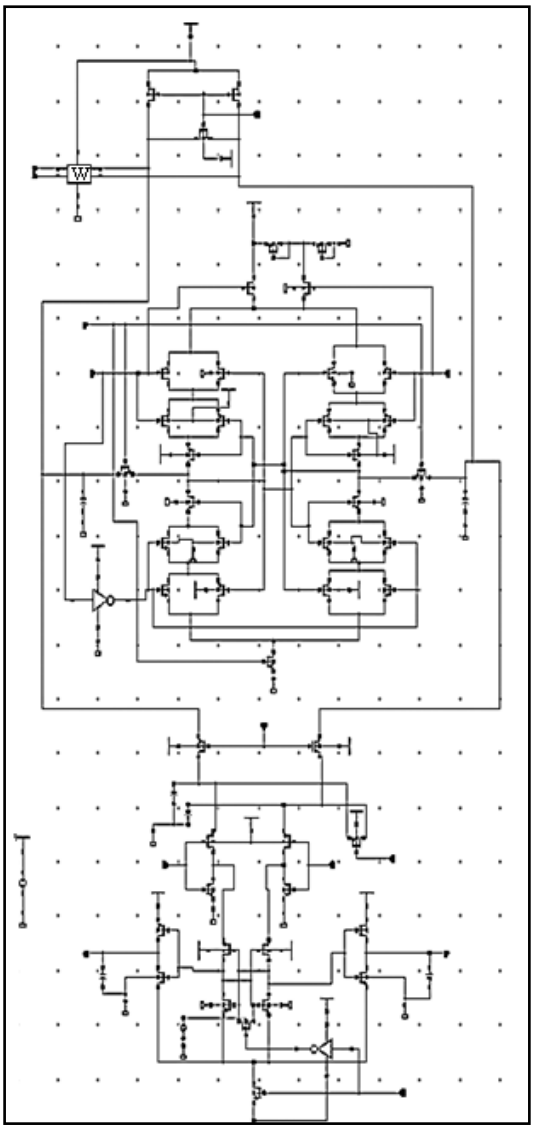

Fig. 4 The Modified SRAM Schematic With Precharge , Write Drive ,Sense Amplifier Circuits

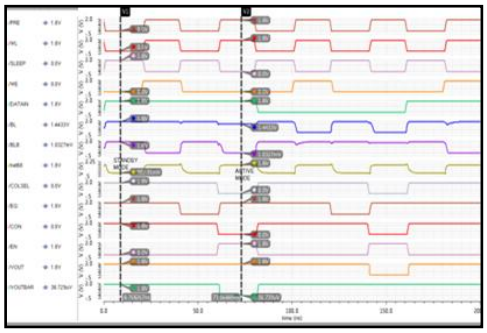

Fig. 5 Graph Showing VDD Supply During Active & Idle Mode

From fig. 5 we can see that during the active mode full VDD i.e., 1.8V power supply is being provided to the circuit while during the stand-by mode nearly 0.9V is being provided .It can be seen from the graph that data is not hampered in the stand-by mode even if 0.9V is supplied.

Fig. 6 shows write-read result for data '1' & data '0'.

We can see that before every read & write the bit lines are precharged to VDD. For write operation precharge, WE,WL are high but all the sense amplifier control signals are intentionally turned off to save power consumption. But during read operation the sense amplifier control signal are turned on as required & the output of sense amplifier indicates the data stored in the memory cell.

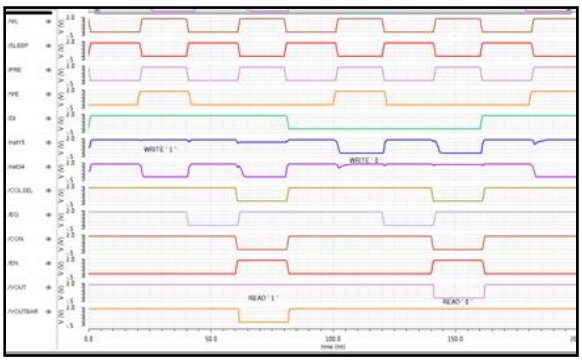

Fig. 6 Result Waveform for Data '1' & '0'

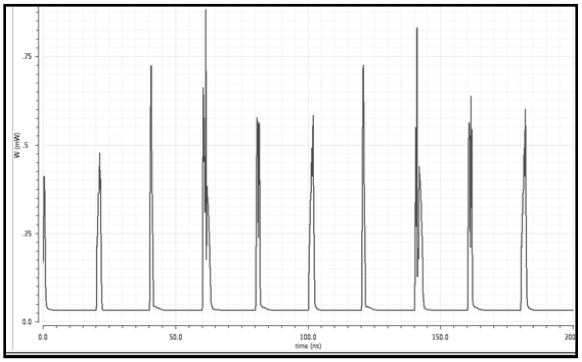

Fig. 7 Power Consumption Graph of 1 Bit SRAM with Peripherals

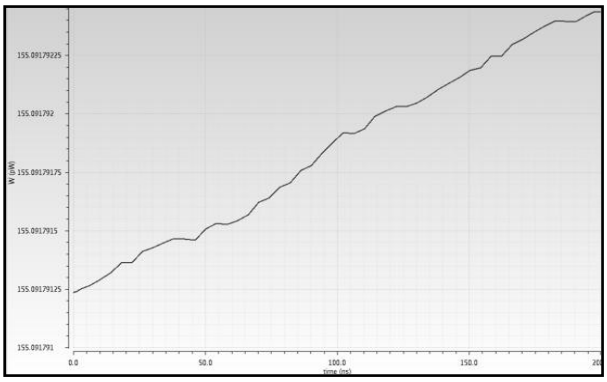

Fig. 8 Leakage Power Consumption of 1 Bit SRAM with Peripherals

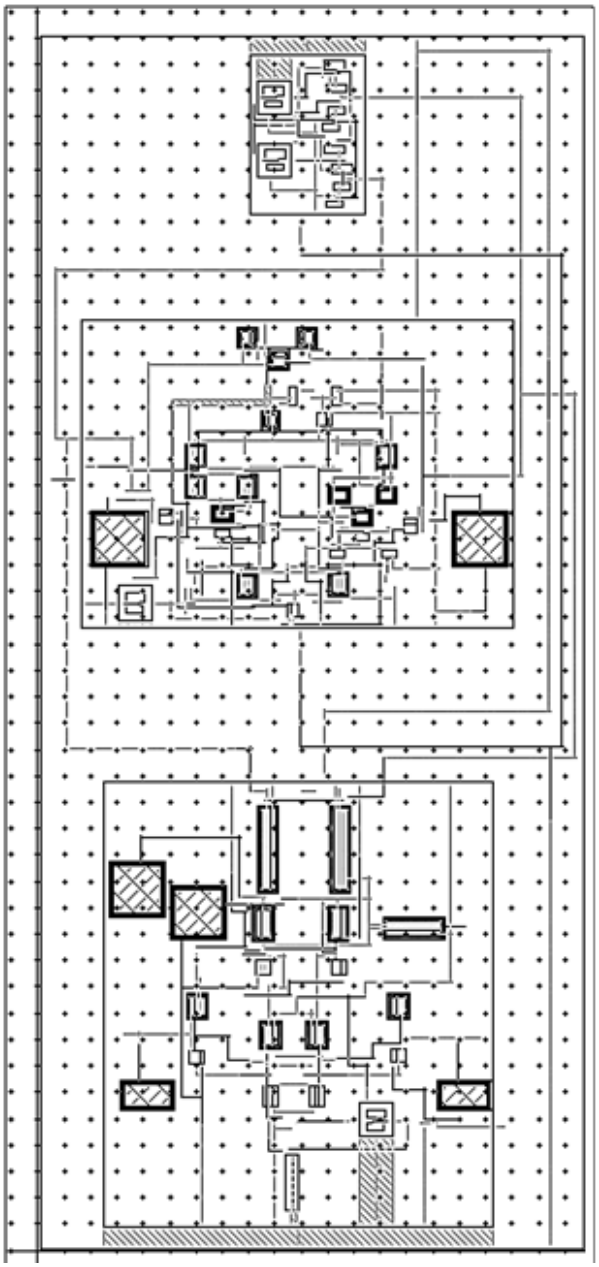

Fig. 9 Layout of 1 Bit Modified SRAM with Peripherals

Fig. 10 shows the 8x8 SRAM array .The array consists of a 3:8 address decoder that helps to enable the required word line. All the transistors in an enabled row are provided full VDD supply while all the rest of transistors are provided with ½ VDD as they were in standby mode.8 write drive circuits are used to provide 8 bit data- one block for each column. Similarly 8 precharge circuits – 1for each column are being used to precharge the bit line pair. But only 1 sense amplifier is being used for all the 8 columns in order to save area & power. Since only 1 bit will be activate at a time the control signals are provided strictly keeping in mind that they are not active undesirably resulting in distorted output.

Fig. 11 shows the output waveform of the 8x8 SRAM array for a input data of ''11001100".We can see that the sense amplifier output is obtained in the same pattern as the given input pattern.

Fig. 12 shows the power consumption of the 8x8 SRAM array

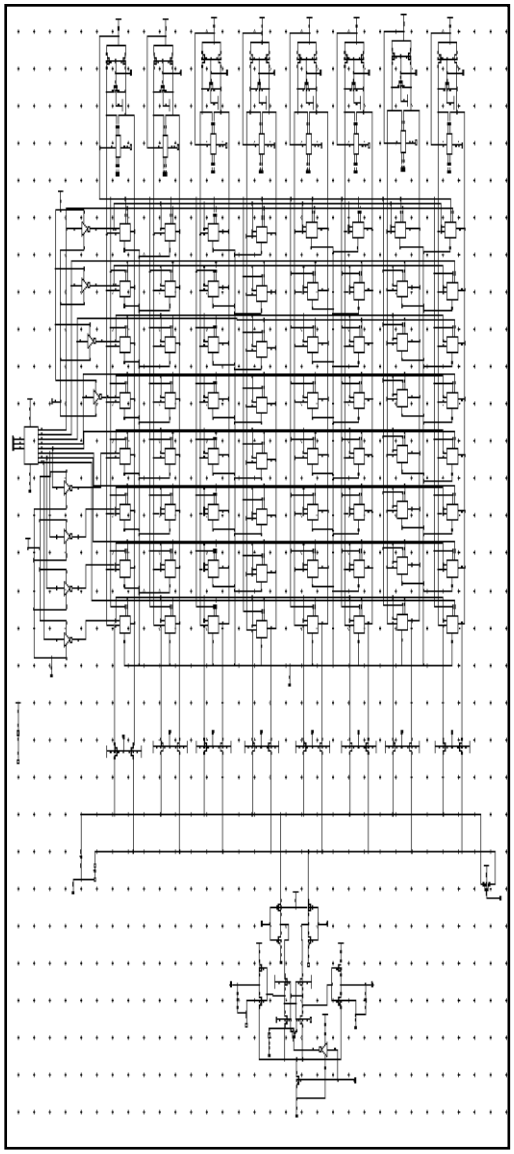

Fig. 10 8x8 SRAM Array

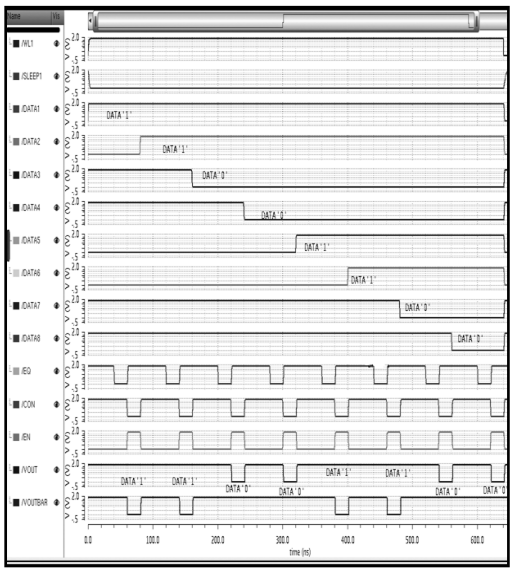

Fig. 11 output waveform for data "11001100"

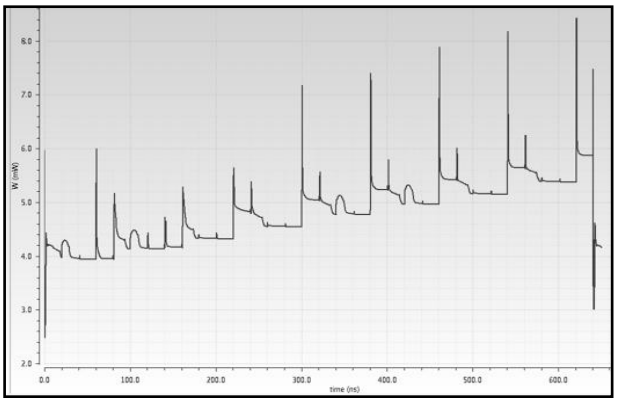

Fig. 12 Total Power Consumption Graph For 8x8 Sram Array

Table I

Comparision Table With Vdd=1.8V, C_{BL} = C_{DL} = 1pF & C_L = 0.1pF

Design	Read Delay in (ns)	Write Delay in (ns)	Total Power	Leakage Power
Conventional SRAM	0.96	12	125.4uW	111.5nW
Modified SRAM	0.79	11.89	53.92uW	155.6pW
8X8 SRAM	160	551	4.6mW	20uW

5. CONCLUSION

The paper presented a modified SRAM design using SCCMOS sleep transistors with stacking along with the keeper transistor and drowsy cache concept .The sleep stack keeper concept helps to reduce the leakage power during the active mode operation while the drowsy cache concept helped to reduce the leakage power during the standby mode .Hence we can conclude that by implementing both concepts together the total power can be reduced along with the leakage power. The design proves much better by using SCCMOS sleep transistors instead of MTCMOS or VTCMOS sleep transistors. The delay overhead added by MTCMOS or VTCMOS is reduced by SCCMOS transistor. It is found that the modified design consumed nearly 40% less power & delay is also reduced when compared to conventional SRAM.

6. ACKNOWLEDGMENT

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