An Approach to Design Different Weighted Code Synchronous Counters by the Sequential Circuit Elements of Reversible Gates

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ABSTRACT

In recent years, reversible logic has emerged as a promising computing paradigm showing its applications in various fields like low power computing, quantum computing, nanotechnology, optical computing and DNA computing. This paper proposes different sequential circuit elements of reversible gates and its application in the designing of different weighted counters. These synchronous reversible counters provide the initial threshold to build the more complex system having reversible sequential circuits as a primitive component and which can execute more complicated operations using quantum computers. Since the output of a sequential circuit depends not only on the present inputs but also on the past input conditions, the construction of sequential elements using reversible logic gates is quite complex than that of a combinational circuit. This paper proposes reversible D flip flop, JK flip flop, T flip flop and also represents 4 bit BCD 8421 weighted code synchronous counter, 842'1' weighted code synchronous counter, 3321 weighted code synchronous counter and 4221 weighted code synchronous counter using the proposed reversible T flip flop . A comparison between these designs in terms of garbage output, number of gates, constant input and total logical calculation also has been made.

General Terms
Reversible logic, Reversible memory elements, Architecture

Keywords
Quantum computing, Nanotechnology, Optical computing, DNA computing, Reversible gates, Flip Flop, Synchronous counter.

1. INTRODUCTION

This Reversible computing is defined as performing computation in such a way that any earlier state of the computation can always be reconstructed by giving a depiction of the current state. This kind of computation is known to be "reversible" as the reconstruction of previous states could be applied to allow rolling backwards through a sequence of states, in a time-reversed manner. In 1961 reversible logic was primarily related to energy by Landauer and he stated that losing of a bit in digital circuits' causes a smallest amount of heat dissipation. And the theoretical limit of heat dissipation for losing of one bit computation would be KTln2 [1] where K is Boltzmann's constant and T is the temperature. Afterward Bennett told that KTln2 joules of energy dissipation can be avoided in a circuit by using reversible logic gates [2]. In 1965, Gordon. E. Moore [3] predicted that the numbers of components on the chip will double every 18 months which is known as Moore's law. At first he predicted only for 10 years but due to growth in the integrated-circuit technology his prediction is valid till today. The effect of Moore's law was carefully studied and researchers have made the conclusion that as the number of components in the chip increases the power dissipation will also increase enormously. Hence power minimization has become an significant matter for today's designing area of VLSI. The main motive of designing reversible logic is to reduce quantum cost, depth of the circuits and the number of garbage outputs.

In reversible circuits number of inputs and outputs must be equal. Research is going on reversible logic and a good amount of research work has been carried out in the area of reversible combinational logic. However, the limited work in the area of sequential circuit like flip-flops and counters yet has been done. A flip-flop or latch is a circuit having two stable states which can be used to store state information. A counter is a sequential circuit capable of counting the number of clock pulses that have arrived at its clock input. In 2005, H. Thapiyal [4] have constructed T flip-flop using basic reversible gates. Again, in year 2006, this design of reversible T flip-flop was improved by SKS Hari [5]. Compared to the design proposed by H. Thapiyal [4], Min-Lun Chuang [6] designed an improved T flip-flop by using D and T latches in 2008. In year 2010, a new reversible gate, Sayem Gate was proposed by Abu Sadat, and Md. Sayem [7] and D, J-K latches were designed using Sayem Gate and basic reversible gates. In 2011, V. Rajmohan [8] have proposed T flip-flop using Sayem Gate and basic reversible gates.

2. REVERSIBLE LOGIC
A reversible logic function can be defined as the function for which each input vector maps to a unique output vector. From the particular outputs, it is always possible to find out back its input in case of reversible function, because there is a one-to-one relationship between the input and output states. For an N X N reversible logic gate the inputs are denoted by $I_1\ I_2\ I_3\ \ldots\ I_N$ and the outputs are denoted by $O_1 O_2 O_3 \ldots O_N$. Some of the vital basic reversible logic gates are Feynman gate [9] which is the only 2*2 reversible gate. Toffoli gate [10], Fredkin gate [11], Peres gate [12] are 3*3reversible gates all of which shown in fig.1 can be used to realize important combinational functions.
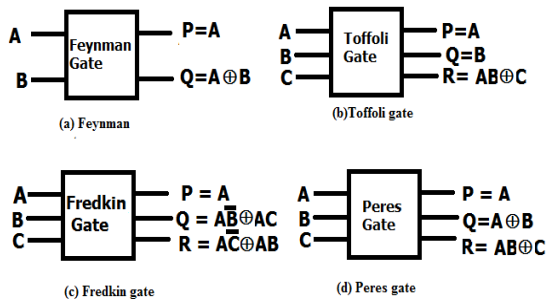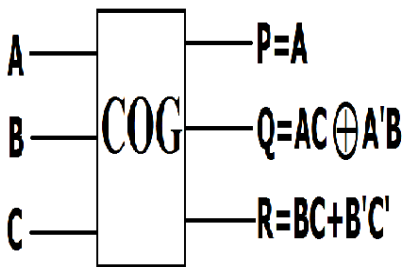
Fig 1: Reversible gates.

A reversible logic circuit should have the following features [13]: Use least number of reversible gates, garbage outputs and constant inputs. The inputs, outputs, garbage outputs and constant inputs of a reversible gate are interrelated as follows.

Input + constant input = output + garbage.

The total logical operation of a reversible circuit [14] is considered by the collective number of AND operations, EX-OR operations and NOT operations. If α represents the number of EXOR operations, β denotes the number of AND operations and δ represents the number of NOT operations then the total logical operation is expressed as the sum of EX-OR, AND and NOT operations required for a specified circuit and is given in terms of α, ß and δ.

3. COG REVERSIBLE GATES AND REALIZATION OF ITS CLASSICAL OPERATION

A reversible gate COG (Controlled Operation Gate) logic shown in fig.2 already had been proposed [15]. The truth table for the corresponding gate is shown in Fig 2 also .The closer look at the truth table shows the input pattern and corresponding specific output pattern. The inputs can be uniquely determined from the outputs maintaining the one-to-one correspondence between the input vector and the output vector. In this gate the input vector is given by $I_v = (A, B, C)$ and the corresponding output vector is $O_v = (P, Q, R)$.

COG reversible gate

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	1	0
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	0	1
1	1	0	1	0	0
1	1	1	1	1	1

Truth table of COG gate

Fig 2: Reversible COG gate & its truth table.

Implementation of the conventional digital gates can be possible [19] by using the COG reversible gate. Implementation of the AND, NOT, NAND, NOR, EXOR, EXNOR, OR and COPYING operations are possible (See Figure 3). All the above specified operations can be get by setting the input values as per the requirement.
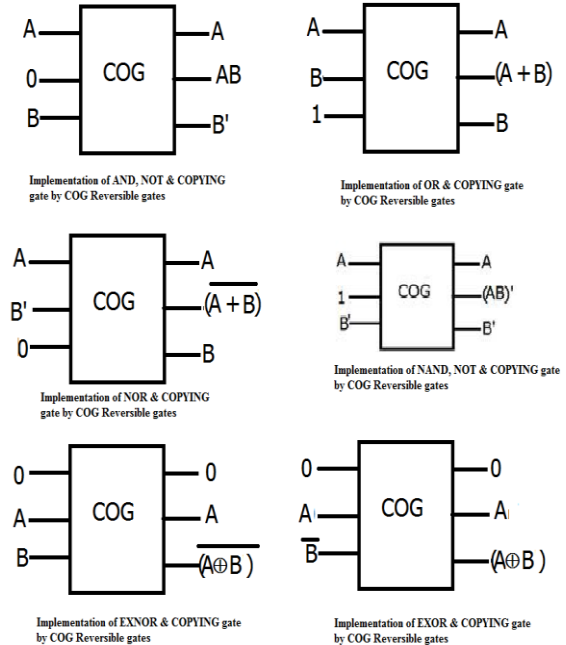

Fig 3: Classical operations using COG gate

4. DESIGNING OF SEQUENTIAL CIRCUIT ELEMENTS USING COG GATES

In this paper designing of flip-flops which can be defined as the basic circuit elements of the sequential circuit has been proposed by using COG reversible gates and a comparison also has been drawn with the existing designs reported in the literature. The characteristic equation of the D Flip-Flop is given as Q(t)=D. The D Flip-Flop without complement output is shown in fig 4. which requires only one COG gate whereas D Flip-Flop with complement output is shown in fig 5. requires only one COG gate and one Feynman gate. The characteristic equation of the J-K Flip-Flop is given as Q(t)=JQ'+K'Q. The J-K Flip-Flop with complement output is shown in fig 6. which requires two COG gates along with one Feynman gate. The characteristic equation of the T Flip-Flop is given as Q(t)=TQ'+T'Q. The T Flip-Flop with complement output is shown in fig7. It requires two COG gates only.
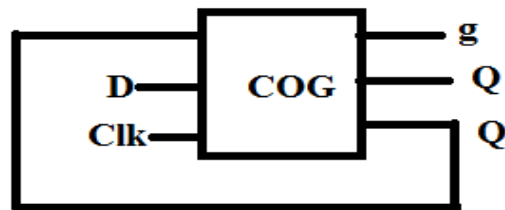

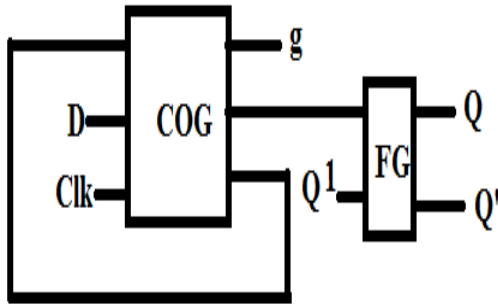**Fig 4: D Flip-Flop using COG reversible gate without complement output**

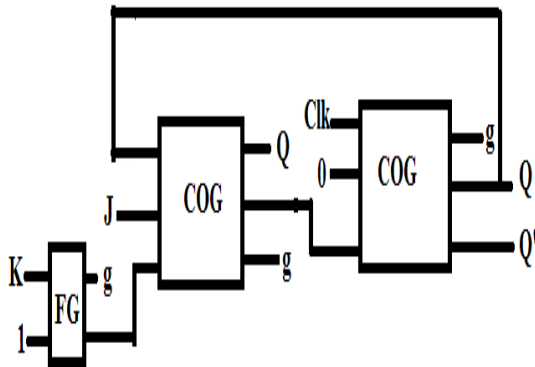**Fig 5: D Flip-Flop using COG reversible gate**

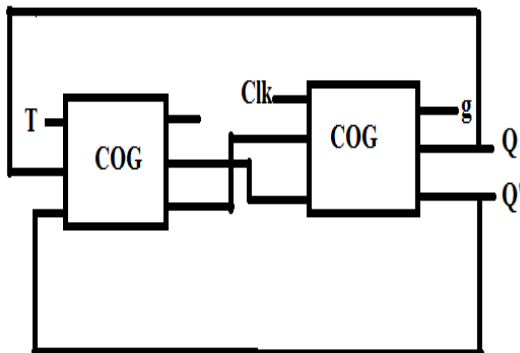
Fig 6: J-K Flip-Flop using COG reversible gate

Fig 7: T Flip-Flop using COG reversible gate

5. DESIGNING OF VARIOUS 4 BIT SYNCHRONOUS WEIGHTED COUNTER

This paper represents the designing of various 4 bit synchronous weighted counters using the reversible sequential elements of reversible gate. Mainly all the designs are made with the proposed reversible T Flip-Flop. As all the proposed counter designs here are the state skip counters, some additional circuitry are needed for faithful implementation of the required circuits. The expression for additional circuitry can be decided from the transition table of each counter. Also in all the designs the clock pulses have been applied simultaneously to all the required flip-flops as because of the synchronous counters have to be designed.

5.1 Designing of BCD 8421 Weighted Code Synchronous Counter using T Flip-Flops

For the designing of 4 bit BCD 8421 weighted code synchronous counter using T Flip-Flops, determination of the inputs of the T Flip-Flops is necessary. So from the output states of the required counter, the transition table related to T inputs can be drawn. The counter counts 0000 - 0001- 0010-0011- 0100 - 0101- 0110 - 0111-1000- 1001-0000.In this counter the states like 1010,1011,1100,1101,1110 and 1111 are skipped .The transition table is shown in Table 1.

Table 1. Transition table for T flip-flops to design BCD 8421 weighted code counter

Output		States		Flip –Flop Inputs			
Q_3	Q_2	Q_1	Q_0	T_0	T_1	T_2	T_3
0	0	0	0	1	0	0	0
0	0	0	1	1	1	0	0
0	0	1	0	1	0	0	0
0	0	1	1	1	1	1	0
0	1	0	0	1	0	0	0
0	1	0	1	1	1	0	0
0	1	1	0	1	0	0	0
0	1	1	1	1	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
0	0	0	0				

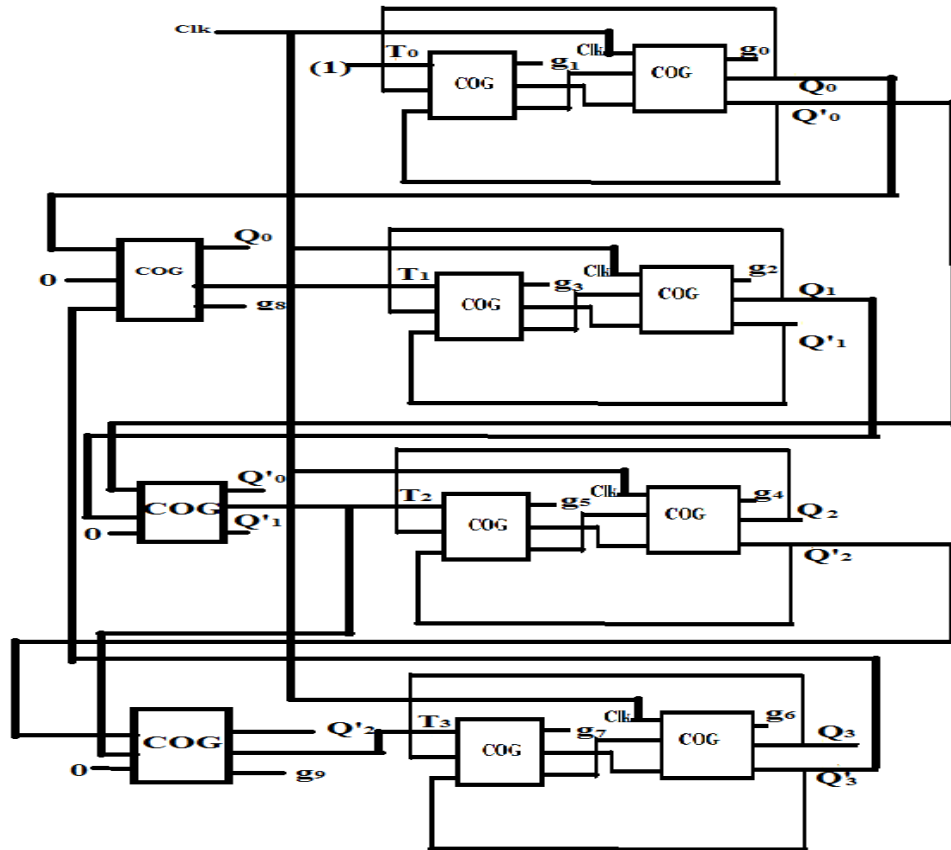From the transition table the T inputs have been calculated as

$T_0=1$

$T_1=Q'_3Q_0$

$T_2=Q_1Q_0$

$T_3=Q_2Q_1Q_0$

The circuit of 4 bit BCD 8421 weighted code synchronous counter using T Flip-Flops is shown in fig8. Total eleven COG gates are required for the designing. The number of constant inputs and garbage outputs are four and ten respectively.

BCD 8421 weighted code counter

Fig 8: BCD 8421 weighted code synchronous counter using Flip-Flop using COG reversible gate

5.2 Designing of 842'1' Weighted Code Counter using T Flip-Flops

For the implementation of 4 bit 842'1' weighted code synchronous counter using T Flip-Flops, determination of the inputs of the T Flip-Flops is required. So from the output states of the required counter, the transition table related to T inputs can be drawn. The counter counts 0000 - 0111- 0110-0101- 0100 - 1011- 1010 - 1001-1000- 1111-0000.In this counter the states like 0001,0010,0011,1100,1101 and 1110 are skipped .The transition table is shown in Table 2. From the transition table the T inputs have been calculated as

$T_0=1$

$T_1=(Q_3Q_2+Q'_0)$

$T_2=(Q_3Q_1Q_0+ Q'_2Q'_1Q'_0)$

$T_3=(Q_3Q_2+Q_2Q'_1Q'_0)$

The circuit of 4 bit 842'1' weighted code synchronous counter using T Flip-Flops is shown in fig 9.Total seventeen COG gates are required for the designing. The number of constant inputs and garbage outputs are ten and fourteen respectively.

Table 2. Transition table for T flip-flops to design BCD 842'1' weighted code counter

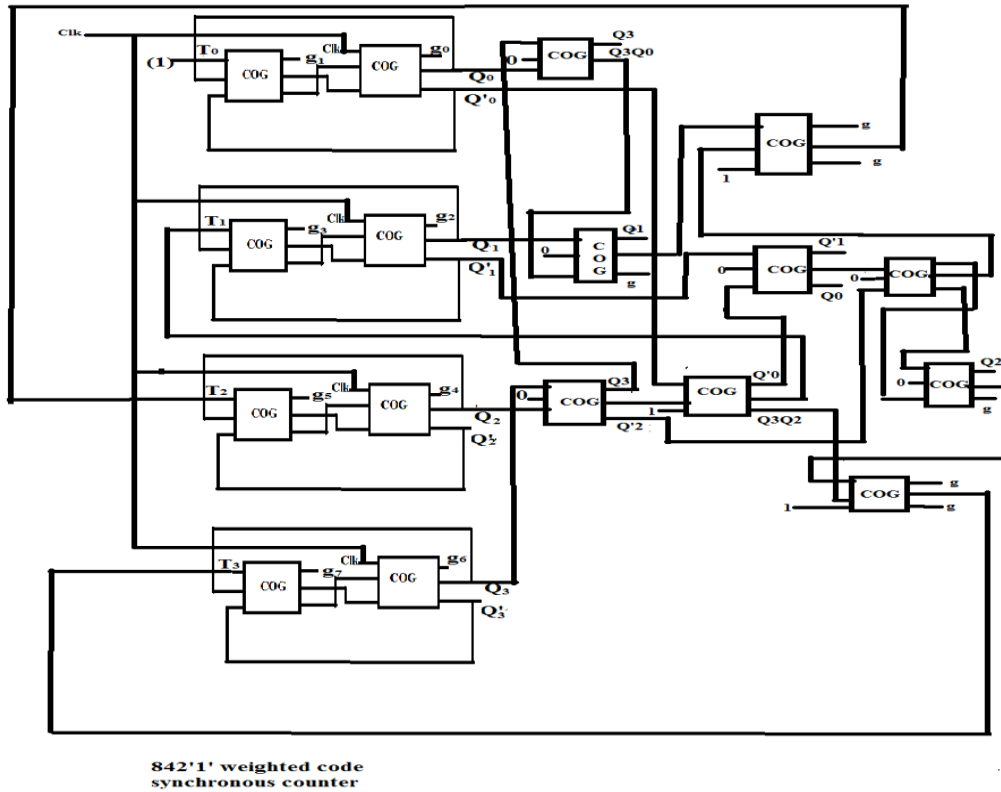| Output	States			Flip	–Flop	Inputs	
Q_3	Q_2	Q_1	Q_0	T_0	T_1	T_2	T_3
0	0	0	0	1	1	1	0
0	1	1	1	1	0	0	0
0	1	1	0	1	1	0	0
0	1	0	1	1	0	0	0
0	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0
1	0	1	0	1	1	0	0
1	0	0	1	1	0	0	0
1	0	0	0	1	1	1	0
1	1	1	1	1	1	1	1
0	0	0	0				

Fig 9: 842'1' weighted code synchronous counter using Flip-Flop using COG reversible gate

5.3 Designing of 3321 Weighted Code Counter using T Flip-Flops

For the designing of 4 bit 3321 weighted code synchronous counter using T Flip-Flops, determination of the inputs of the T Flip-Flops is necessary. So from the output states of the required counter, the transition table related to T inputs can be drawn. The counter counts 0000 - 0001- 0010-0100- 0101 - 1010- 1011 - 1101-1110- 1111-0000.In this counter the states like 0011,0110,0111,1000,1001 and 1100 are skipped .The transition table is shown in Table 3.

From the transition table the T inputs have been calculated as

$$T_0 = Q'_1 + Q_3 (Q_2 + Q'_0)$$

$$T_1 = (Q'_3 Q_1 + Q_0)$$

$$T_2 = Q_1 Q_0 + Q'_3 (Q_1 + Q_2 Q_0)$$

$$T_3 = Q_0 Q_2 (Q'_3 + Q_1)$$

The circuit of 4 bit 3321 weighted code synchronous counter using T Flip-Flops is shown in fig10. Total nineteen COG gates are required for the designing. The number of constant inputs and garbage outputs are eleven and seventeen respectively.

Table 3 . Transition table for T flip-flops to design BCD 3321 weighted code counter

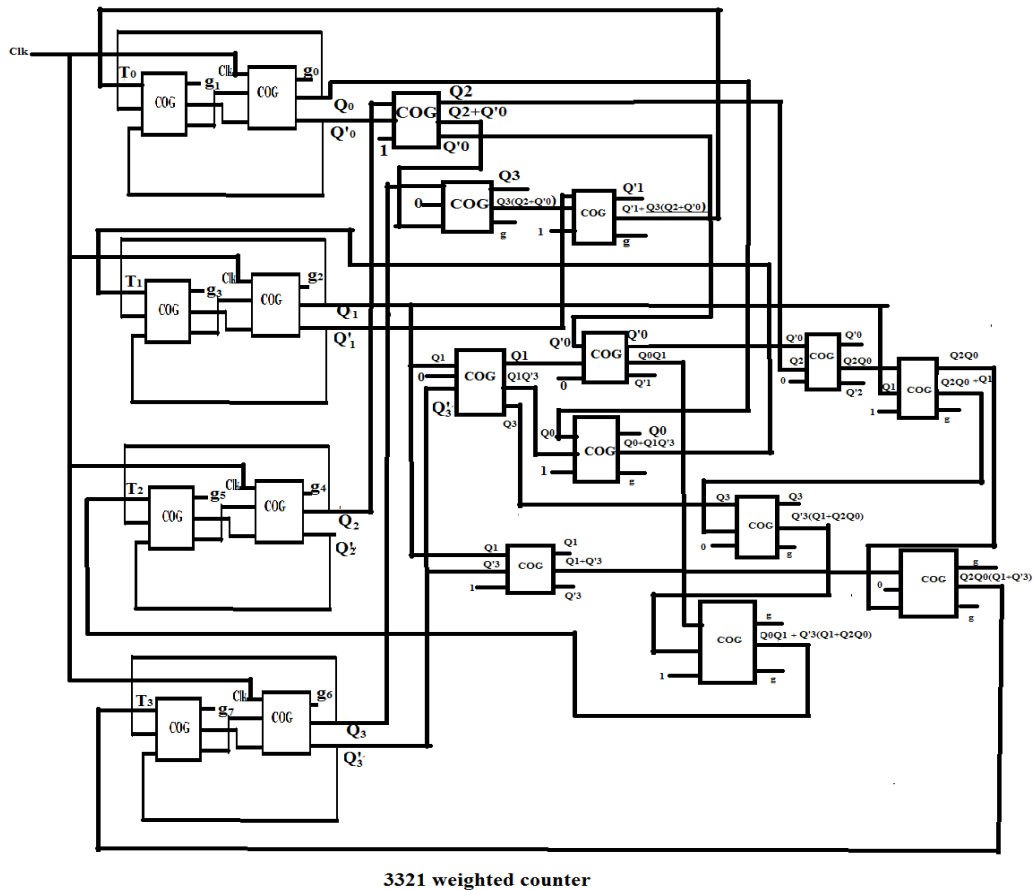| Output States				Flip –Flop Inputs			
Q_3	Q_2	Q_1	Q_0	T_0	T_1	T_2	T_3
0	0	0	0	1	0	0	0
0	0	0	1	1	1	0	0
0	0	1	0	0	1	1	0
0	1	0	0	1	0	0	0
0	1	0	1	1	1	1	1
1	0	1	0	1	0	0	0
1	0	1	1	0	1	1	0
1	1	0	1	1	1	0	0
1	1	1	0	1	0	0	0
1	1	1	1	1	1	1	1
0	0	0	0				

3321 weighted counter

Fig 10: 3321 weighted code synchronous counter using Flip-Flop using COG reversible gate

5.4 Designing of 4221 Weighted Code Counter using T Flip-Flops

For the designing of 4 bit 4221 weighted code synchronous counter using T Flip-Flops, determination of the inputs of the T Flip-Flops is necessary. So from the output states of the required counter, the transition table related to T inputs can be drawn. The counter counts 0000 - 0001- 0010-0011- 0110 - 1001- 1100 - 1101-1110- 1111-0000.In this counter the states like 0100,0101,0111,1000,1010 and 1011 are skipped .The transition table is shown in Table 4.

From the transition table the T inputs have been calculated as
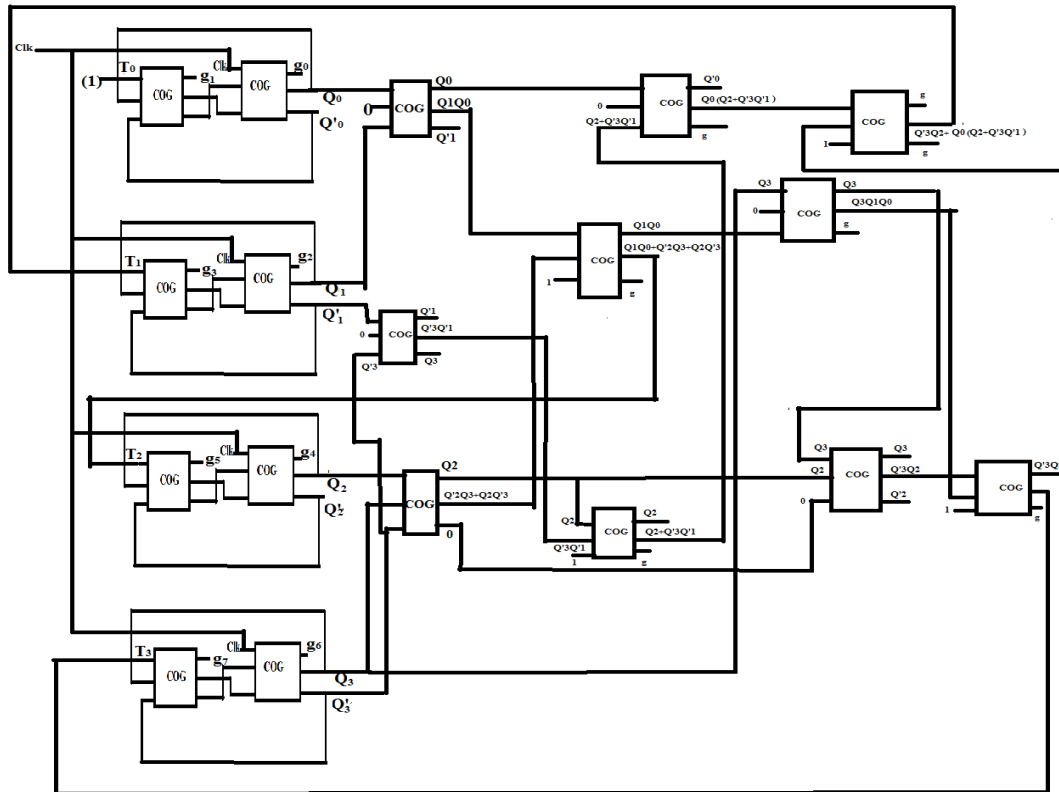
$T_0 = 1$

$T_1 = (Q'_3 Q_2 + Q_2 Q_0 + Q'_3 Q'_1 Q_0)$

$T_2 = (Q'_3 Q_2 + Q_3 Q'_2 + Q_1 Q_0)$

$T_3 = (Q_3 Q_1 Q_0 + Q_2 Q'_3)$

The circuit of 4 bit 4221 weighted code synchronous counter using T Flip-Flops is shown in fig11. Total eighteen COG gates are required for the designing. The number of constant inputs and garbage outputs are nine and fifteen respectively.

Table 4. Transition table for T flip-flops to design BCD 4221 weighted code counter

Output States				Flip –Flop Inputs			
Q_3	Q_2	Q_1	Q_0	T_0	T_1	T_2	T_3
0	0	0	0	1	0	0	0
0	0	0	1	1	1	0	0
0	0	1	0	1	0	0	0
0	0	1	1	1	0	1	0
0	1	1	0	1	1	1	1
1	0	0	1	1	0	1	0
1	1	0	0	1	0	0	0
1	1	0	1	1	1	0	0
1	1	1	0	1	0	0	0
1	1	1	1	1	1	1	1
0	0	0	0				

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4221 weighted counter

Fig 11: 4221 weighted code synchronous counter using Flip-Flop using COG reversible gate

6. COMPARISON RESULTS

Comparison results are made between the existing Flip-Flops and the proposed Flip-Flops. Table 5 shows the comparison result for D Flip-Flop, whereas Table 6 shows the comparison result for J-K Flip-Flop and Table 7 shows the comparison result for D Flip-Flop, in terms of number of gates, garbage output. Another comparison result between the counters presented in this paper is shown in Table 8 in terms of number of gates, garbage output, constant input and total logical calculation.

Table 5. Comparison of Different D Flip Flop

Design	No. of gates	No. of garbage output
Paper[16]	5	6
Paper[17]	2	2
Paper[18]	2	2
Proposed	1	1

Table 6. Comparison of Different J-K Flip Flop

Design	No. of gates	No. of garbage output
Paper[16]	4	8
Paper[17]	3	3
Paper[18]	4	4
Proposed	3	2

Table 7. Comparison of Different T Flip Flop

Design	No. of gates	No. of garbage output
Paper[16]	5	8
Paper[17]	2	2
Paper[18]	3	2
Proposed	2	2

Table 8. Comparison of Different 4 Bits Synchronous weighted Counter

Types of synchronous weighted counter	No. of gates	No. of constant input	No. of garbage output	No. of logical operation
8421	11	4	10	22 α+22ß+22 δ
842'1'	17	10	14	34α+34ß+34 δ
3321	19	11	17	38 α+38ß+38 δ
4221	18	9	15	36α+36ß+36δ

7. CONCLUSION

In this paper various reversible sequential circuit elements have been represented and also different weighted counters are designed using reversible COG gates. From the comparison results shown in Table 5, Table 6 and Table 7, it can be concluded that the proposed Flip-Flops are better in respect to the existing Flip-Flops. Various counters represented here are also compared in terms of number of gates, garbage output, constant input and total logical calculation shown in Table 8. Counters are the most important part in various field of real life applications. Thus for future research, efficient design schemes for reversible more complex sequential circuit is an interesting area to investigate. Alternate optimization methods are under investigation as a future work.

8. ACKNOWLEDGMENT

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