A High Speed CMOS Current Comparator in 90 nm CMOS Process Technology

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ABSTRACT
In this paper a current mode comparator is presented, more aptly can be called as the "Current Comparator". The proposed circuit consists of a current differencing stage which accepts two current inputs where one is the reference current and the other is the input current. The comparator stage outputs a rail-to-rail voltage depending on the difference of the two currents. Simulation of the proposed design is carried out in Cadence using EDA tool in 90nm technology. The operating speed of the current comparator was found to be 1.82GHz with an average power dissipation of 122µW. The high speed operation was confirmed by the transient analysis results in which the delay was found to be 0.55ns at an input current difference of ±1µA.

Keywords:
Current comparator, input current, current mode circuits, positive feedback, reference current

1. INTRODUCTION
Comparators form an essential building block for many electronic systems and have always been extensively used in ADC's. Unlike voltage mode comparators that compare two voltage signals, current comparators are basically used to compare two current signals. Some types of sensors such as the photo sensor, temperature sensors, etc produce output in the form of current signal and hence necessitate the use of current comparators. Moreover the latest advancements in current mode approach in terms of reduced chip area, operation over large bandwidth at reduced supply voltage and at the same time consuming less power makes the current mode approach to be suitably used in analog design.

D. Freitas and K. Current [1] proposed the first current comparator in 1983 that comprised of simple cascode current mirroring technique. The main limitations of this technique were reduced operational frequency and low resolution. Some satisfactory implementations have been reported in [2] - [4]. An ideal current comparator should posses a faster response time; consume less power, low input impedance and a rail-to-rail output swing. H.Traff proposed a novel design of current comparator in 1992 by implementing a positive feedback [2]. A source follower in the input stage and a CMOS inverter were used to effectively provide positive feedback that ultimately helps in lowering the response time alongwith the input impedance. Longer delay times and presence of deadband zone for small values of input current were the main drawbacks of Traff's comparator. The Traff's comparator has been modified since then as seen in works presented in [4] – [12]. The main motivation behind improving the performance of current comparators lays in the enormous demand for reduced power consumption, high speed and to be more specific the shrinking device sizes.

In this work, an enhancement to the Traff's current comparator is done by altering the gain stage which directly accounts for reduction in delay time. An additional current difference stage has been added in this new design which determines the difference of the two input currents which has been neglected in the previous earlier existing designs. The current difference stage also contributes to the power as well as delay of the current comparator. To refine the rail-to-rail output swing another CMOS inverter has been added in the output stage. Simulations of the proposed design were carried out in *Cadence* environment in 90nm technology. Performance parameters like delay, power and slew rate were determined using the EDA tools available in *Spectre* simulator. In this paper Section II describes the basic current comparator concepts; the proposed design is presented in Section III followed by simulation and results in Section IV. Finally in Section V the conclusion of the work is presented.

2. CURRENT COMPARATOR CONCEPT
A current comparator accepts two current inputs and generates a voltage output based on the result of comparison. The current comparator operates in three different stages as shown in Fig. 1. 1) Current Difference Stage, 2) Gain Stage and 3) Output Stage. The current difference stage accepts two current inputs and produces an output which is the current difference of both the currents.

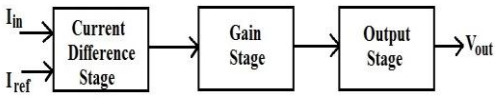

Fig. 1 Current Comparator Stages

When we speak of comparison with a current, the comparison is actually carried out between two currents. We need to set a threshold or reference current with which the input current that we inject needs to be compared. The reference current (I_{ref}) is taken to be a constant current. The principle that governs the operation of the current comparator is:

When $I_{in} > I_{ref}$, V_{out} = Logic High, and

When $I_{in} < I_{ref}$, V_{out} = Logic Low

The current difference (I_{diff}) generated as the output in this stage is given as input to the comparator stage. The sub stages of the comparator stage consist collectively of the gain stage and the output stage. The gain stage accounts for increasing the voltage at the input node as well as for lowering the input impedance. The output stage produces the desired rail-to-rail output based on the comparison results.

3. PROPOSED CURRENT COMPARATOR

The proposed current comparator schematic is shown in Fig. 4 in which the two stages of current comparator are explicitly shown. The current difference stage as shown in Fig. 2 consists of two current mirror, which accepts the two current inputs, namely, the input current I_{in} and the reference current, I_{ref}. The transistors M1-M4 and M5-M8 form two analogous current mirrors. The transistors M9-M12 generate the current difference $I_{diff}(\Delta I)$. The current difference generated is given as the input to the comparator stage.

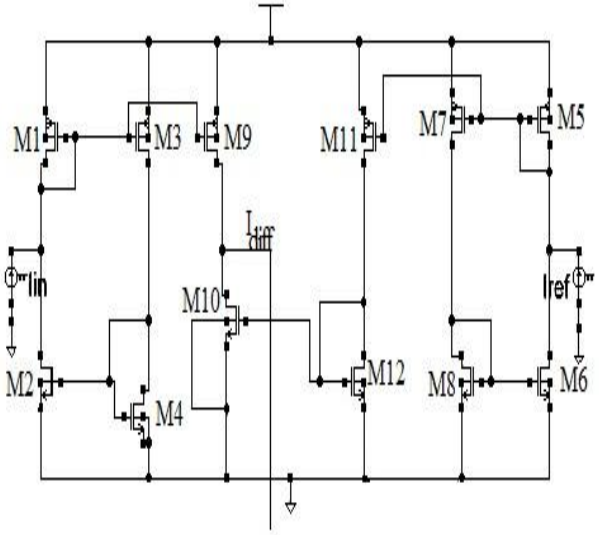

Fig. 1 Schematic of Current Differencing Stage

The comparator stage is shown in Fig. 3 consists of transistors M13 - M22, Mn and Mp. The actual operation of the comparator is carried out in this stage. The comparator works in the same way as in [2], but achieves a greater gain in the comparator stage due to the two cascaded resistive load inverters and the CMOS inverter. To minimise delay, the resistive load inverters use NMOS load devices M13 and M15 instead of conventional PMOS devices as in [12].

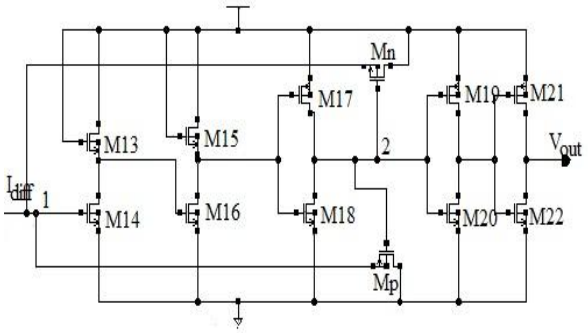

Fig. 3 Schematic of Comparator Stage

The mobility of electrons in NMOS devices is more than that of holes in PMOS devices, due to the fact that electron mobility is twice of that of holes. Also NMOS devices occupy less size as compared to the PMOS devices. The NMOS devices have reduced capacitance due to smaller junction areas. The on-resistance of NMOS devices is half of that of the same size PMOS counterparts. As the speed of operation is mostly due to the RC components, hence this attribute of NMOS device of reduced capacitance and impedance helps in achieving lesser delay due to its small size.

Mn and Mp transistor form a non-linear feedback across the gain stage to reduce the voltage at node 1. These two transistors alternatively remain ON or OFF depending on the voltage that is generated due to the current difference at node 1. The aspect ratios of Mn and Mp devices were selected in such a way that the voltage at node 1 is to be maintained low preferably around the operating point of the first resistive load inverter stage. Also this non linear feedback helps in maintaining a low impedance input node, which is an essential requirement in current mode circuits. The subsequent resistive load inverters in the gain stage followed by the CMOS inverter raise the voltage level as seen at node 2 as compared to the voltage that appears at node 1.

The output stage consists of two CMOS cascaded inverters M19-M22 to produce rail to rail output. The output stage indicates the result of comparison. It has to be designed so as to produce a rail-to-rail voltage. A logic high output indicates the current being compared is higher than the reference current. Similarly a logic low output indicates the input current is less than the reference current.

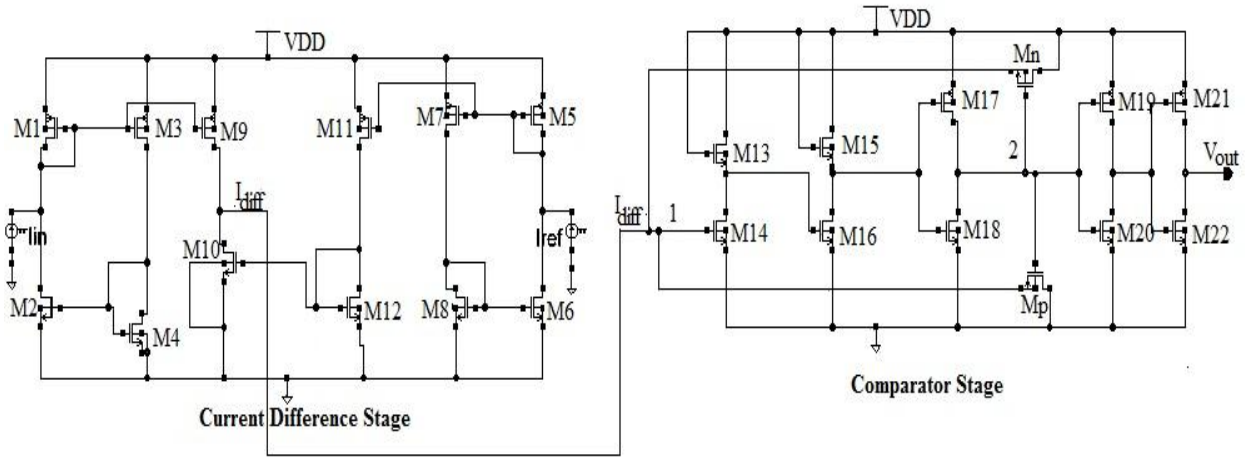

Fig. 4 Schematic of Proposed Current Comparator

4. SIMULATION & RESULTS

To verify the circuit operation various simulations were carried out in Cadence environment in Spectre simulator in 90 nm CMOS process technology. In the proposed work two currents are given as input to the current difference stage. The input current is taken as a pulse and is varied from 0µA to 2µA with a reference current of 1µA. Both dc and transient analysis has been performed on the design and parameters like propagation delay, slew rate, dc power consumption have been found out. All simulations were carried out at a supply voltage of 0.9V and at a room temperature of 27ºC with an input current difference of ±1µA. The dc response of the comparator is shown in Fig. 5.

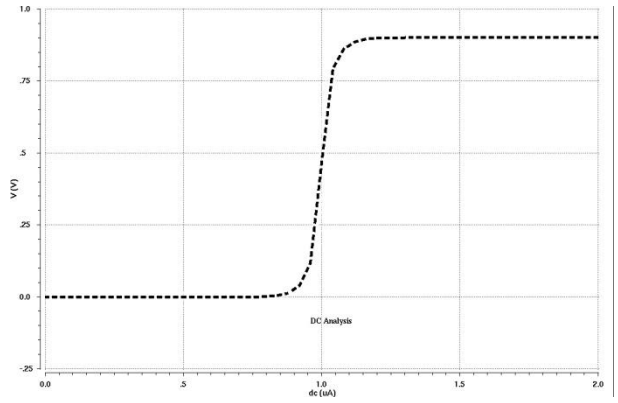

Fig. 5 DC Response Analysis of the Proposed Work

The high speed performance of the proposed design is confirmed through transient operation of the circuit as seen in Fig. 6. For I_{in} = 0µA, output voltage is low. This confirms the correct operation of the current comparator when the input current is less than the reference current which is 1µA. Similarly, when the input current is higher than the reference current the output voltage corresponding to the current detection is 0.9V which is the supply voltage.

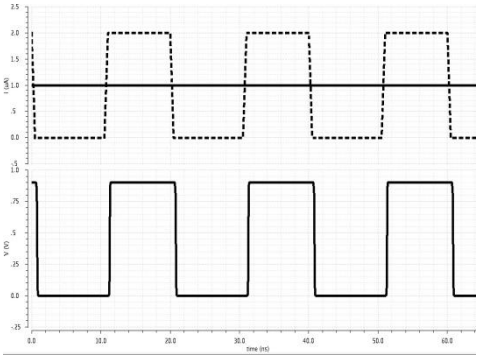

Fig. 6 Transient Response Analysis of Proposed Work

Hence as we can clearly see in Fig. 6 the output swings from rail-to-rail, depending on the current detected. The output voltage swing achieved in the design is shown in Fig. 7. For a current difference of ±1µA, the delay was found to be 0.55ns. The slew rate of the proposed design was found to be 8.8V/ns. The average power dissipation of the design at a current difference of ±1µA was found to be 122µW.

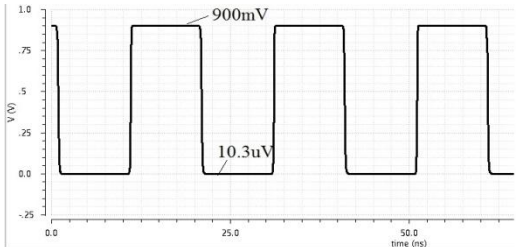

Fig. 7 Output Voltage Swing

The delay and average power dissipation is plotted against the current difference as shown below in Fig. 8 and Fig. 9 respectively. The highest and lowest power dissipation is found to be 146.4µW and 122µW respectively for current difference of ±0.1µA and ±1µA respectively. Fig. 10 shows the plot of PDP (Power Delay Product) against the current difference. The highest and lowest PDP values found are 0.1054pJ and 0.0675pJ for current difference of ±0.1µA and ±1µA respectively. The resolution of the current comparator was found to be ±10nA.

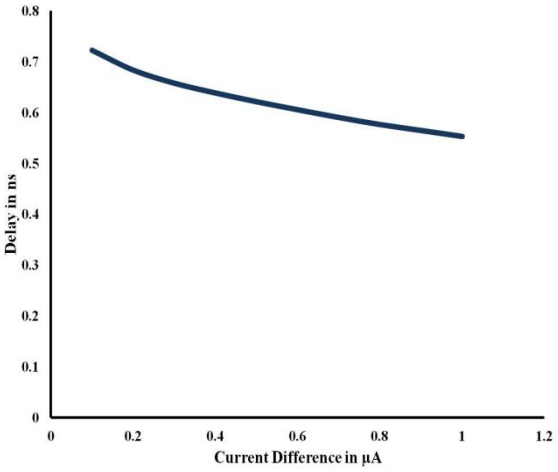

Fig. 8 Variation of Delay with Current Difference

The temperature variation cannot be avoided in the everyday performance of any circuit design. The performance of the proposed current comparator is verified by varying the temperature from -100ºC to 150ºC. The power and delay are plotted against temperature as shown in Fig. 11 and Fig. 12 respectively. It is seen that the delay increases at high temperatures as compared to low temperatures. The power dissipation of the circuit falls at high temperatures.

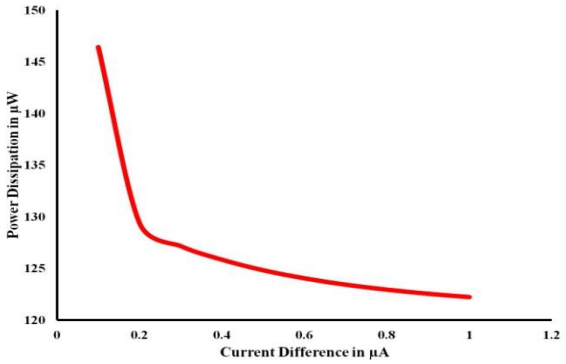

Fig. 9 Variation of Power Dissipation with Current Difference

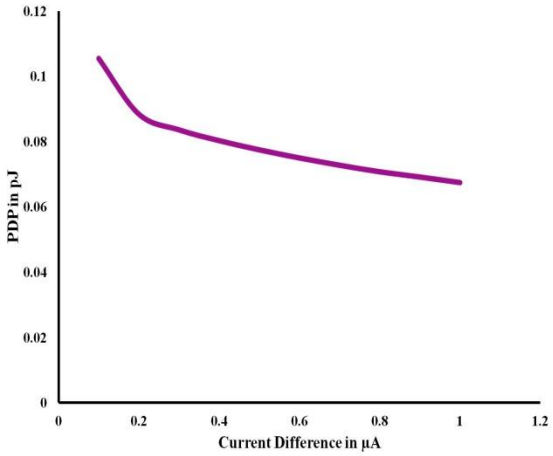

Fig. 10 Plot of PDP against Current Difference

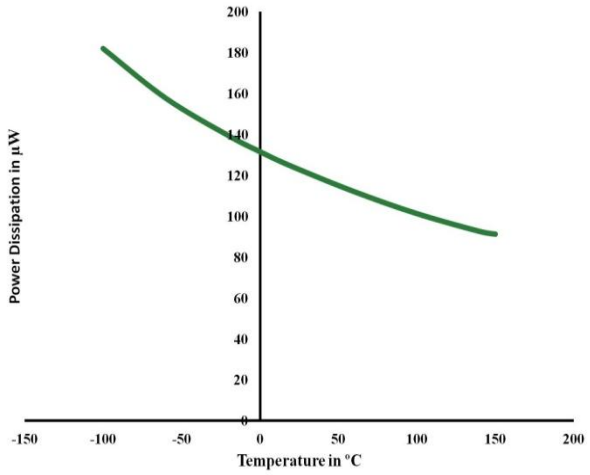

Fig. 11 Variation of Power with Temperature

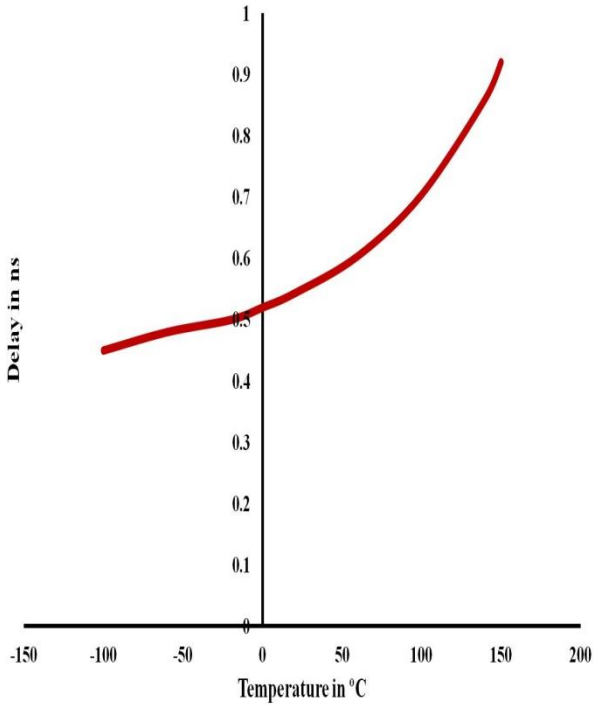

Fig. 12 Variation of Delay with Temperature

In Table I, a comparative analysis of the results obtained in the present design is compared with the earlier existing designs and is listed below. From the table we can conclude that the present design shows better performance in terms of delay and power over the pre-existing designs. The current comparator designed in [4] has the highest delay of 11ns as well as it dissipates the highest power. The designs in [2] and [4] have not included a current differencing stage which is implemented in the design presented in [12] and has also been included in our present design.

Table 1. Comparative Analysis of Existing Designs and Proposed Design

	Year	**Technology**	**Supply Voltage (V)**	**Input Current Difference (Idiff) (µA)**	**Delay (ns)**	**Average Power Dissipation (mW)**
Design in [2]	1992	2 µm	5	1	4	0.39
Design in [4]	1994	1.6 µm	5	0.1	11	1.4
Design in [10]	2004	0.5 µm	3	0.1	1.67	0.63
Design in [12]	2012	0.18 µm	1.8	1	0.86	0.65
Present Work	2014	90 nm	0.9	1	0.55	0.122

5. CONCLUSION

The current comparator designed in this paper can favourably be used in low power and high speed applications. At a current difference of ±1µA it exhibits a delay of 0.55ns and has an average power dissipation of 122µW. The power delay product of this design was found to be 0.0675pJ which is very less as compared to the existing designs. From the simulation results we can see that the comparator presented in this work shows improved performance and can be used in ADC's.

6. ACKNOWLEDGMENT

This work is successfully carried out and supported by KIIT University, Bhubaneswar, Odisha.

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