Modified Double-Edge Triggered Clock Branch Sharing Architecture for Ultra Low Power Design

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ABSTRACT
Power consumption plays an essential role in VLSI design. Earlier, the VLSI designers were more concentrated on performance and area, but, gradually, low power consumption became one of the most important factors in VLSI design. Increasing demand and growth of portable devices have increased the demand of power efficient VLSI circuits. In this paper, various conventional low power designs are analyzed and a low power double-edge triggered flip-flop using clock branch sharing technique along with MTCMOS and Voltage Scaling technique has been proposed. All the simulations have been carried out using Cadence EDA tools in 0.18 µm technology at room temperature. The power consumption has reduced significantly as compared to earlier techniques.

Keywords:
Clock, Delay, Clock Branch Sharing Technique, MTCMOS, Voltage Scaling.

1. INTRODUCTION
Two factors namely, "clock distribution network" and "timing elements" constitute the whole clock system [1] & [2] and it consumes about for 30 to 60 per cent of the total power consumption[3]. Thus, overall power dissipation of the system will be reduced by reducing the clock power. The major components of power dissipation in a digital system are summarized in the following equation [4].

$$P_T = \alpha^{(0\rightarrow1)}V^2_{dd}f_{clk} + V_{dd}(I_{sc} + I_{leakage} + I_{static}) \quad (1)$$

P_T stands for total power dissipation; $\alpha C_L V^2_{dd} f_{clk}$ represents the switching power dissipation, where α stands for the switching activity factor; C_L stands the load capacitance and f_{clk} is the clock frequency. I_{sc} represents the short circuit current; $I_{leakage}$ represents the leakage current; I_{static} represents the static current i.e. the direct current from power rail to ground rail. For high-speed and low-power applications, reducing the leakage and switching power is essential.

Voltage scaling and Multi-Threshold voltage (MTCMOS) technique are the most effective ways for reducing dynamic power and static power respectively. Another method could be the dual-edge clock triggering that can reduce the total power dissipation substantially.

Flip-flops are used as data storage elements which store the logical state of any data input signal with respect to a clock pulse [5]. In general the clock circuit consumes a lot of power; hence, reducing the clock frequency by half will help in reducing the total power dissipation by nearly one half. Using DETFF (dual-edge triggered flip-flop) in the clock distribution network will decrease the original clock frequency by half [6], decreasing the total power dissipation and thus making them appropriate for low power systems.

Various conventional designs given in the literature [6]-[9] effectively reduce the total power consumed by the clock system. A number of the existing applications use pulse-triggered flip-flops and master-slave flip-flops selectively. The literature contains two types of edge triggered flip-flops: hard edge (transmission gated edge triggered flip-flops and sense amplifier based flip-flops) and soft edge (pulse triggered flip-flops). The hard edge triggered flip-flops consist of one master stage and a slave stage which causes the D-to-Q delays to be high. The soft edge triggered flip-flops reduces the two stages to a single stage and is characterized by a soft edge property. Again, the pulse edge triggered flip-flop is classified into explicit-pulsed (ep-FF) and implicit pulsed (ip-FF) triggered flip flops respectively. In ep-FF, the externally present clock pulse generator is distributed among the adjacent flip-flops, thereby distributing the power overhead across several other explicit-pulsed flip-flops. This improves the performance of the circuit.

This paper is organized into the following sections. Section II gives a brief explanation about the drawbacks of the conventional designs. Section III discusses the conventional design of double-edge triggered clock branch sharing implicit pulsed flip-flop. Section IV presents the proposed DE CBS-ip flip-flop using MTCMOS and voltage scaling technique. Section V presents the simulation results. Section VI concludes the paper. Section VII gives the future work.

2. DRAWBACKS OF THE CONVENTIONAL TOPOLOGIES
The area and load is duplicated in the conventional DEFFs. In case of explicit-pulsed flip-flops, the power is increased because of the use of external clock pulse generators. Also, the concept of dynamic logic cannot be implemented. SCPGFF uses implicit pulsing. In case of DECPFF the redundant switching activity is removed, but the clock branch duplicating structure is complex and the number of clocked transistors also increases up to 21.

3. DUAL-EDGE TRIGGERED CLOCK BRANCH SHARING IMPLICIT PULSED FLIP-FLOP (CBS_IP)
The conventional dual-edge triggered CBS_ip flip-flop implements the clock sharing concept (Fig. 1). The first and the second stage of the CBS_ip flip-flop share the clocked branches respectively. This clock branch sharing concept overcomes the drawbacks of the previous conventional flip-flops i.e. large clock load, thereby decreasing the number of transistors. The sharing concept is similar to STCFF [9].

A split path technique (node X drives P2 only) ensures that the flip-flop functions properly after merging the two sets of clocked transistors in DECPFF [14]. This sharing concept reduces the total number of clocked transistors thus decreasing power[2].

Comparison between the conventional flip-flops is presented in Table I [14].

TABLE I:

Device Name	No. of transistors	D-Qb (ps)	Power (µW)	PDP (fJ)
SPGFF	30	162	16.4	2.66
ep-DSFF	20	155	14.5	2.25
CBS_ip	23	179	13.0	2.33

4. PROPOSED DOUBLE-EDGE TRIGGERED CLOCK BRANCH SHARING FLIP-FLOP

The keeper circuit is replaced by a weak pmos, P3(Fig 2). P3 works exactly like the keeper circuit, retaining the previous state/value until the output Qb is LOW.

The clocked branch uses the sharing concept as in the previous CBS_ip flip-flop. It uses another conditional discharge technique as a result of which D and Qb have opposite polarity. P1should be properly sized in order to reduce charge sharing between the four stacked transistors N1, N3, N5 and N7. Charge will be shared if either three of the four transistors are ON at the same time. Direct noise coupling is prevented by the inverter I4 placed after Q.

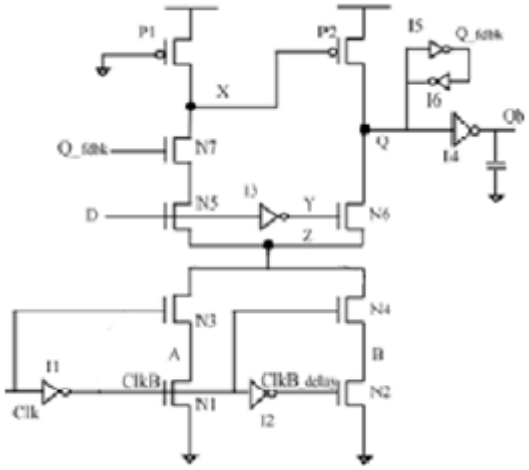

Fig. 1: Clock Branch Sharing_ip Flip-Flop

The circuit operation, Fig 2, is as follows. Qb controls the transistor N7. When the clock signal is 1, ClkB = 1 for one inverter delay, during which the flip-flop will be in the evaluation mode; (N1, N3) turn on while N2, N4 are off. Similarly when clock signal is 0, ClkB = 1 and ClkB_delay =1 for two inverter delays, during which N2, N4 turn on and N1, N3 are disconnected.

The low-to-high transitions of D are captured by the first stage. Node X discharges such that Q is HIGH and Qb is LOW. N7 turns off. When D = 1, the first stage gets disconnected, thus node X does not undergo redundant switching activity.

The high-to-low transitions of D are captured by the second stage. The high-to-low input transitions turns on the pull down network of the second stage resulting in Q = 0 and Qb = 1.

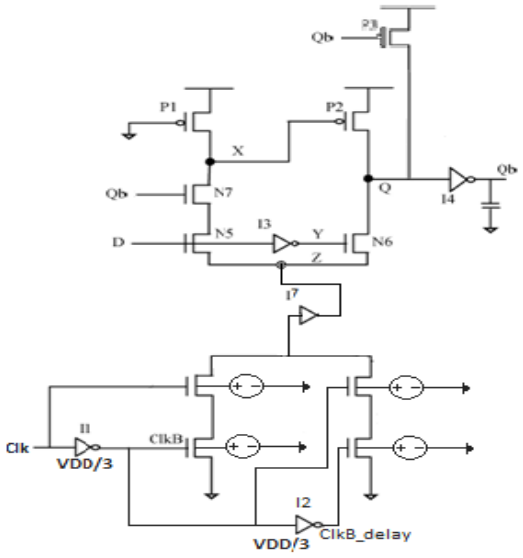

Fig 2: Proposed Clock Branch sharing implicit pulsed Flip-Flop

The Clock Branch Sharing implicit pulsed flip-flop (CBS_ip) uses split-path technique i.e. node X drives only P2 and node Y drives only N2, as a result of which the propagation delay through the flip-flop is reduced. The skew inverters I1 and I2 driving the clocked transistors N1 and N2 turn ON a little before the rising/falling edge of the clock, thereby reducing the discharge time.

The proposed circuit implements Voltage Scaling and MTCMOS techniques for reducing the leakage power, functionality and die performance (Fig 2).

The voltage supplied to the skew inverters is taken as Vdd/3. The bias voltage used in the clock circuit is 300 mV.

5. SIMULATION RESULTS

The simulation results were obtained from Cadence EDA tools in 0.18-µm technology at room temperature. The setup used in our simulation is as follows Fig 3.

For accurate results, the circuits are simulated in real environment where the output load is driven by outputs and the inputs i.e. clock (clk) and data (D) are operated by input buffers. The load capacitance at Q, C_{load} = 21 fF (load capacitances of ep-DSFF and CBS_ip flip-flops are at Qb) [13]. Another capacitance at the clock driver is kept at 3 fF [13].

Input D is supplied with pseudorandom input data to reflect the average power consumption [1], [12]. In ep-DSFF and CBS_ip flip-flops, the delay was measured from D to Qb; in all other flip-flops the delay is calculated from D to Q. Delay is the sum of C-to-Q delay and the setup time [1], [2]. In a dual-edge triggered flip-flop data sampling is carried out at both the edges of the clock. Hence four D-to-Qb delay cases are checked: 0-1 data transition at the clock rise/fall edge; and 1-0 data transition at the clock rise/fall edge.

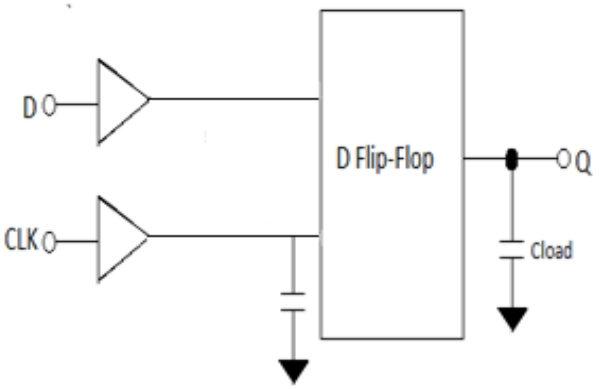

Fig 3: Setup used for simulation

Table II presents the comparison table of CBS_ip with respect to the conventional CBS_ip.

Power is reduced by 47% with respect to the conventional CBS_ip with a delay of 167 ps at a supply voltage of 1.8V. PDP is reduced by 48.5% respectively.

Fig 4 shows the power vs delay plot of the proposed CBS_ip with technology scaling and without technology scaling. The output waveform of the proposed CBS_ip flip-flop is shown in Fig 5. The output waveform shows both low-to-high and high-to-low transitions of D.

Table Ii: Proposed CBS_Ip using Voltage Scaling and Mtcmos Technology in Terms of Power, Delay and PDP

Supply Voltage	No. of transistors	D-Qb (ps)	Power (µW)	PDP (fJ)
1.8 V	22	167.0	6.9	1.2
1.5 V	22	211.1	4.9	1.0
1.3 V	22	265.3	3.8	1.0

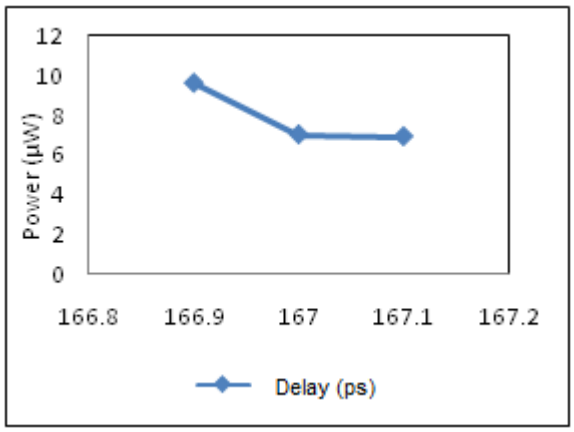

Fig 4: Power vs Delay plot

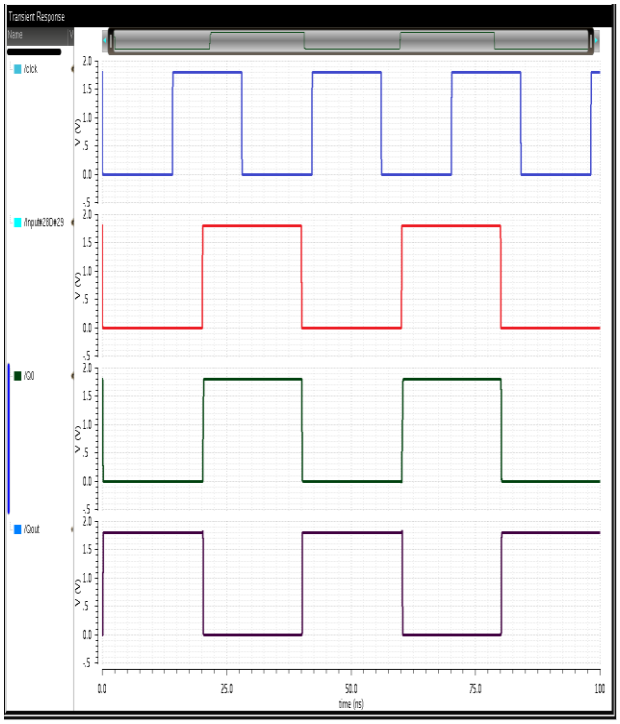

Fig 5: Output waveform of the proposed CBS_ip

6. CONCLUSION

The newly proposed CBS_ip flip-flop consumes much less power than any other conventional dual-edge design. In view of PDP also the proposed design is better. The clock branch sharing technique effectively decreases the total number of transistors used in the clock circuit resulting in low power and high speed. The split path technique and the conditional discharge technique used in the CBS_ip help in reducing short circuit current and redundant switching activity respectively. It is best suited for low power and high speed applications since the number of clocked transistors and power consumption is minimum.

7. FUTURE SCOPE

The future scope of the proposed design can be extended to its hardware implementation by dumping the design in a Spartan 4 FPGA kit. Also, the leakage power could be reduced by using a pmos stack as a voltage divider that will act as supply to the skew inverters.

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