All Optical Reversible NOR Gates using TOAD

Ashis Kumar Mandal[1], Goutam Kumar Maity[2]
[1]Department of Physics, Chakur Haris Seminary High School, Howrah, India
[2]Department of Electronics and Communication Engineering, MCKV Institute of Engineering, Howrah , India

ABSTRACT
In recent past, reversible logic is emerged as a promising computing paradigm with applications in low-power CMOS, quantum computing, optical computing and nanotechnology. Optical logic gates become potential component to work at macroscopic (light pulses carry information), or quantum (single photon carries information) levels with high efficiency. In this paper, we propose a novel scheme of TOAD-based all optical reversible NOR gates and their universal application in all-optical domain. Simulation results verify the functionality of these TNOR and PNOR gates as well as reversibility.

Index Terms
Reversible logic gates, Terahertz Optical Asymmetric Demultiplexer (TOAD). TNOR gate, PNOR gate

1. INTRODUCTION
All-optical switching - the switching of one beam of light by another — is an essential operation for transparent fiber optic networks and for all forms of optical information processing [1-6]. To overcome the electronic bottlenecks and fully exploit the advantages of optical fiber communication, it is necessary to move towards networks where the transmitted data would remain exclusively in the optical domain without optical-electrical-optical (OEO) conversions [7-9]. Two fold driving forces for this all-optical switching are the broadband photonic network environment that emerges due to rapid convergence of telecommunication and informatics.

In conventional computers, majority of the computation operations are irreversible i.e. once a logic block generates the output bits based on certain input combinations, the later bits are lost. The classical set of gates such as AND, OR and X-OR are irreversible as they are all multiple-input single output logic gates. However, this is not the case for reversible logic circuits. A gate is reversible if the gate's inputs and outputs have a one-to-one correspondence, i.e. there is a distinct output assignment for each distinct input combination. Therefore, a reversible gate's inputs can be uniquely determined from its outputs. Reversible logic gates must have an equal number of inputs and outputs. Then the output rows of the truth table of a reversible gate can be obtained by permutation of the input rows. Reversible logic circuits have been emerged as a promising technology in the field of information processing, for example, military data processing to preserve intelligence or medical signal to prevent data loss or revert back data modification. Irreversible computation results in energy dissipation due to data loss [10]. On the other hand, the reversible logic circuits offer an alternative form that allows computation with arbitrary small energy dissipation [11].

2. OPERATIONAL PRINCIPLE OF TOAD BASED OPTICAL SWITCH
TOAD based gate has taken an important role in optical communication and information processing [12-24]. Sokoloff et al. [17] demonstrated a TOAD capable of demultiplexing data at 50 Gb/s.

The TOAD consists of a loop mirror with an additional intraloop 2×2 (ideally 50:50) coupler. The loop contains a control pulse (CP) and a nonlinear element (NLE) that is offset from the loop's midpoint by a distance Δx as shown in Fig. 1.

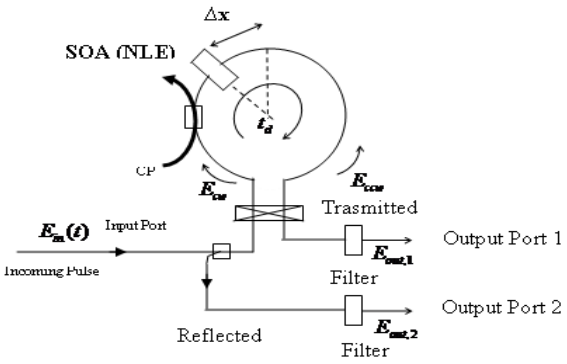


Fig. 1: TOAD-based optical switch

A signal with field $E_{in}(t)$ at angular frequency ω is split in coupler. It travels in clockwise (cw) and counter clockwise (ccw) direction through the loop. The electrical field at port-1 and port-2, can be expressed as follows .

$$\underline{E}_{out,1}(t) = \underline{E}_{in}(t-t_d)\cdot e^{-j\omega t_d}\cdot\left[d^2\cdot\underline{g}_{cw}(t-t_d) - k^2\cdot\underline{g}_{ccw}(t-t_d)\right] \quad (1)$$

$$\underline{E}_{out,2}(t) = jdk\underline{E}_{in}(t-t_d)\cdot e^{-j\omega t_d}\cdot\left[\underline{g}_{cw}(t-t_d) + \underline{g}_{ccw}(t-t_d)\right] \quad (2)$$

Where t_d is pulse round trip time within the loop as shown in the Fig- 1. Coupling ratios *k* and *d* indicate the cross and through coupling, respectively. The cw signal be amplified by the complex field gain. $\underline{g}_{cw}(t)$, while ccw by $\underline{g}_{ccw}(t)$. The output power at port-1 can be expressed as,

$$P_{out,1}(t) = \frac{P_{in}(t-t_d)}{4}\cdot\left\{G_{cw}(t)+G_{ccw}(t)-2\sqrt{G_{cw}(t)\cdot G_{ccw}(t)}\cdot\cos(\Delta\varphi)\right\} = \frac{P_{in}(t-t_d)}{4}\cdot SW(t) \quad (3)$$

where, $SW(t)$ is the transfer function. The phase difference between cw and ccw pulse is defined by $\Delta\varphi = (\varphi_{cw} - \varphi_{ccw})$. The symbols $G_{cw}(t), G_{ccw}(t)$ indicate

the respective power gains. Power gain is related with the field gain as $G = g^2$ and $\Delta\varphi = -\frac{\alpha}{2}\cdot\ln\left(\frac{G_{cw}}{G_{ccw}}\right)$.

Now we will calculate the power at port-2

$$P_{out,2}(t) = \frac{1}{2}\underline{E}_{out,2}(t)\cdot\underline{E}^{*}_{out,2}(t)$$

$$= d^2k^2\cdot P_{in}(t-t_d)\cdot g_{ccw}^{\ 2}(t-t_d)$$

$$\cdot\left\{1+\frac{g_{ccw}^{\ 2}(t-t_d)}{g_{cw}^{\ 2}(t-t_d)}+2\cdot\frac{g_{ccw}(t-t_d)}{g_{cw}(t-t_d)}\cdot\cos\left[\varphi_{cw}(t-t_d)-\varphi_{ccw}(t-t_d)\right]\right\}$$

$$= d^2k^2\cdot P_{in}(t-t_d)\cdot G_{cw}\cdot\left\{1+\frac{G_{ccw}}{G_{cw}}+2\cdot\sqrt{\frac{G_{ccw}}{G_{cw}}}\cdot\cos\left[\Delta\varphi\right]\right\}$$

$$= d^2k^2\cdot P_{in}(t-t_d)\cdot\left\{G_{cw}+G_{ccw}+2\cdot\sqrt{G_{ccw}\cdot G_{cw}}\cdot\cos\left[\Delta\varphi\right]\right\} \qquad (4)$$

For ideal 50:50 coupler, $d^2 = k^2 = 1/2$. In the absence of a control signal, data signal (incoming signal) enters the fiber loop, pass through the SOA at different times as they counter-propagate around the loop, and experience the same unsaturated amplifier gain G_0, recombine at the input coupler i.e. $G_{ccw} = G_{cw}$. This leads to $\Delta\varphi = 0$. So expression for $P_{out,1}(t) = 0$ and $P_{out,2}(t) = G_0\cdot P_{in}$. It shows that data is reflected back toward the source. When a control pulse is injected into the loop, it saturates the SOA and changes its index of refraction. As a result, the two counter-propagated data signals will experience a differential gain saturation profiles i.e. $G_{ccw} \neq G_{cw}$. Therefore, when they recombine at the input coupler, the data will exit from the output port-1. For this case, the mathematical forms of two output powers can be expressed as, $P_{out,1}(t) = \frac{P_{in}(t-t_d)}{4}\cdot SW(t)$ and $P_{out,2}(t) \approx 0$. Result of numerical simulation with Matlab7.0 has been shown in Fig. 2. In this simulation line-width enhancement factor of SOA (α) was taken 9.5 and the ratio G_{ccw}/G_{cw} was taken 0.52.

A polarization or wavelength filter may be used at the output to reject the control and pass the input pulse. Now it is clear that in the absence of control signal, the incoming pulse exits through input port of TOAD and reaches the output port-2 as shown in Fig. 2. In this case no light is present in the output port-1. But in the presence of control signal, the incoming signal exits through output port of TOAD and reaches the output port-1 as shown in Fig. 1. In this case no light is present in the output port-2.

In the absence of incoming signal, Port-1 and Port-2 receive no light signal as the filter blocks the control signal.

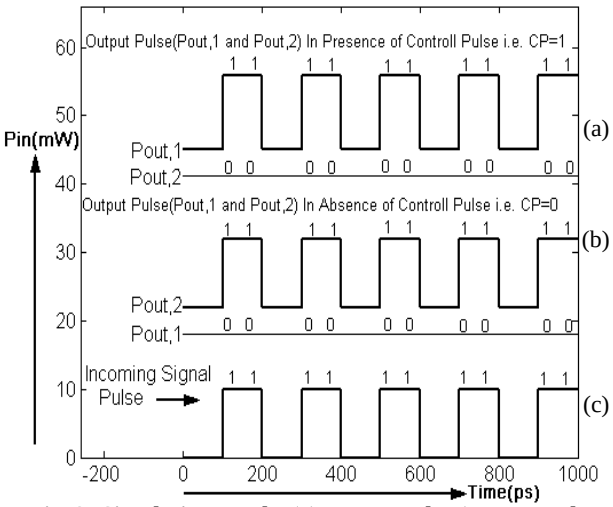


Fig. 2: Simulation result: (a) output pulse (Pout,1 and Pout,2) in presence of control pulse i.e. CP=1 (b) output pulse (Pout,1 and Pout,2) in absence of control pulse i.e. CP=0 (c) incoming signal pulse.

Schematic block diagram is shown in Fig. 3 and truth table of the operation is given in Table-I.

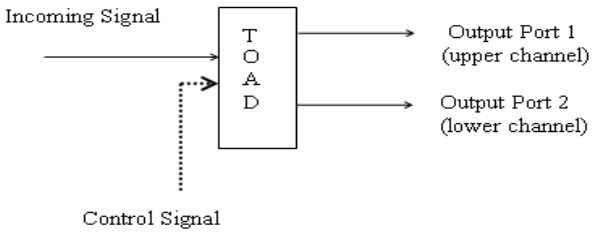


Fig. 3: Schematic diagram of TOAD-based optical switch

TABLE-I
Truth table of TOAD-based optical switch of fig .3

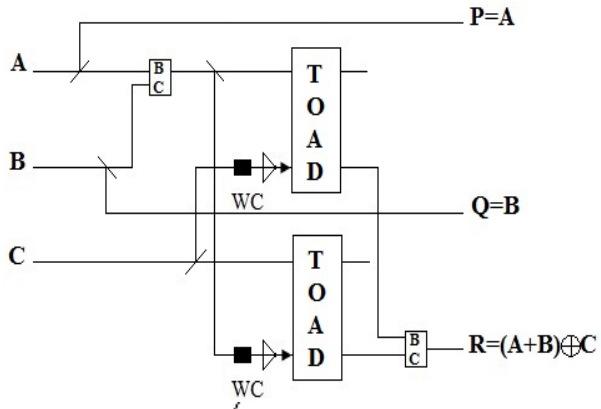
Incoming Signal	Control Signal	Output Port-1	Output Port-2
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	0

3. PROPOSED ALL OPTICAL TNOR GATE

This proposed all optical TNOR gate performs as a replacement of existing NAND based all optical Toffoli gate. The TNOR gate works as NOR based implementation of reversible boolean functions in optical computing domain with less optical cost and delay[25]. The all optical TNOR gate is a 3x3 conservative reversible logic gate. It has inputs to outputs mapping as (A,B,C) to (P = A, Q = B, R = (A+B)⊕C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. Figure 4(a) and Fig. 4(b) show the all optical implementation of all optical TNOR gate and the block diagram, respectively. The truth table of all optical TNOR gate is given in Table 2. The all optical TNOR gate will perform as a NOR gate when the value of input signal C is 1. When C=1, the outputs of the TNOR gate transforms as P = A, Q = B and R = (A+B)⊕1 = A + B. The all optical TNOR gate can be implemented using 2 TOAD-based switches, 4 beam splitters (BS) and 2 beam combiners (BC). The optical cost of TNOR gate is considered

as 2, since its optical implementation requires 2 TOAD-based switches. The delay of all optical TNOR gate is 1Δ, as in its optical design two TOAD switches works in parallel.

(a)



BC: Beam Combiner, / BS: Beam Splitter, ▷ EDFA: Erbium Doped Fiber Amplifier, ■ WC: Wavelength Converter

(b)

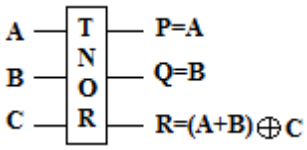


Fig. 4 (a) all optical implementation of the TNOR gate, (b) Block diagram of the TNOR gate

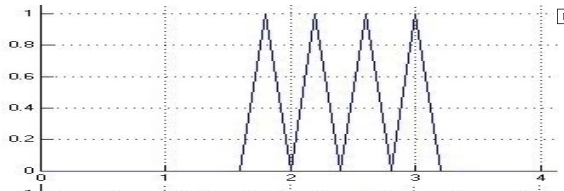
TABLE-II
Truth table of TNOR gate

Inputs			Outputs		
A	B	C	P=A	Q=B	R = (A + B) ⊕ C
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	1	0

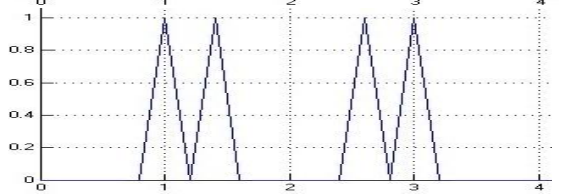
4. SIMULATION AND RESULT

Simulation is done with Matlab-7. Figure 7(a), (b) and (c) are the three inputs A, B and C respectively. And figure 7(d) to (j) are the simulation results of figure 6(a) to 6(g) respectively.

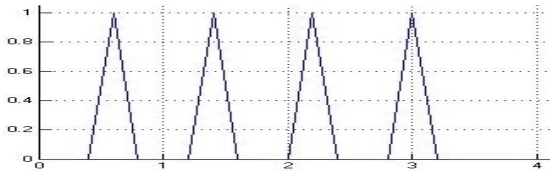
(a)



(b)



(c)



(d)

Fig 5 (a) input A, (b) input B, (c) input C, (d) output R of fig 4(a)

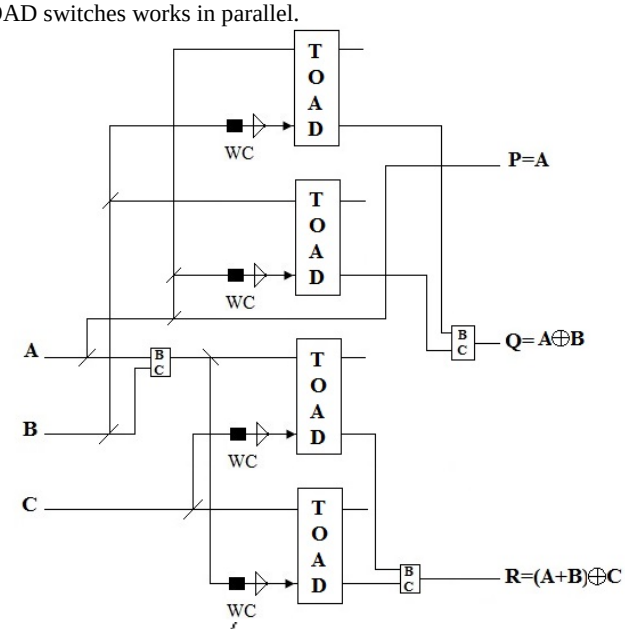
5. PROPOSED ALL OPTICAL PNOR GATE

This proposed all optical PNOR gate is a (3x3) conservative optical reversible gate with the inputs to outputs mapping as (A, B, C) to (P = A, Q = A ⊕ B, R = (A + B) ⊕C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. The proposed all optical PNOR gate can be used as the replacement of existing NAND based all optical Peres gate [26].

The truth table of all optical PNOR gate is given in Table 3. An all optical PNOR gate can be implemented using 4 TOAD-based switches, 7 beam splitters (BS) and 3 beam combiners (BC). Figure 5(a) and Fig. 5(b) show the all optical implementation of PNOR gate and the block diagram, respectively.

The optical cost of PNOR gate is considered as 4 as its optical implementation requires 4 TOAD-based switches. The all optical PNOR gate has delay of 1Δ as in its optical design four TOAD switches works in parallel.

(a)



BC: Beam Combiner, / BS: Beam Splitter, ▷ EDFA: Erbium Doped Fiber Amplifier, ■ WC: Wavelength Converter

(b)

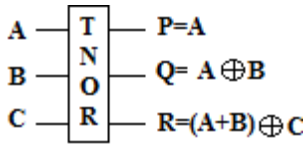


Fig. 6 (a) All optical implementation of the PNOR gate, (b) Block diagram of the PNOR gate

TABLE-III

Truth table of PNOR gate

Inputs			Outputs		
A	B	C	P=A	Q=A ⊕ B	R = (A + B) ⊕ C
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

6. SIMULATION AND RESULT

Simulation is done with Matlab-7. Figure 7(a), (b) and (c) are the three inputs A, B and C respectively. And figure 7(d) to (j) are the simulation results of figure 6(a) to 6(g) respectively.

(a)

(b)

(c)

(d)

(e)

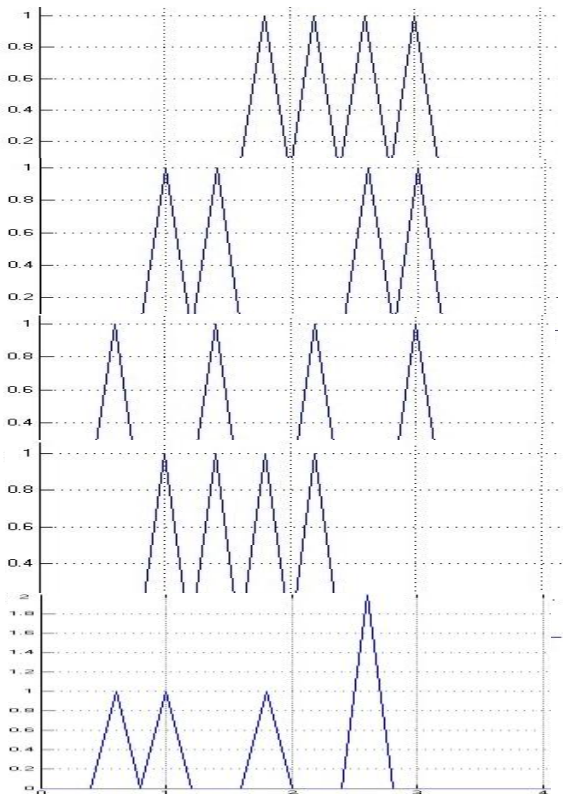
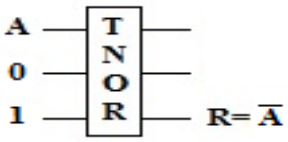


Fig 7 (a) input A, (b) input B, (c) input C, (d) output Q, (e) output R of fig 6(a)

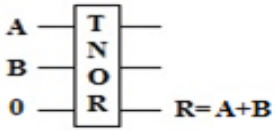
7. APPLICATION OF TNOR GATE AS UNIVERSAL GATE

TNOR gate can be used to perform as universal logic gate. Proposed arrangements to perform various gate operations are as follow.

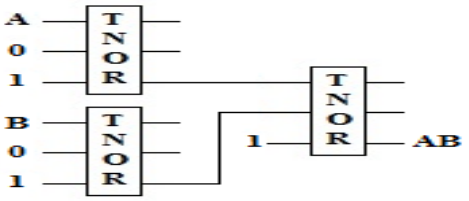
(a)



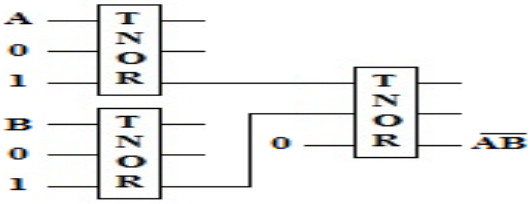
(b)



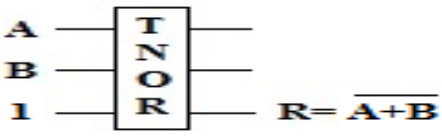
(c)



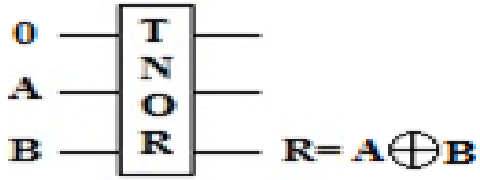
(d)



(e)



(f)



(g)

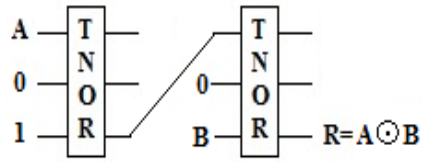


Fig. 8 (a) to 8(g) are for NOT, OR, AND, NAND, NOR, X-OR and X-NOR

8. SIMULATION AND RESULT

Figure 9(a), (b) and (c) are the three inputs A, B and C respectively. And figure 9(d) to (j) are the simulation results of figure 8(a) to 8(g) respectively. Simulation is done with Matlab-7.

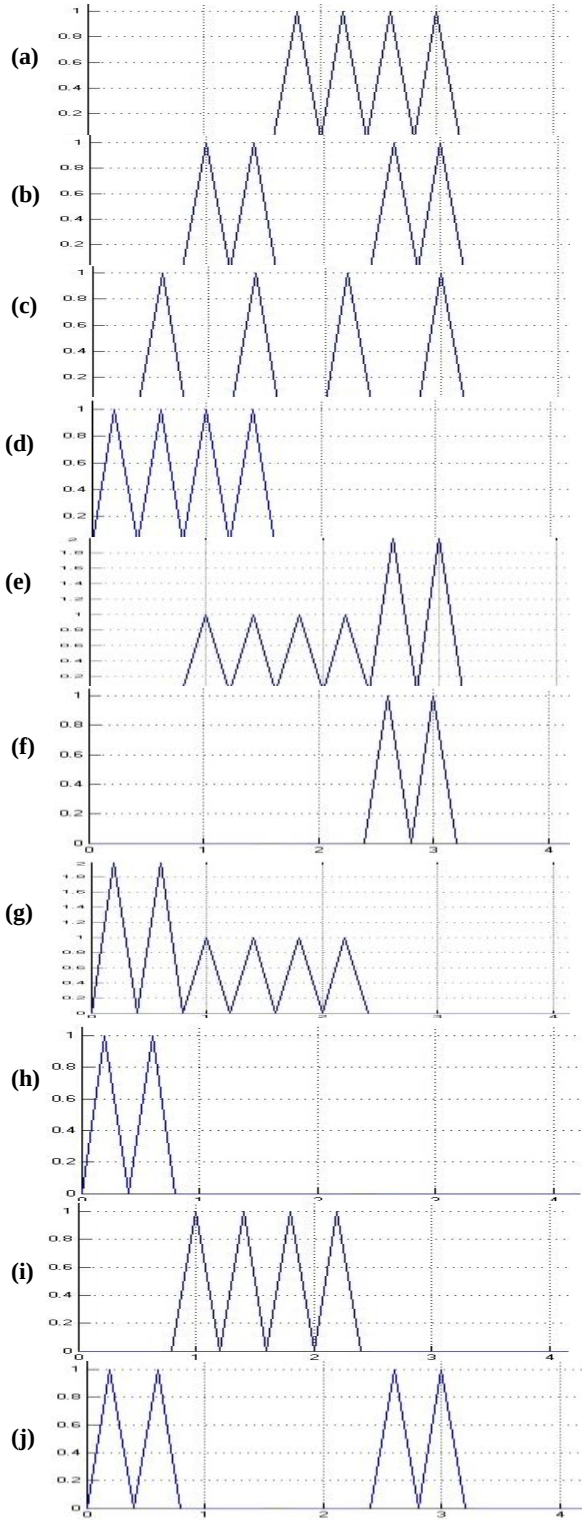


Fig 9(a) input A, 9(b) input B, 9(c) input C and 9(d) to 9(j) simulation result of gates of fig 8(a) to 8(g)

The vertical axis in all figures of simulation results indicates in dB, while horizontal axis represents time scale in ps.

9. CONCLUSION

In this paper, we have designed two new all optical reversible NOR gates for NOR based implementation of reversible boolean functions and arithmetic operations. The first all optical TNOR gate can be used as a replacement for existing all optical Toffoli gate, while the second all optical PNOR gate can be used as a replacement of all optical Peres gate. It is reported that the proposed all optical reversible NOR gates have significant advantages over existing reversible NAND gates in terms of optical cost and delay. So, these new optical reversible NOR gates can be profitable for minimizing the optical cost and delay of the optical reversible circuits. All the optical reversible gates are functionally verified at the logic level using Matlab-7. In conclusion, this paper helps the state of the art of reversible optical circuits by using the NOR logic based reversible gates as an alternative to NAND logic based reversible gates. The theoretical models developed and the results obtained numerically are useful to future all-optical reversible logic computing system.

10. REFERENCE

[1] J.Hardy and J.Shamir, Optics inspired logic architecture, Optics Express, 15(1), (2007), 150-165.

[2] S. Dolev, T. Haist and M. Oltean, Optical Supercomputing: First International Workshop, Vienna, Austria, (Springer) P. 33-45 (2008).

[3] F. T. S. Yu, S. Jutamulia, S. Yin, Introduction to information optics. Academic Press, San Diego (2001).

[4] G. P. Agrwal Applications of nonlinear fibre optics (Academic press, India [an imprint of Elsevier, San Diego, USA,]) (2001).

[5] M. A. Karim, A. A. S. Awal, Optical Computing: an introduction (Wiley, New York) (1992).

[6] A.I. Zavalin, J. Shamir, C. S. Vikram, H. J. Caulfield, Achieving Stabilization in interferometric Logic Operations, Appl. Opt. 45, (2006), 360-365.

[7] T. Houbavlis, K. E. Zoiros, SOA-assisted Sagnac switch and investigation of its roadmap from 10 to 40 GHz, Optical and Quantum Electronics 35, (2003), 1175–1203.

[8] T. Houbavlis, K. E. Zoiros, Ultrafast pattern-operated all-optical Boolean XOR with semiconductor optical amplifier-assisted Sagnac switch, Opt. Eng. 42 (12), (2003), 3415–3416.

[9] K. E. Zoiros, T. Houbavlis, M. Kalyvas, Ultra-high speed all-optical shift registers and their applications in OTDM networks, Optical and Quantum Electronics 36, (2004), 1005–1053.

[10] R.Landauer, Irreversibility and heat generation in the computational process. IBM Journal of Research and Development (1961), 5:183–91.

[11] CH. Bennett, Logical reversibility of computation. IBM Journal of Research and Development (1973), 17:525–32.

[12] DP. Vasudavan, PK. Lala, J. Di, JP. Parkerson, Reversible-logic design with online testability. IEEE Transactions on Instrumentation and Measurement (2006), 55(2):406–14.

[13] M. Mohammadi, M.Eshghi, M.Haghparast, Bahroloom A. Design and optimization of reversible BCD adder/subtractor circuit for quantum and nanotechnology

based system. World Applied Sciences Journal (2008), 4(6):787–92.

[14] M.Haghparasat, K.A. Navi, novel reversible BCD adder for nanotechnology based systems. American Journal of Applied Sciences (2008), 5(3):282–8.

[15] J. Shamir, HJ.Caulfield, W.Micelli, RJ. Seymour, Optical computing and Fredkin gates. Applied Optics (1986), 25(10):1604–7.

[16] N. A. Whitaker, Jr., M. C. Gabriel, H. Avramopoulos, A. Huang, All-optical, all-fiber circulating shift register with an inverter, Opt. Lett. (1991), 16(24).

[17] J. P. Sokoloff, P. R. Prucnal, I. Glesk, M. Kane, A terahertz optical asymmetric demultiplexer (TOAD), IEEE Photon. Techno. Lett. 5 (7), (1993), 787-789.

[18] J. P. Sokoloff, I. Glesk, P. R. Prucnal, R. K. Boneck, Performance of a 50 Gbit/s Optical Time Domain Multiplexed System Using a Terahertz Optical Asymmetric Demultiplexer, IEEE Photon. Techno. Lett.6 (1), (1994), 98-100.

[19] Z.Y. Shen and L. L. Wu, Reconfigurable optical logic unit with a terahertz optical asymmetric demultiplexer and electro-optic switches, Appl. Opt. 47(21), (2008), 3737-3742.

[20] Y. J. Jung, S. Lee, N. Park, All-optical 4-bit gray code to binary coded decimal converter, Optical Components and Materials, Proceedings of the SPIE, Volume 6890, (2008), 68900S.

[21] B.C. Wang, V. Baby, W. Tong, L. Xu, M. Friedman, R.J. Runser, I. Glesk, P. R. Pruncnal, A novel fast optical switch based on two cascaded Terahertz Asymmetric Demultiplexers(TOAD), Optics Express 10(1), (2002), 15-23.

[22] Y.K.Huang, I.Glesk, R.Shankar, P.R.Prucnal, Simultaneous all-optical 3R regeneration scheme with improved scalability using TOAD, Optics Express, 14(22), (2006), 10339-10344.

[23] J.N.Roy, D.K.Gayen, Integrated all-optical logic and arithmetic operations with the help of TOAD based interferometer device – alternative approach, Appl. Opt. 46(22), (2007), 5304-5310.

[24] J. N. Roy, G. K. Maity, D. Gayen, T. Chattopadhyay, Terahertz Optical Asymmetric

[25] Demultiplexer based tree-net architecture for all-optical conversion scheme from binary to its other 2^n radix based form, Chinese Optics Letter 6(7), (2008), 536-540.

[26] S. Kotiyal, H. Thapliyal and N. Ranganathan, Mach-Zehnder Interferometer Based All Optical Reversible NOR Gates,Proceedings of the IEEE Computer Society Annul Symposium, Aug. 19-21, IEEEXplor Press,Amherst, MA.,pp:19-21.DOI:10.11.09/ISVLSI.2012.72.

[27] H. V. Jayashee, A. N. Nagamani, H. R. Bhagyalakshmi, Modified TOFFILI GATE and its Application in Designing Components of Reversible Arithmetic and Logic Unit, Volume 2, Issue 7, July 2012, ISSN: 2277 128X.