Low Power Efficient D Flip Flop Circuit

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ABSTRACT
This paper enumerates low power, high speed design of D flip-flop. It presents various techniques to minimize subthershold leakage power as well as the power consumption of the CMOS circuits. The proposed circuit in this paper shows a design for D flip flop to increase the overall speed of the system as compared to other circuits. This technique allows circuit to achieve lowest power consumption with minimum transistor count.

General Terms
D Flip Flop, Power Delay Product.

Keywords
Low Power, MTCMOS.

1. INTRODUCTION
Technology scaling of transistor feature size has provided a remarkable innovation in silicon industry for the last three decades. Designers are striving for small silicon area, higher speeds, low power consumption and reliability due to ever increasing demand and popularity of portable electronics. The dynamic power consumption is one of major factor that contributes in the power consumption of the digital systems. In order to minimize the dynamic power consumption the smaller geometries have been acquired which as a result has affected static power consumption. Dynamic power is proportional to the square of supply voltage, so reducing the voltage significantly reduces power consumption. The continuous scaling of device dimensions and threshold voltage in today's VLSI circuit has significantly increased sub threshold leakage currents exponentially. This has greatly increased the overall total power consumption. In recent nanometer CMOS technologies such as 90- and 45-nm, it is not uncommon to see leakage current being responsible for almost half of total power consumption. In 90nm node, leakage power can be as much as 35% of chip power. It is very necessary to reduce this power consumption as the use of portable devices and wireless system is enhancing day by day. These devices are much more complex than single VLSI chip. They have several components which may be digital or non digital. This is done at the system level to lengthen battery lifetimes for embedded applications. The battery service life is diminished by high power consumption. Hence, the power optimization techniques should be applied at different levels of the digital design. One of these techniques is to use low power logic styles which should be used in design of latches and flip-flops.

2. BRIEF LITERATURE RIVIEW
Figure 1 shows Single Threshold Transmission Gate flip flop. The D flip flop is constructed using CMOS transmission gates as shown in Figure 2. The first stage (master) is driven by the clock signal, while the second stage (slave) is driven by the inverted clock signal. Thus the master stage is positive level sensitive, while the slave stage is negative level sensitive.

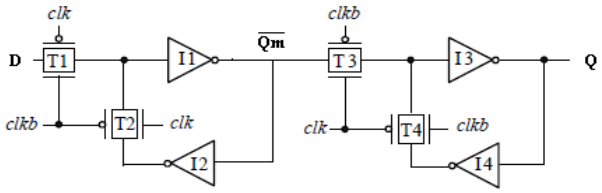

Fig 1: Single Threshold Transmission Gate Flip Flop

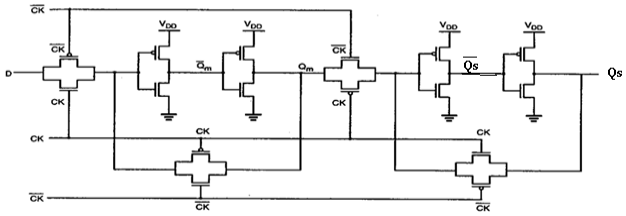

Fig 2: CMOS D-flip flop implementation.

When the clock is high, the master stage follows the D input while the slave stage holds the previous value. When the clock changes from logic "1" to logic "0", the master latch ceases to sample the input and stores the D value at the time of the clock transition. At the same time, the slave latch becomes transparent, passing the stored master value Qm to the output of the slave stage, Q. The input cannot affect the output because the master stage is disconnected from the input D. When the clock changes again from logic "0" to "1", the slave latch locks in the master latch output and the master stage starts sampling the input again. It is also known Single Threshold Transmission Gate flip flop. The block diagram is shown in Figure. 1. ST-TG FF is extensively used in sequential systems thus it is taken as a benchmark circuit for comparing the performances of the flip-flops in this paper. The TG-FF, is one of the fastest and low-power consuming flip-flop designs [1], [2].

The LFBFF is a multi-threshold CMOS (MTCMOS) storage device that retains its state even during sleep mode by

selectively maintaining an active path to power or ground. MTCMOS logic uses high V_T devices as power gating switches to reduce leakage current during sleep mode. The ability of the LFBFFs to cut off high leakage paths during sleep mode in an MTCMOS circuit means that any power savings from standby voltage scaling come in addition to the savings achieved by entering sleep mode. The combined use of MTCMOS sleep mode with standby voltage scaling can produce dramatic total reductions in power. A leakage feedback flip-flop (LFB FF) shown in Figure 3 applies the principles of the leakage feedback gate to a traditional master slave flip-flop [2], [7].

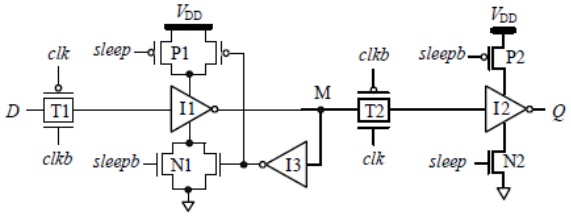

Fig 3: Leakage Feedback Flip Flop

A gate-length biasing flip-flop is shown in Figure.4, which is implemented with CMOS inverters and tri-state inverters. As CMOS technology is scaled, variations in gate length, oxide thickness, and doping concentrations are becoming more significant. If we employ gate-length biasing only to those transistors that are turned off when both D-input and Q-output are low, as shown in Figure 4, the leakage for the two states of the flip-flop can be made very different. The variation of the nominal gate length can change the leakage current and minimize it [3], [8].

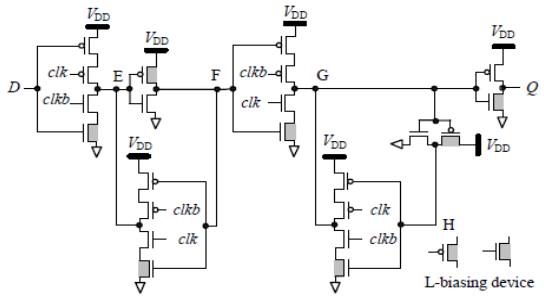

Fig 4: Gate Length Biasing Flip Flop

A more effective method of dealing with subthreshold leakage currents is to employ dual V_T technology, where the process has both high and low threshold voltage devices. By having two different flavors of devices, one can utilize specialized circuit topologies to take advantage of the speed benefits of low V_T as well as the leakage reduction benefits of high V_T devices. A dual V_T technique provides inherently fast and non-leaky devices that can be engineered through the process to provide the desired performance characteristics. Its structure is the same as a ST-TG FF, but a higher threshold voltage is assigned to the transistors in the blocks of Figure.5 to reduce its leakage current, which is used to hold the state. Dual Threshold Transmission Gate Flip Flop (DT-TG) consists of two paths, namely non-critical and critical. The circuits that hold the state use high-threshold transistors to reduce its leakage current. The performance is maintained due to the low-threshold transistors in the critical path. Moreover, no any additional dynamic power is caused, because no more transistors are added in the flip-flop [2].

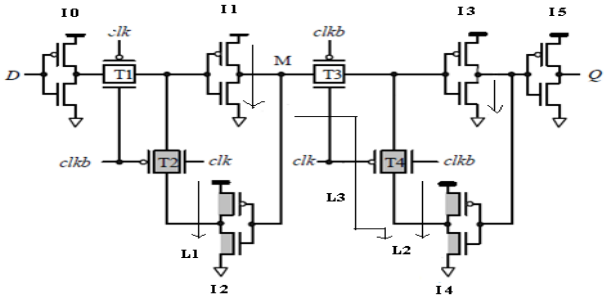

Fig 5: Dual Threshold Transmission Gate Flip Flop

3. PROPOSED DESIGN

Although the circuit shown in Figure 5 gives the least delay but provides very high power consumption. To overcome this drawback of that system we are proposing another design. By using the technique shown in Figure 6 the overall power consumption and power delay product is effectively reduced. This circuit is built by adding 2 sleep transistors in the 5 T Latch circuit. When CLK and input IN are high then the transistors M1, M5 are OFF and remaining transistors M2, M3, M4 are ON. The output becomes high. During ON clock period whatever is the value of input it becomes output. It also acts as a flip-flop when the input IN has less pulse width [5],[6].In this MTCMOS circuit sleep and sleepbar transistors are used which have high threshold voltages.

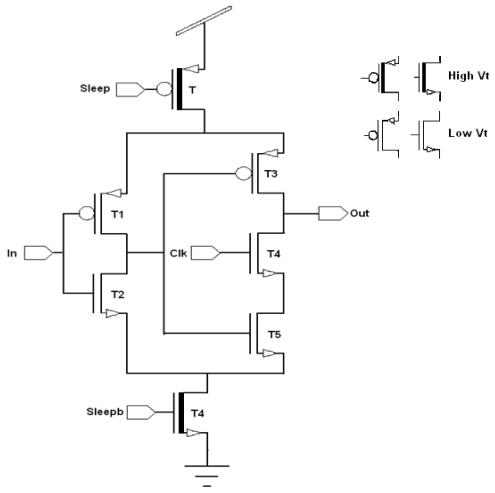

Figure 6: D Flip Flop using MTCMOS Technique

In the active mode, the high V_T transistors are turned on and the logic gates consisting of low V_T transistors can operate with low switching power dissipation and small propagation delay. When the circuit is driven into standby mode, on the other hand, the high V_T transistors are turned off and the conduction paths for any subthreshold leakage currents that may originate from the internal low circuitry are effectively cut off [4],[9].

4. SIMULATION ANALYSIS

4.1 Simulation Environment

All the circuits have been simulated on BSIM3V3 90nm technology on tanner EDA tool. To establish an impartial testing environment each circuit have been tested on the same input patterns.

4.2 Simulation Comparison

In this section various D flip flops are compared in terms of delay, power consumption and power delay product.ST-TG FF is taken as a benchmark circuit for comparing their performances in this paper. Table 1 and 2 shows the delay produced by the various D flip flops at different Vdd. It is clear from Table 1 and 2 that at higher values of Vdd the ST-TG has least delay as compared to other circuits and at lower values of Vdd the least delay is observed in DT-TG circuit.

Table 1. Delay (Sec) Comparison of D Flip Flops

Vdd	ST-TG	LF-TG	GLB
1	1.96E-08	2.25E-08	2.02E-08
1.2	1.99E-08	1.07E-08	1.99E-08
1.4	1.99E-08	9.41E-09	2.00E-08
1.6	4.27E-10	1.01E-08	2.00E-08
1.8	8.68E-10	1.04E-08	1.99E-08
2.0	9.71E-09	1.05E-08	1.99E-08

Table 2. Delay (Sec) Comparison of D Flip Flops

Vdd	DT-TG	8T	MTCMOS
1	4.62E-10	7.20E-09	1.98E-08
1.2	7.15E-10	1.06E-08	1.99E-08
1.4	7.68E-10	1.00E-08	2.00E-08
1.6	9.86E-09	1.00E-08	2.00E-08
1.8	8.68E-10	1.04E-08	1.99E-08
2.0	9.71E-09	1.05E-08	1.99E-08

Power Consumption of flip flops is listed in Table 3 and 4. The minimum power consumption is observed in the MTCMOS circuit i.e. the proposed design.

Table 3. Power Consumption (Watt) Comparison of D FF's

Vdd	ST-TG	LF-TG	GLB
1	2.83E-06	2.45E-06	7.20E-07
1.2	6.67E-06	3.89E-06	1.68E-06
1.4	1.19E-05	5.74E-06	3.36E-06
1.6	1.42E-05	8.55E-06	5.64E-06
1.8	2.62E-05	1.24E-05	1.82E-05
2.0	6.79E-05	1.63E-05	3.18E-05

Table 4. Power Consumption (Watt) Comparison of D FF's

Vdd	DT-TG	8T	MTCMOS
1	1.20E-05	5.20E-07	1.17E-07
1.2	5.28E-05	1.04E-06	1.98E-07
1.4	1.24E-04	1.78E-06	1.32E-06
1.6	2.04E-04	2.56E-06	5.06E-07
1.8	3.47E-04	3.50E-06	7.66E-07
2.0	9.30E-02	4.58E-06	1.12E-06

Figure 7 and 8 shows variation between power supply Vdd and power delay product of flip flops. It can be seen in Figure 7 that LF-TG has steady low PDP in contrast to other circuits. Whereas in Figure 8 it can be analyzed that MTCMOS circuit has better performance as the PDP is constant in range 1 to 2 V of power supply Vdd.

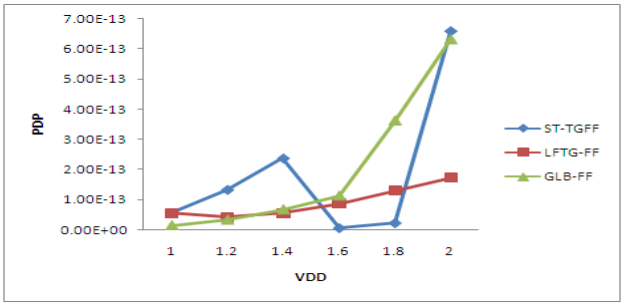

Fig 7: Variation of PDP Vs V_{dd} for various Flip Flops

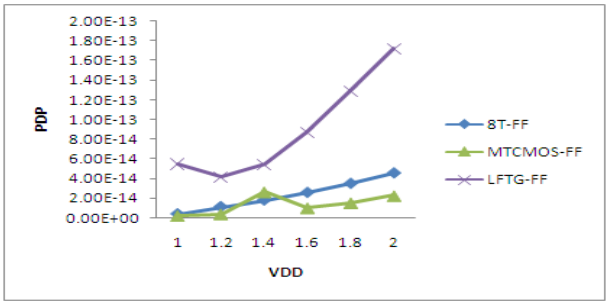

Fig 8: Variation of PDP Vs Vdd for various Flip Flops

5. CONCLUSION

For low power applications the scaling of Vdd is done to obtain optimum results. Therefore DT-TG circuit can be use for low values of supply voltage. Although it has high speed and lower delay but it offers more power consumption. Minimization of power consumption is essential for high performance VLSI systems. In order to have lower power consumption we use MTCMOS circuits. Here the proposed circuit described in Figure 6 has lesser power consumption than other circuits because it has few transistor count. PDP is calculated for all circuits. Among these MTCMOS FF is having least power delay product; therefore its performance is the best. It achieves considerable energy savings over the other similar implementations. This design idea could provide a significance reference that would guide the design of the other circuits.

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