Power Optimal Design of SRAM in 90 nm

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ABSTRACT
Low threshold voltage and ultra thin oxide become essential in power optimal VLSI circuit design. This paper analyzes the effect of dual thickness and dual threshold on static random access memory (SRAM) leakage power. The different hybrid cell configurations are analyzed for power optimal design of SRAM in 90nm technology node. Cell ratio of SRAM is an essential parameter for area centric SRAM design. It also decides the non destructive read operation of SRAM cell. Variation of cell ratio has also been analyzed. The effect of voltage-scaling is also analyzed for SRAM cells. It is found that voltage-scaling reduces the energy consumption but at the cost of read and write delay in SRAM cells.

General Terms
Conventional SRAM, hybrid SRAM, and leakage reduction.

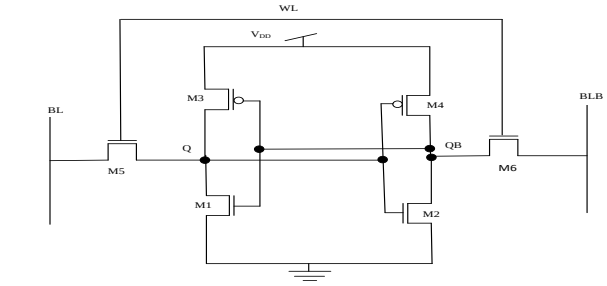
Keywords
Cell Ratio, Read Current, Write Delay, PDP, Voltage Scaling.

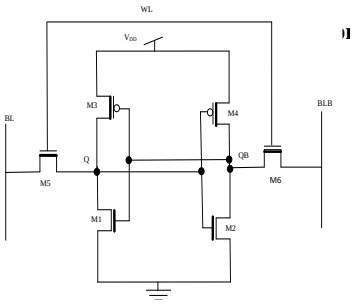
1. INTRODUCTION
In the current VLSI digital circuits, power consumption is one of the main design concerns. Static RAM plays a key role in modern electronics gadgets as the technology scales down and the need for high performance in very deep sub-micron CMOS design is on the increase. As the size of the SRAM enters nanometer regime the variations in electrical parameters viz. threshold voltage reduces. The reduction is steady due to the sensitivity in process parameters i.e. density of impurity concentration, oxide thickness and diffusion depths. The data retention of the SRAM cell in hold state and the read state are important constraints in advanced CMOS technology nodes. The SRAM cell becomes less stable at low supply voltage (V_{DD}), with increasing leakage currents and variability. The stability is usually defined by the static noise margin (SNM) as the maximum value of the DC noise voltage that can be tolerated by the SRAM cell without altering the stored bits. SNM deteriorates with decrease in supply voltage and increases with the transistor mismatch. This mismatch occurs due to variations in physical quantities of identically designed devices i.e. their threshold voltages, body factor and current factor. Though, the SNM decreases for low V_{DD}, the overall SRAM delay increases. Moreover, the read operation at low V_{DD} leads to storage data destruction in SRAM [1-2].

CMOS scaling requires not only very low threshold voltages to retain the device switching speeds, but also ultra-thin gate oxides to maintain the current drive and keep threshold voltage variations under control when dealing with short-channel effects [3]. Low threshold voltage results in an increase in the sub

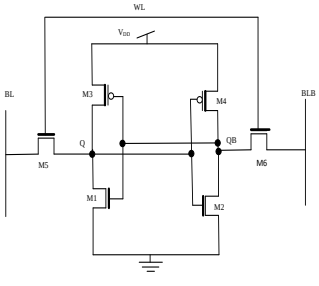
threshold leakage current, whereas ultra-thin oxide causes an increase in the gate leakage current. Consequently, one way to reduce leakage current is to increase threshold voltage. In literature, a number of techniques are reported to increase threshold voltage. Of this threshold voltage can be increased by body bias technique and channel doping concentration [4]. To reduce gate tunneling current, oxide thickness needs to be increased. Increase in oxide thickness in turn increases threshold voltage. Therefore it reduces both sub-threshold leakage and oxide leakage current. In literature, various researchers have reported on CMOS leakage problem [5-9].
Cell ratio is an important parameter to determine the SRAM area. Cell ratio also decides whether a read operation is destructive or not. Silicon area is always an important concern and it needs to be minimized. These techniques have been employed and cell ratio has been optimized in SRAM analysis in the present work. The rest of paper is organized as follows: section 2 gives the conventional SRAM cell. In section 3 hybrid SRAM cells have been described. Results and discussion have been presented in section 4. Finally conclusions are drawn in section 5.

2. CONVENTIONAL SRAM
The functionality and design issues of SRAM are detailed in [10-11]. Figure 1 shows a 6T CMOS SRAM cell, where WL is wordline, BL is bitline, BLB is bitline bar, Q and QB (Q bar) are node voltages. The values stored on the Q and QB nodes remain preserved as long as supply voltage connected to SRAM is greater than data retention voltage. SRAM holds the value due to cross coupled inverters formed by M1, M3 and M2, M4 respectively. M5 and M6 are access pass transistors required for read and write operation. SRAM needs to be sized properly for read and write stability.

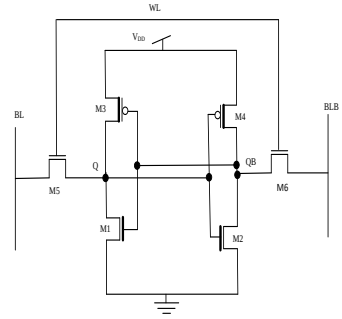




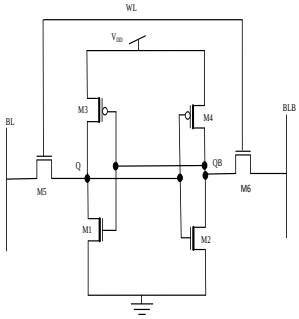
C1 Cell



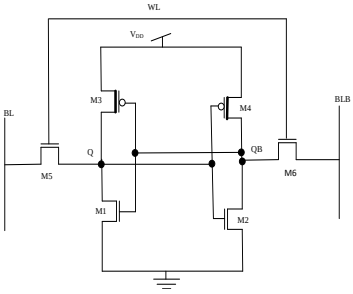
C2 Cell



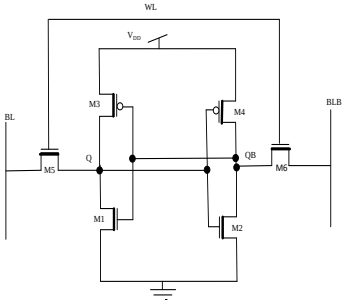
C3 Cell



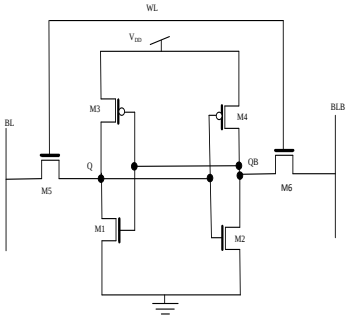
C4 Cell



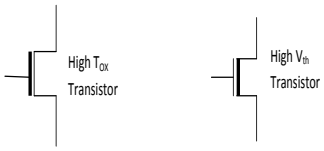
C5 Cell



C6 Cell



C7 Cell



The symbols in cell C1 to C7 represent the use of above two transistors i.e. bold line on gate is for high T_{OX} and bold line on channel is for high V_{th}

Figure 2: Hybrid SRAM Configurations [12]

3. HYRID SRAM CONFIGURATIONS

The concept of hybrid SRAM configurations is reported in literature [12]. Two types of leakage currents are considered viz. sub threshold current and gate tunneling current. The sub-threshold current can be decreased by increasing threshold voltage and gate tunneling leakage current can be decreased by increasing oxide thickness in the hybrid configurations. In 6T SRAM, different thickness and threshold voltages are assigned to reduce the leakage power. Change in pull down transistor affects the read delay and change in pull up transistor affect the write delay. Different configurations are used to optimize the performance. In Figure 2 only a few best combinations are shown out of the total 32 possible combinations. It has been shown in Figure 2 that in C1 cell, pull down transistors have high oxide thickness whereas pull up transistors have high threshold voltage and both access transistors have high threshold voltage. Pull down and both access transistors have high oxide thickness and the pull up transistors have high threshold voltage in cell C2. Access transistors remain unchanged in case of cells C3, C4, and C5. In cell C3 pull down transistors have high oxide thickness and pull up transistors have high threshold voltage whereas in cell C4 both pull down and pull up transistors have high threshold voltage. In cell C5, only pull up transistors have high threshold voltage. In present work two extreme cases have also been considered. In SRAM cell C6 all transistors have high threshold voltage whereas in SRAM cell C7 all transistors have high oxide thickness.

4. RESULTS AND DISCUSSION

In this section, the results for various SRAM cells are presented for an optimal cell ratio. The simulations are carried out for 90nm technology node for PTM model using TSPICE tool [13-14].

4.1 Cell Ratio in SRAM Cells

The maximum allowed voltage value 0+ΔV of the node Q or QB storing logic "0" during read access given as [14].

$$\Delta V = \frac{V_{sat,n} + CR(V_{DD} - V_{th,n}) - \sqrt{V_{sat,n}^2(1+CR) + CR^2(V_{DD} - V_{th,n})}}{CR} \quad (1)$$

where CR is cell ratio, $V_{sat,n}$ is drain to source voltage of NMOS in saturation region, V_{DD} is supply voltage. The cell ratio (CR) is given as [15]

$$CR = \frac{W_1 / L_1}{W_5 / L_5} = \frac{W_2 / L_2}{W_6 / L_6} \quad (2)$$

where W_1/L_1, W_2/L_2, W_5/L_5, and W_6/L_6 are the aspect ratio for M1, M2, M5, M6 MOSFETs respectively in Figures 1 and 2.

The value of CR should be [16]

$$CR > \frac{2(V_{DD} - 1.5V_{th,n})V_{th,n}}{(V_{DD} - 2V_{th,n})^2} \quad (3)$$

To ensure a non-destructive read operation cell ratio must be greater than 1. Read current increases with increase in cell ratio. But higher CR increases the cell area. A smaller cell ratio ensures moderate read speed with moderate cell area. It can be seen in Figure 3(a) that read current increases with increase in cell ratio. It also has been observed from Figure 3(a) that hybrid SRAM cells C2 followed by C4 have considerably lesser read current compared to standard SRAM cell C0. Write delay decreases with increased cell ratio as observed from Figure 3(b). In present case the safe value for CR is 2.1. The different hybrid SRAM cells have been analyzed with CR of 2.2.

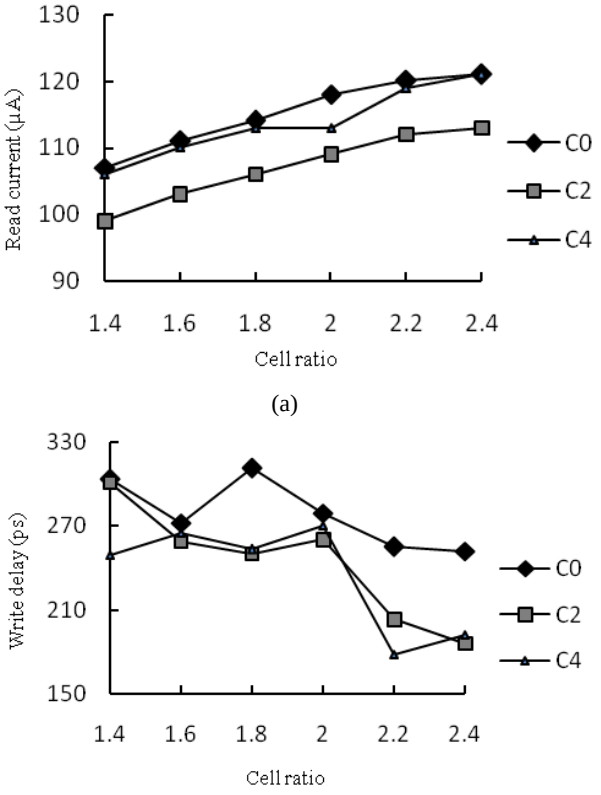


Figure 3: a) Read current and b) Write delay variations with cell ratio for C0, C2, and C4 SRAM cells

4.2 Process Corners

In semiconductor manufacturing, a process corner is an example of a design-of-experiments (DoE) technique that refers to variation of fabrication parameters used in applying an integrated circuit design to a semiconductor wafer. Process corners represent the extremes of these parameter variations within which a circuit on the silicon wafer must function correctly. A circuit running on devices fabricated at these process corners may run slower or faster than specified and at lower or higher temperatures and voltages. However, if the circuit does not function at all at any of these process extremes the design is considered to have inadequate design margin. One of the naming conventions for process corners is to use two-letter designators, where the first letter refers to the N-channel MOSFET (NMOS) corner, and the second letter refers to the P channel MOSFET (PMOS) corner. For example TT, FF, and SS
refer to both NMOS and PMOS being typical, fast or slow respectively. In this naming convention, three corners exist viz. typical, fast and slow. Fast and slow corners exhibit carrier mobility that is higher and lower than normal or typical respectively. In the present work typical, fast, and slow process corners have been analyzed and named as such [17].

4.3 Write Delay

The effect on write delay for different SRAM cells is seen in Figure 4. Write delay is mainly affected by pull up transistors. Access transistors affect both write and read delay. Hybrid SRAM cell C4 has least write delay of 178ps among all SRAM cells in typical process corner and cell C3 and C2 has fastest write operation among all hybrid SRAM cells in fast and slow process corners showing a write delay of 252ps and 132ps respectively.

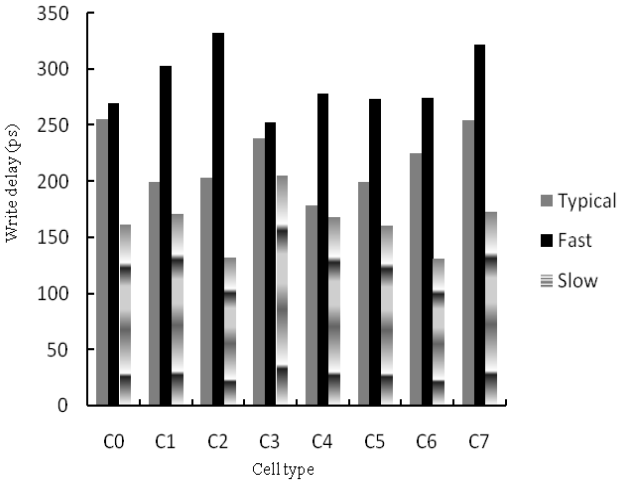


Figure 4: Variation in write delay for different SRAM cells

4.4 Read Delay

Read current indirectly show how fast the read operation is. Read delay is not greatly affected by pull up transistors. Figure 5 shows the variation of read current for different hybrid SRAM cells. More read current means less read delay or indirectly it can be said that it will have faster read operation. All cells have nearly comparable read delay. Hybrid SRAM cell C7 has least read current among different hybrid SRAM cell in all three process corners as shown in Figure 5. It can be said that cell C7 is the slowest cell among all SRAM cells.

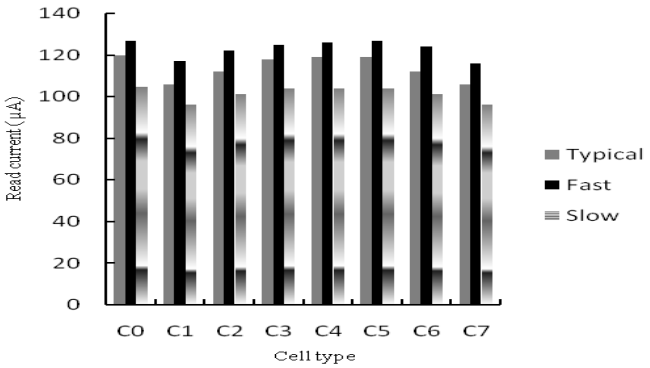
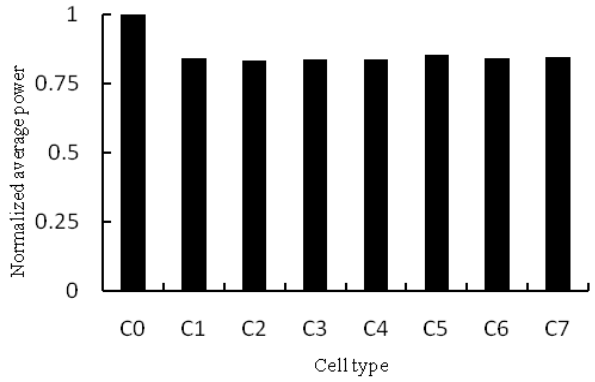


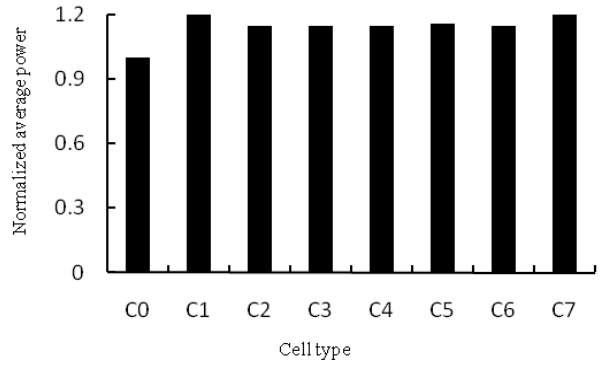
Figure 5: SRAM Cell type versus read current

4.5 Average Power

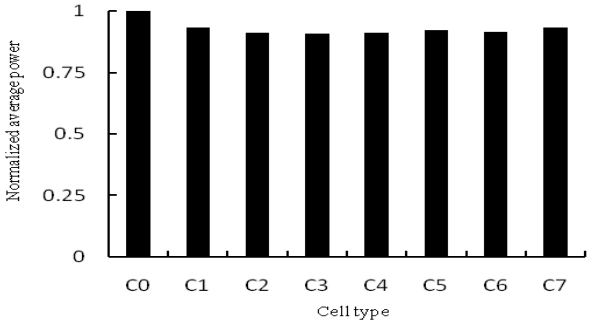
The trends for normalize average power consumed in different SRAM cells is seen in Figure 6. The power consumed is normalized with respect to the power for stanadard SRAM cell (C0). Simultions are carried out for all the three process cornners. It can be seen from Figure 6(a) that SRAM cells C2, C3, and C4 have nearly 17% reduction in total average power in typical process corner. Fast corner give contradictly results as seen in Figure 6(b). As shown in Figure 6(c) SRAM cell C3 has 10% reduction in average power whereas cell C2 and cell C4 has nearly 9% reduction in average power as compared to SRAM cell C0.



(a)



(b)

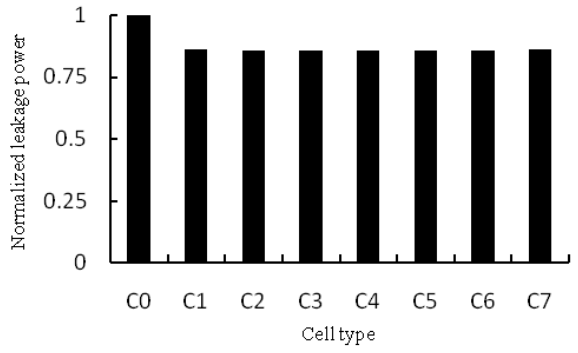


(c)

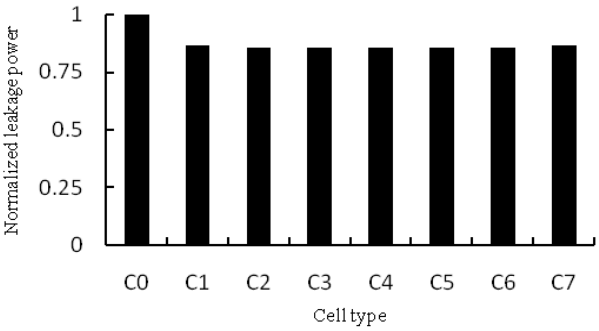
Figure 6: Normalized average power for various hybrid SRAM cells a) Typical, b) Fast and c) Slow process corners

4.6 Leakage Power

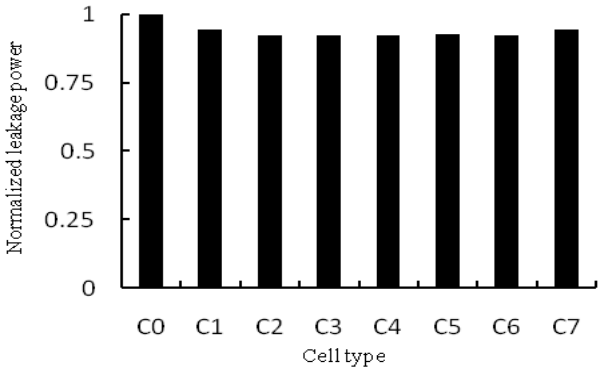
A large fraction of power is consumed in hold state. This is called leakage power.Figure 7 shows the normalized leakage power in different SRAM cells. Normalization has been carried out with respect to cell C0. All hybrid SRAM cell configurations show a large amount of reduction in leakge power. It can be seen from Figure 7(a) that hybrid SRAM cells C2, C3, and C4 have nearly 15% reduction in leakage power in typical process corners. In Figure 6(b) SRAM cells C2, C3, and C4 have 6.5%, 6.5%, and 6.3% leakage power reduction respectvely in fast process corner. SRAM cells C2, C3, and C4 have 7.5% leakage power reduction in slow process corners as seen in Figure 7(c).



(a)



(b)

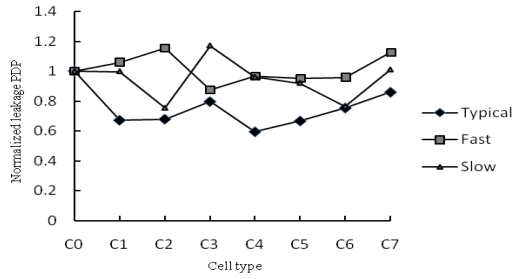


(c)

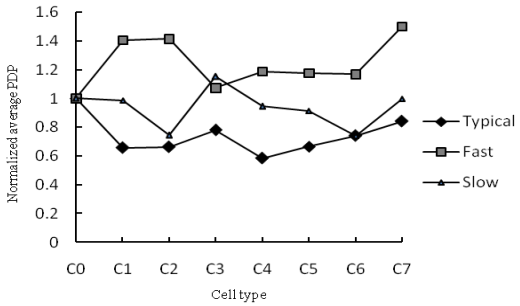
Figure 7: Leakage power variations in hybrid SRAM cells for a) Typical, b) Fast and c) Slow process corners

4.7 PDP Variation in Hybrid SRAM Configuration

Power_delay_product (PDP) is an important performance metric for electronic circuits. It is a measure of energy consumption. Lower PDP value ensures energy efficient design. In Figure 8 different SRAM cells are optimized using PDP. In Figure 8(b) PDP is computed using total average power, whereas in Figure 8(a) only leakage power is used. Here also normalization is done with respect to C0. Hybrid SRAM Cell C4 has nearly 41.5% reduction in total energy consumption and 40.4% reduction in leakage energy as compare to standard SRAM cell.



(a)



(b)

Figure 8: Normalized power delay product (PDP) variation for (a) leakage power and b) average power for various SRAM cell configurations

4.8 Effect of Voltage Scaling

The effect of voltage scaling on the read current and write delay of SRAM cells is also analyzed. These are shown in Tables 1 and 2, for cells C2 and C4 respectively. As voltage is scaled down to reduce power consumption, there is decrease in read current and increase in write delay. Tables 1 and 2 show the increasing trend of write delay and decreasing behavior of read current for cell C2 and C4 respectively. SRAM cells get slow due to voltage scaling; however the power consumption decreases by order 3 in case of C2 and C4 SRAM cell respectively as voltage is scaled down from 1.2V to 0.3V but at the cost of speed.

Table 1. Voltage scaling effect on cell C2

V_{DD} (V)	Read current (µA)	Write delay (ps)	Avg Power (µW)
1.2	112	203	99.08
0.9	66	218	22.88
0.6	21	324	.42
0.3	0.3	5429	.03

Table 2. Effect of voltage scaling on cell C4

V_{DD} (V)	Read current (µA)	Write delay (ps)	Avg Power (µW)
1.2	99.60	178	99.60
0.9	22.91	210	22.91
0.6	0.420	301	.42
0.3	0.031	4300	.031

5. CONCLUSIONS

Six transistors CMOS SRAM cells have been analyzed using dual oxide and dual threshold technique. Two threshold voltages (typical and high) and two values of oxide thickness (typical and thick) in a single CMOS have been used. These do increase the fabrication cost, but lead to better performance of SRAM cells. All hybrid cells have very low leakage power consumption in comparison with standard SRAM. However, there is some increase in write and read delay. Power_delay_product is considered the figure of merit and all cells are optimized for least PDP. The effect of cell ratio and voltage-scaling on SRAM performance has been analyzed. Simulations are carried out using different process corners which show the fabrication and functional feasibility.

6. ACKNOWLEDGMENTS

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