Stability Analysis of 6T SRAM Cell at 90nm Technology

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ABSTRACT
SRAM is the most crucial part of memory designs and are imperative in many simple or compound applications that implicate system on chip (SoCs). Power dissipation and stability has now become the most essential area of concern in sub-micron SRAM cell design with continuous technology scaling according to Moore's law. At latest, retrenchment of channel length MOSFET is directly proportional to the new technologies generating step by step with new innovative tools. With an improvement in technology there is a sudden retrenchment of channel length of MOSFET. Moreover, in this network of stability SRAM has become very essential and major area to research in. Static noise margin generate its crucial role in the stability of SRAM. This paper introduce to the basic 6T SRAM cell. The outperforms of this SRAM cell in elaboration with transient response and static noise margin is described with the counter fit results using the EDA tool Custom Designer at 90nm CMOS Technology.

Keywords
Static random access Memory (SRAM), CMOS, Static Noise Margin (SNM), Read noise margin, Write noise margin, wordline, bitline.

1. INTRODUCTION
The power efficient processor has become a need with an increase in the imposition of portable devices. In the idle mode, the leakage of power has become a great problem mostly in the portable devices that are managed by batteries. In the memory design, the Static Random Access Memory SRAM is the major component of the computing circuits. In nanometer design many design challenges occurs due to device scaling. In most of SRAM cell the read and write operations are separated from each other to attain the better performance. Power consumption of SRAM component must be reduced and has been under broad investigation in the technical literature. The most forceful approaches to meet this objective are to design SRAM cells whose operation is ultra-low power. Latter presented works have shown that the Conventional 6T SRAM deteriorates severe stability degradation due to access disruption at low–power mode. The intention of this paper is to determine the effect of certain circuit parameters on the SNM of 6T SRAM Cell designed in 90nm process technology. All the simulation has been done on 90nm technology. Tool used to take the simulation is Custom designer.

2. BASIC 6T SRAM CELL
In Conventional 6T Static Random Access Memory (SRAM) which is a type of semiconductor memory, a bistable latching circuit is used to store a bit/data. Including two CMOS made of 4 transistors, 6T SRAM consists of 6 transistors. It has two access transistors to control the access to a storage cell during read and write operations. Word line contributes to the access passage to the cell that moreover further controls the two access transistors N3 & N4 that are connected to the bit line BL and bit line bar BL BAR. The bit lines functions as I/O buses that carry and store the data for both reading and writing operations. The noise margin of the cell is improved by inverse of bit line.

2.1 Basic Operation
The three operating modes of SRAM are hold, read and write. In hold mode, the cell from the circuits disconnected by the access transistors N3 and N4. To maintain the cross coupled invertors in active state, the power supply connection is not disconnected and the word line is not pronounced. First a positive pulse line is applied to word line then the store bit is transferred from q and qbar to bit lines in the read mode. In the write mode, the desire data that has to be written in the cell is applied to the bit line BL and complimentary of that data signal is applied to bit line bar i.e. BLB. Thus by making word line WL asserted the write operation is performed successfully. The Schematic diagram of 6T cell is shown in Fig 1 and simulation waveform of basic SRAM operation is shown in Fig 3.

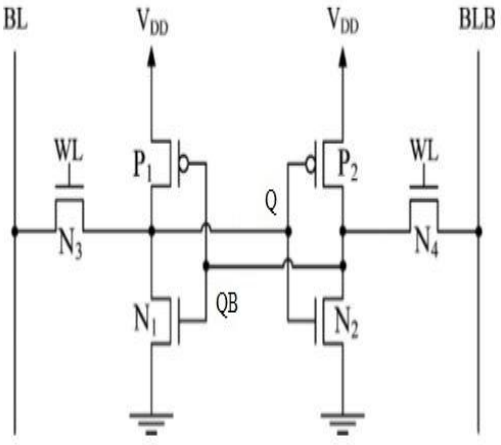

Fig: 1 6T SRAM Cell

2.2 Sizing of 6T SRAM cell
The transistor sizing of PMOS and NMOS in 6TSRAM plays a very important role in achieving the best performance in its operation. The ratio of access transistor is always kept higher than the PMOS transistor to achieve good layout density in the memory designs. Focusing on the high stability during read operation, the ratio of access transistor (N3) and NMOS Pull down (PUD) transistor (N1) is kept more than 1.2 during read operation.

3. STABILITY IN TERMS OF READ AND WRITE MARGIN
The traditional 6T-cell schematic is shown in Figure 2. This most regularly used SRAM cell implementation has the merit

of very less area.

However, the potential stability issue of this design occurs during read and writes execution where the cell is most unsafe towards noise and thus the stability of the cell is sensitized. If the cell structure is not designed properly, it may flip its state during read and write operation. There are two types of noise margin which affects the stability of cell that are explained shortly.

3.1 Read Static-Noise Margin

During read approach, the Read-SNM decreases [8]. This is due to the logic that Read-SNM is computed when the word line is set high and both bit line are fixed precharged high. At the onset of a read access, the access transistor (WL) is set to "1" and the bit-lines are earlier precharged to "1".The internal node of the bit-cell representing a zero gets forced higher through the access transistor due to the voltage dividing effect across the access transistor and drive transistor. Thus the SNM during read operation degrades due to this increase in voltage as shown in the Figure 3. meanwhile the read operation, a stored "0" can be overwritten by a "1" when the voltage at node V1 reaches the V_{th} of nMOS N1 to pull node V2 down to "0" and in turn pull node V1 up even further to "1" due to the functioning of positive feedback. This results in false read access or a destructive read when the cell changes state [3].

3.2 Write Static-Noise Margin

The write noise margin is described as the minimum bitline voltage needed to flip the state of cell. At the time a write operation, the input data are forward towards the bitlines and then the word lines are activated to access the cell. The bitline that is charged to '0' force the node of the cell storing '1' to '0' causing the cell to flip state. By reason of the cross-coupled inverters have complementary data so their VTCs are calculated using different circuits. The circuit that performs the inverter with '1' at its output and its bit line is connected to GND to simulate a write '0' to that node. A DC voltage sweep is forced at node V1 and the voltage output at node V2 is measured, when the bit line (BL) is connected to GND and word line (WL) is charged to V_{dd}.

4. EFFECT OF DEVICE PARAMETERS ON SNM OF SRM CELL

To reform stability of the Conventional 6T SRAM, SNM of the circuit should be improved. Many circuits having larger transistor count i.e. 8T, 9T etc. have been carried out. The SNM can be boost by taking larger transistor count but speed gets degraded. Power consumption rose up and the possibility of switching activity factor rises with increasing number of transistor resulting in large silicon area. Due to the need of battery operated device, the scaling in CMOS technology never ceases. So there is a modification of 6T SRAM cell to attain the optimum cell stability by modifying supply voltage, cell ratio, pull-up ratio and word line voltage modulation. These modifications show a drastic change in the static noise margin curves.

5. EXPERIMENTAL ANALYSIS

Simulation of the 6TSRAM is performed using HSPICE at 90nm technology. Circuits have been simulated on the same input patterns at the supply voltages of 1.8V for 90nm technology.

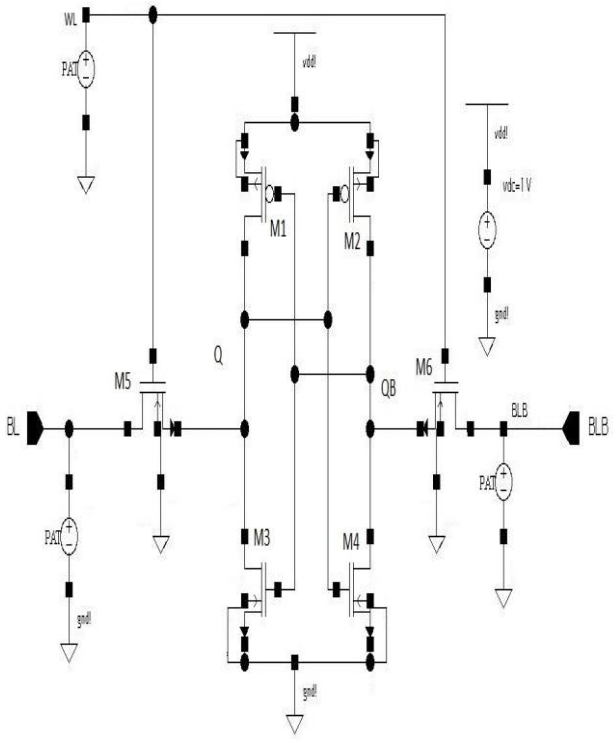

Fig: 2 Schematic of 6T SRAM Cell

5.1 Transient response

Now we will discuss the transient response of the proposed SRAM cell, the timing diagram in the write mode of 6T SRAM cell is shown in Figure 3 for a 1.8V and 90nm CMOS technology. The bit line and bitline bar is the input data that has to be written in the SRAM cell. The wordline data define the write operation of the cell. When the wordline signal is high then the write operation will be performed. If the wordline signal is low then cell will perform HOLD operation and the previous data will be maintained in the cell as shown in fig.3. The Q and QB specify the data has been written in the cell. These two nodes are also known as output storage node and both are complimentary to each other means if storage node Q stores '0' bit then QB will store '1' bit.

Table 1.Simulation results for write delay and average power

SRAM cell	Technology node	Power supply	Write delay	Average power
6T	90nm	1.8V	9.47ps	0.104µw

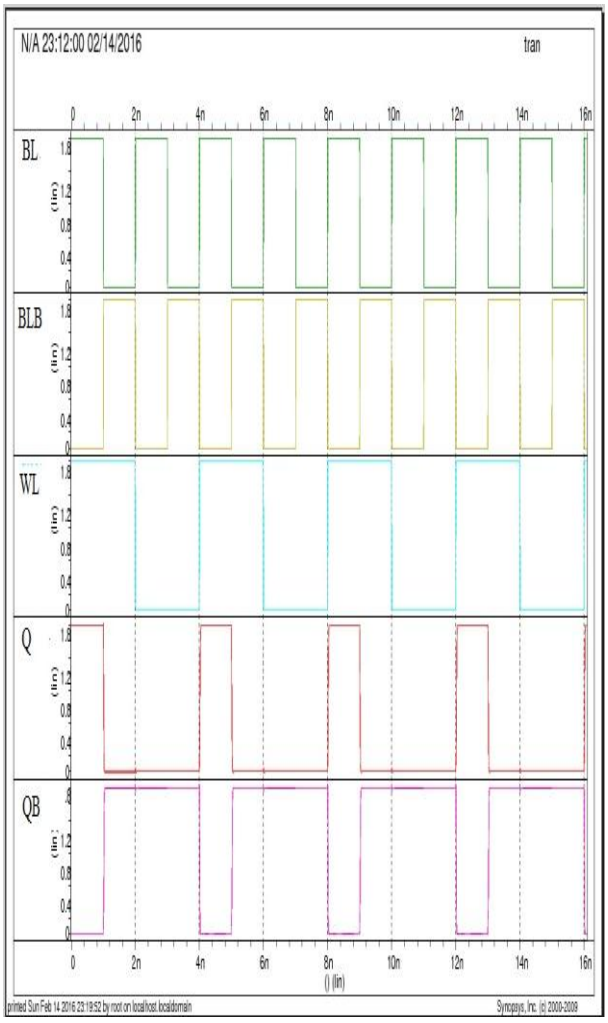

Fig: 3 Transient Response of 6T SRAM Cell

5.2 Static Noise Margin

The performance of SRAM cell in nanotechnology regime is highly dependent on its stability. The stability of SRAM cell is depends upon the static noise margin. The stability of SRAM during read and write operation can be determined by measuring Static Noise Margin (SNM). A basic SNM depends upon butterfly curve formed by mirroring inverter characteristic and finding maximum possible square between them. E. Seevinck [1] has proposed two methods to measure SNM called trial and error method and graphical method. In this paper, stability of SRAM cell is calculated using graphical method

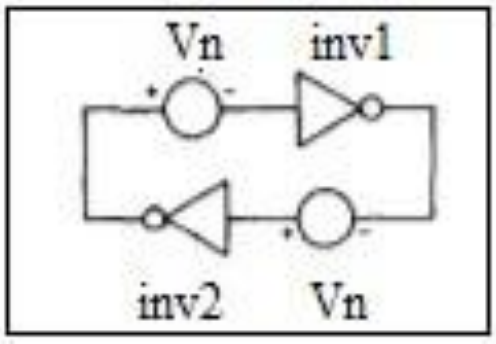

Fig: 4 Standard setup to calculate SNM

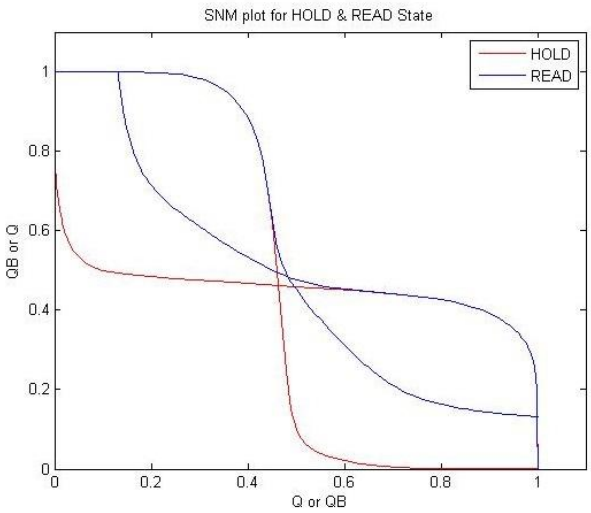

Fig: 5 SNM plot for HOLD & WRITE state

5.3 Cell ratio vs. Read Static Noise Margin

Cell ratio is described as ratio between the sizes of the driver (pull down) transistor to the size of access transistor.

CR (r) = Size of pull down transistor / Size of access transistor

Effect of cell ratio on READ SNM is shown in Fig.6. The cell ratio affects the stability of SRAM Cell during read operation. The read noise margin, increases with increasing the cell ratio. To keep cell area within reasonable values, we restrict the values of Cell ratio (r) and pull up ratio (q) between the minimum 1, and a maximum of 2.5, (i.e. rmax = qmax = 2.5).

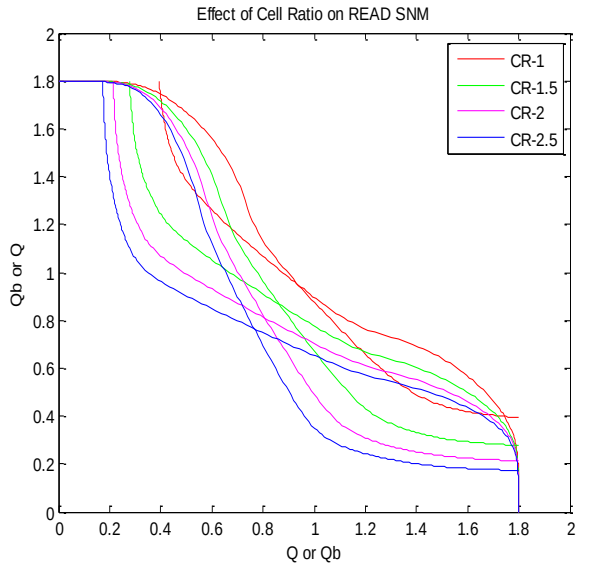

Fig: 6 Effect of cell ratio on READ SNM

5.4 Pull up ratio vs. Write Static Noise Margin

Ratio between sizes of the load transistor (pull up) to the size of access transistor is termed as pull up ratio.

PR (q) = Size of pull up transistor / Size of access transistor

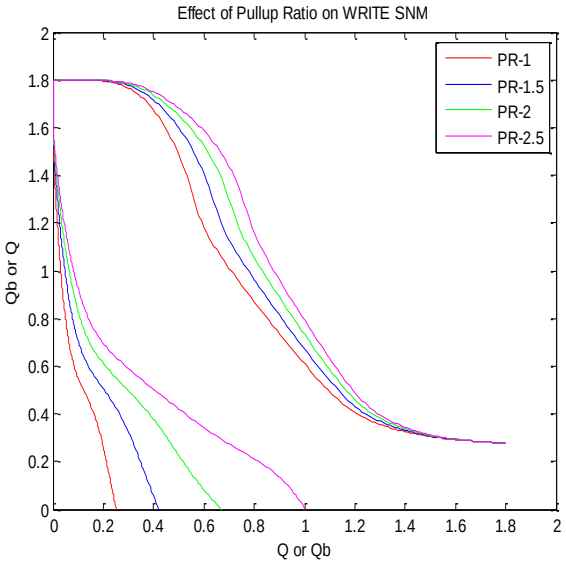

Fig: 7 Effect of cell ratio on WRITE SNM

The pull up ratio affects the stability of SRAM Cell during write operation. Fig.7 demonstrates the effect of cell ratio on Write SNM. During write operation, the critical part of the circuit is the voltage divider formed by the pull up and access transistors whose size ratio defines the pull-up ratio. The bitline pulled to GND pulls the node storing '1' to GND to flip the state. The strength of the pull-up transistor determines the difficulty of writing data or flipping the state of cell. With increased pull-up ratio, it is more difficult to write or pull the node to GND and hence the write margin and write trip voltage is decreased. Thus increasing the pull up ratio during write is of no good as it increases the difficulty in writing data into the SRAM Cell.

5.5 Supply voltage scaling effect

The effect of power supply modulation is crucial parameter which revises the cell stability during read mode and has been widely acceptable. It is superior that the supply voltage must be maximizing for increase SNM and also for cell stability. For this analysis, the supply voltage is varied from 0.2V to 1.8V. The noise margin for all operations is proportional to the supply voltage. Voltage scaling confine the level such that noise margin is still greater than the expected noise margin. The consequences of decreasing supply voltage on Read SNM and Write SNM is as shown in Figure 7.

5.5.1 Effect of Voltage Scaling on SNM

It is clear from the SNM plot is that as we scale down the supply voltage to the SRAM bit cell, the SNM value decreases thus the stability of cell also reduces. Fig. 8 shows the voltage scaling effect on HOLD SNM. Fig.9 demonstrates the effect on Read SNM of voltage scaling.

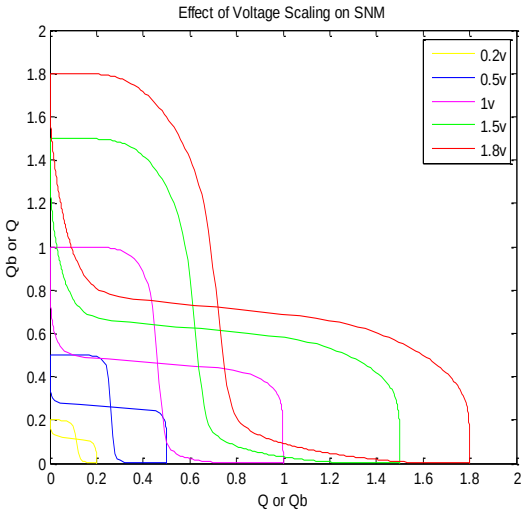

Fig: 8 Voltage scaling effect on HOLD SNM

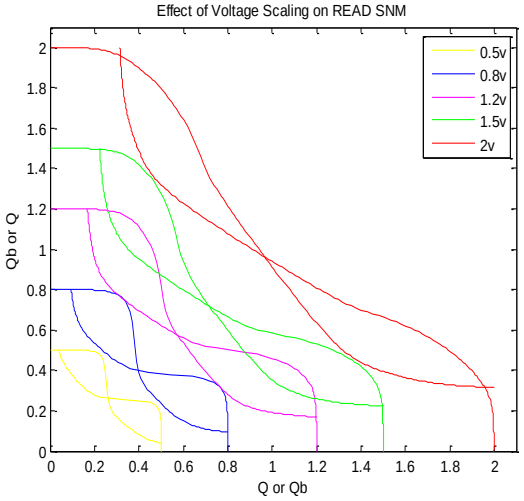

Fig: 9 Voltage scaling effect on READ SNM

5.5.2 WORD LINE Voltage Scaling Effect

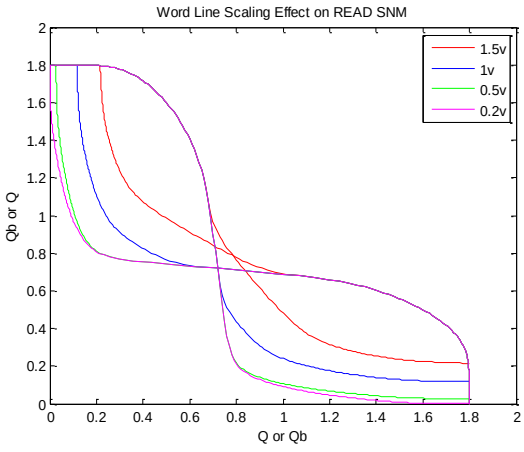

Fig: 10 Wordline voltage scaling effect on READ SNM

For the low power supply, with the help of wordline modulation the SRAM cell stability can be increased. This approach is based on compressing the maximum voltage surge of the wordline to maintain the cell during read operation. The

wordline voltage is varied from 0.2V to 1.5V and the effect on Read SNM is as shown in Figure10. It can be seen that as we limits the Wordline Voltage, the Stability of the SRAM Cell is improved.

6. CONCLUSION

The simulation results, discussed above improve the Read SNM and Write SNM of Conventional 6T SRAM Cell. The higher SNM can be achieved by modifying the device parameters of conventional 6T SRAM cell without requiring any modification of the SRAM cell array design. The Modified 6T can be used as a cache memory in internal CPU. It also maintains its Read-SNM at higher temperature range, thus it can be used in Industry and Military purposes also. So to overcome the SNM problem confront with conventional 6T SRAM cell and to avoid the area overhead occurred due to additional transistors, we have proposed a method of introducing the effect of device parameters for improving the Static-Noise-margin of Conventional 6T SRAM Cell.

7. REFERENCES

[1] E. Seevinck et al., "Static-Noise Margin Analysis of MOS SRAM Cells," IEEE J.Solid-State Circuits, vol.SC-22, no.5 pp.748-754, Oct. 1987.

[2] E. Grossar "Read Stability and Write-Ability Analysis of SRAM Cells for Nanometer Technologies", IEEE J.Solid-State Circuits,vol.41,no.11 ,pp. 2577-2588,Nov. 2006.

[3] S.Birla et a.l."Static Noise Margin Analysis of Various SRAM Topologies"IACSIT,pp.304-309,vol.3,No.3,june 2011.

[4] S. Nakata et al.,"Increasing Static Noise Margin of Single-bit-line SRAM Lowering Bit-line Voltage during Reading".IEEE 54th International Midwest Symposium on Circuits and Systems 2011.pp.1-4,7 Aug,2011.

[5] PM Vansi Kiran et al.,"Design and Analysis of Different types SRAM Cell Topologies" ICECS.pp.167-173,26-27Feb,2015.

[6] Paridhi Athe et al. .,"A Comparative Study of 6T,8T and 9T Decanano SRAm Cell" ISIEA.pp.889-894,4oct,2009.

[7] M. Alioto, "Understanding DC behavior of sub-threshold CMOS logic through closed-form analysis," IEEE Transactions on Circuits and Systems I. vol. 57, no. 7, pp. 1597-1607, 2010.

[8] S. Tavva et al. "Variation Tolerant 9T SRAM Cell Design" GLSVLSI'10,pp.55-60,may 16, 2010.

[9] Spector, A. Z. 1989. Achieving application requirements. In Distributed Systems, S. Mullender

[10] 1 Hooman Farkhania, Ali Peiravia and Farshad Moradib, " A new asymmetric 6T SRAM cell with a write assist technique in 65 nm CMOS technology" Proc. Of Microelectronics journal, pp. 1556-1565, 2014.

[11] M.kavitha et.al., "Low power multimodal switch for leakage reduction and stability improvement in SRAM cell", Arabian journal for science and engineering,vol,41,no.8,p.p 2945-2955,12Feb,2016.

[12] Wang, J.; Nalam, S.: Analyzing static and dynamic write margin for nanometer SRAMs. In: Proceedings of the ACM/IEEE International Symposium on LPED, pp. 129–134 (2008).

[13] Expanding margins for writing," in Proc. [SSCC Dig., pp. 480-481, Feb. 2005.

[14] R. Heald et al., "Variability in sub-100 nm SRAM designs," in Proc. IEEE/ACM ICCAD, Nov. 2004, pp. 347–352.