# Full Adder Circuits using Static Cmos Logic Style: A Review

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## ABSTRACT
This paper presents 1-bit CMOS full adder cell using standard static CMOS logic style. The comparison is taken out using several parameters like number of transistors, delay, power dissipation and power delay product (PDP). The circuits are designed at transistor level using 180 nm and 90nm CMOS technology. Various full adders are presented in this paper like Conventional CMOS (C-CMOS), Complementary pass transistor logic FA (CPL), Double pass transistor logic FA , Transmission gate FA (TGA), Transmission function FA, New 14T,10T, Hybrid CMOS, HPSC, 24T, LPFA (CPL), LPHS, Hybrid Full Adders.

## Keywords
PDP, CMOS full adder, power dissipation, low power, Delay etc.

## 1. INTRODUCTION
Full Adder Cell plays a very important role in Digital Signal Processors , Application Specific ICs or Digital Processors etc. By Enhancing the performance of 1-bit full adder have great effects on enhancing the performance of the overall system.

Among all arithmetic operation the addition is a basic one and acts as the origin of other operations like subtraction, multiplication, division, address generating and so on. The most important feature of modern electronics is low power and energy efficient active block that enables the implementation of long lasting battery operated devices [1]. For different type applications, various types of logic styles are used for designing a full adder cell [2]. For performance analysis of different-2 full adders different parameters are calculates like average power dissipation, delay, number of transistors in used and PDP of circuit. In a design it is optimised desired that the circuit dissipate less power, have very less delay, low supply voltage and avoid degradation in output voltage [3].Power and delay depends on size and number of transistors, parasitic capacitance and capacitance due to inter cell and intra cell routing [4]. Power dissipation depends on switching activity Dynamic power contributes the overall power dissipated in CMOS circuits so it is necessary to study dynamic power more profoundly. Dynamic power ($P_D$) is explained in equation (1)&(2) .

$$P_{avg} = P_{static} + P_{dynamic} + P_{short\text{-}circuit} \quad (1)$$

$$P_{dynamic} = C_{TOTAL} \times V^2_{CC} \times f \quad (2)$$

Power dissipation (Pavg) and dealy (τ) is very important parameters for low power operations but there is trade-off between this parameters [3].

Reducing the number of transistors may lead to reduced power but sometime does not improve. All above stated parameters of full adder vary from one logic to other logic [5]. This paper represents the comparison between various full adders at 180nm and 90nm CMOS technology. The CMOS logic circuits are defined into two categories: - static and dynamic logic circuits. These different logic styles are used according to design necessities such as power consumption, speed and area. So, in static logic circuit, at every point the output will be connected to either $V_{DD}$ or Ground through a path having low resistance [4]. The static logic alienates pre charging and decreases extra power dissipation [3][4][5]. The organization of this paper is as follows: Section I is having basic introduction, Section II presenting logics for full adder, Section III presenting different 1-bit full adders. In Section IV comparison table of delay, average power and PDP are given. Finally in Section V conclusion of is present.

## 2. STATIC LOGIC BASED FULL ADDER CELLS
Adder is a circuit in order to operate for a given three one bit inputs A, B, C and two one bit outputs sum and carry.

$$SUM = A \oplus B \oplus C \quad (3)$$

$$SUM = \bar{C} \cdot (A \oplus B) + C.\overline{(A \oplus B)} \quad (4)$$

$$COUT = A.B + C\,(A \oplus B) \quad (5)$$

$$= C.(A \oplus B) + A.\overline{(A \oplus B)} \quad (6)$$

## 3. REVIEW OF VARIOUS STYLES OF FULL ADDER CELLS
There are different kinds of CMOS full adder. This section reviewed the various states 1-bit full adders. Various types of the full adder designs are:

### 3.1 Conventional CMOS Full Adder
The regular structure of Conventional CMOS full adder cell includes 28 no. of transistors which can be either pull up or pull down structure. It consists pairs of complementary transistors which provides high stability, high noise margins and layout regularity at low voltage and also make the straight forward circuit layout. It has less number of interconnecting wires[7], strength against voltage scaling and sizing of transistor [8] and drawback is that SUM realizes on COUT signal which generates undesired additional delays. It dissipates more power and takes larger area and also have weak output driving capability [4].

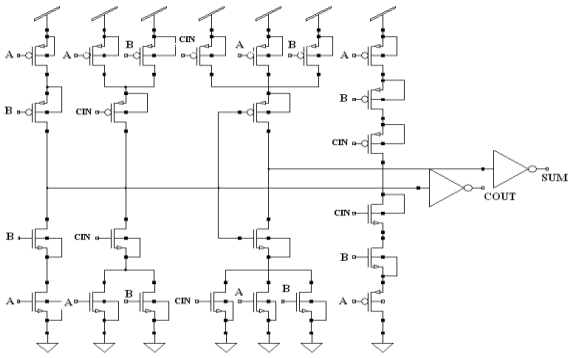



**Fig.1 Conventional CMOS full adder schematic**

## 3.2 Complementary Pass Transistor Logic Full Adder

The general structure of Complementary Pass Transistor Logic **(**CPL) full adder cell includes 32 transistors which is based on logic style of multiplexer so it requires all input in invert form also. In this to drive other circuits it required each signal carried by two wires one true values and other invert form [6].It gives complementary in-out values. The advantage of this is that is faster than CCMOS but drawbacks is that it has high delay, wiring complexity and also not applicable for low power application [4].The CPL full adder with swing restoration shown in Fig. 2 [9]&[10].

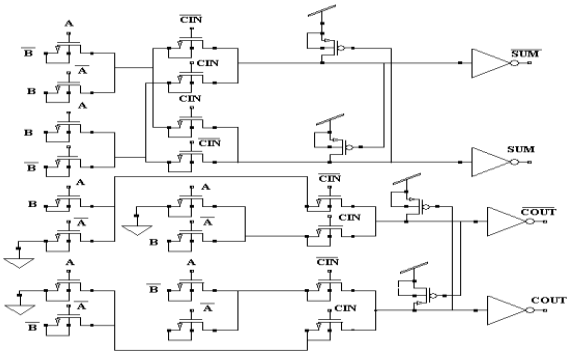



**Fig.2 Complementary Pass Transistor Logic adder schematic**

## 3.3 TFA Full Adder

The simpler schematic of transmission full adder (TFA) with driving ability is shown in Fig. 3. It consists less transistor comparing with earlier explained full adder. The transistor used in TFA is 26T. The drawbacks are that it has high delayas well as high power consumption [10]. In this circuit there are two feasible short circuit paths to ground. CPL style is used to derive the load pull-up and pull-down. It consumes less area and power as well [2].

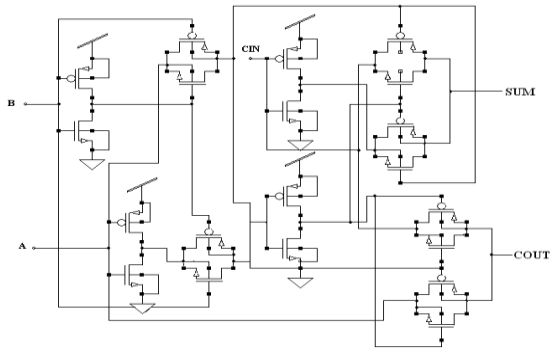



**Fig.3 Transmission full adder schematic**

## 3.4 10T Full Adder

The 10-Transistors full adder as shown in Fig. 7 uses hybrid logic style [10]. It is not full swing though it requires fewer transistors. This full adder suffers from the deficiency of driving capabilities and the performance of it diminishes dramatically when they are connected in series. This full adder generates Exclusive-or of A and B signal used as a select signal to get the desired outputs. It must be notified that when supply voltage is below 1.8V this adder cannot work efficiently [11].

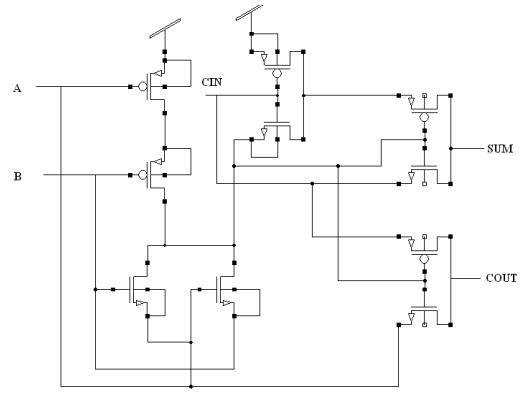



**Fig.4 10T Full adder schematic**

## 3.5 HPSC Full Adder

In given presented paper, a new low power full adder which is capable of operating at 0.5V. A structural two stage design having full-swing enhanced pass logic front stage driving a low load output stage is adopted. Though circuit has higher number of transistors, The proposed circuit has outperformed in terms of power delay product while comparing to various circuits which are executed with similar conditions [12].

## 3.6 TGA Full Adder

A transmission gate adder (TGA) based on CMOS is shown in fig 4.A transmission gate logic is a connection of PMOS and NMOS transistor in parallel formal.This parallel connection is controlled by a complementary control signals. It is a special type of pass transistor[13].

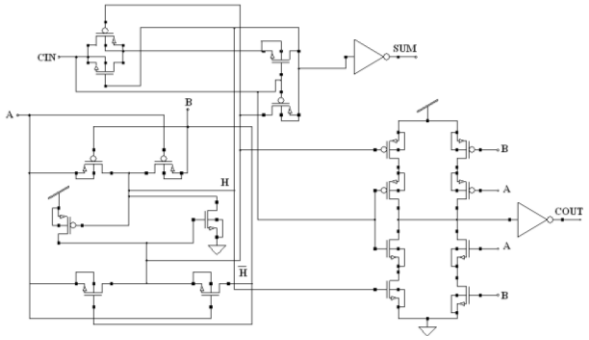



**Fig.5 HPSC Full adder schematic**

In TGA both input logic "0" or "1" pass through path provided by NMOS and PMOS, hence no problem of voltage drop is there. The TGA has a drawback of having double transistor compared to standard pass transistor [14]&[15].

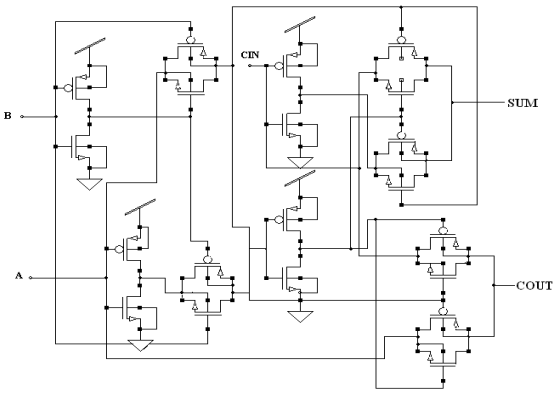



**Fig.6 Transmission gate adder schematic**

## 3.7 14T Full Adder

As the name indicates it consists 14 transistors. It is also called as hybrid full adder because it uses more than one logic style [2]. It uses a XOR/XNOR circuit. Although the transistor count is very low but still it has low driving capability and noise immunity [3]. This circuit includes recently proposed XOR (6-transistors) to produce both an XOR as well as XNOR function[3]. This proposed circuit was compared to another PTL full adder with a low transistor count to check the performance. As the results the respective propagation delays were also similar for both adders. [14]

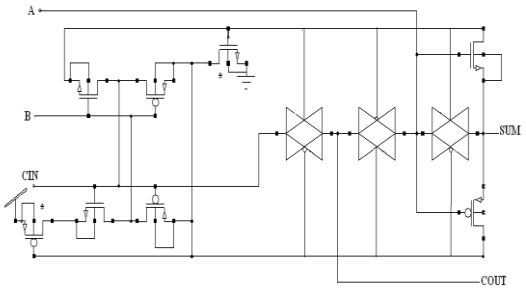



**Fig.7 14T Full adder schematic**

## 3.8 Hybrid CMOS

Hybrid-CMOS design style presents very accurate idea to the select various modules in a circuit according to the application. A new outstanding Hybrid-CMOS design style is represented having objective to achieve low Power and delay. This hybrid CMOS full adder has ultimate performance than existing full adders. It performs very well with scaling of $V_{DD}$ (input voltage) with different conditions and for all high-performance circuits design. The advantages of this adder is that it has good noise immunity and applicable for sub micrometer applications static [3].

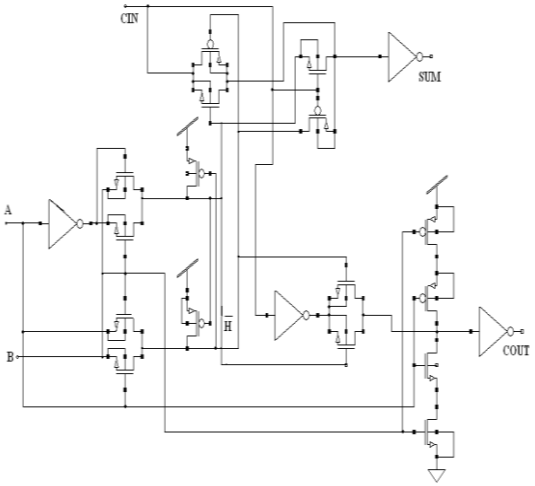



**Fig.8 Hybrid Full Adder schematic**

## 3.9 24T Full Adder

A novel 24T Full Adder is shown in Fig. 9.After comparing the characteristics (power consumption, delay time and the power-delay product) with different previous designs, the compared results shows that 24T design is extraordinary to other designs. After simulation, a prominent improvement of the circuit than previous literature is 1.8% to 36% in power dissipation, 11.7% to 41.2% in delay time of Cout, and 13.7% to 92% in PDP of Cout [10].

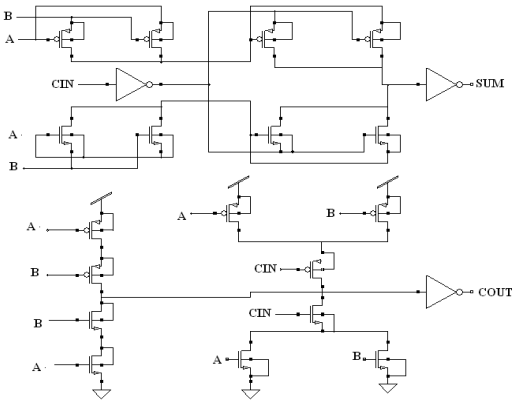



**Fig.9 24T Full Adder schematic**

## 3.10 GDI Based Full Adder

A Gate diffusion input (GDI) technique is implemented to design a low power as well as high speed full adder cell. Fig.11 shows the new adder simulated in GDI technique [3]. GDI cell has 3 inputs- G, P and N where G stands for input of NMOS and PMOS, P stands for input to the source /drain of PMOS and N for input to the source/drain of NMOS. A total of 24 transistors are used in GDI based full adder cell. In GDI based full adder there are 2 prime stages. XOR and XNOR logics are produced by first stage of GDI. This stage gives full swing with low voltage and complementary outputs with respect to other is deliver to second stage [17].

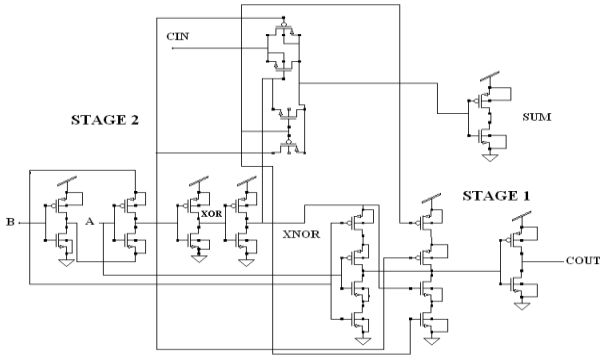
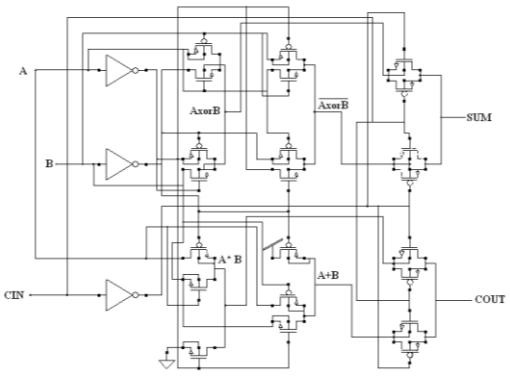



**Fig.10 GDI Based Full adder schematic**

## 3.11 LPFA Full Adder

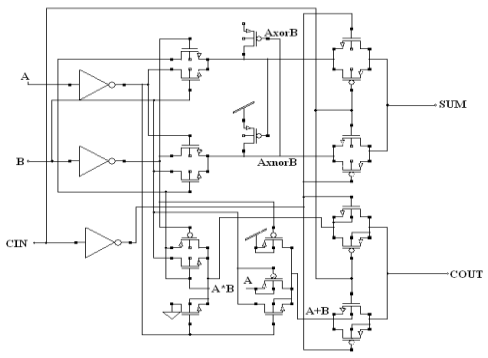
LPFA (low power full adder) is shown in Fig. 11(a) & 11(B) To exhibits its benefits, two full-adders were made with combination of pass-transistor either by powerless or groundless logic styles. H-spice simulations showed speed improvements up to 25%, power savings up to 80% and 85% for the power-delay product. The consumes very less area which is only 40% area of the largest full-adder at supply voltage of 0.6v, since both realizations designed using this scheme (a) and (b) exhibit the smallest propagation delay. On the Base of the results calculated in [1], two new design of full-adders using the logic styles double pass-transistor (DPL) and swing restored (SR-CPL) structure represented in Fig.11(a) and Fig.11 (b).




(a)

## 3.12 Hybrid A Full Adder

Hybrid A full adder cell includes of 12 transistors as shown in Fig. 12[6]. In the paper [18] Hybrid A full




(b)

**Fig.11 Low Power Full-adder (a) DPL & (b) SR-CPL logic style**

adder is simulated at 90nm technology with at 27°c temperature. Power is obtained by changing the value of aspect ratio and also operating supply voltages $V_{DD}$. The advantages of Hybrid A full adder circuits is that it provides good driving capability of output and better power delay performance at 0.6.

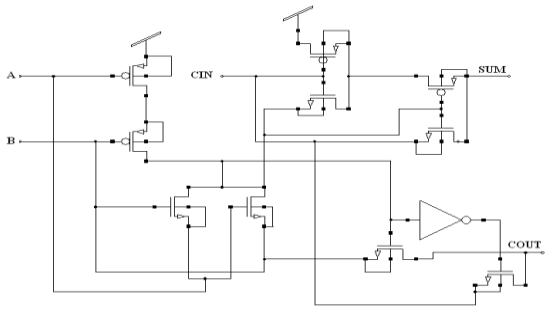



**Fig.12 Hybrid-A full adder schematic**

## 3.13 Hybrid B Full Adder

Hybrid B full adder is designed using low power XOR and XNOR for implementation of sum and carry. Hybrid B full adder includes 16 transistors as shown in Fig 14 [6]. It is similar to the Hybrid A FA but the difference is it includes two transistor more. It consumes less power and delay [18].

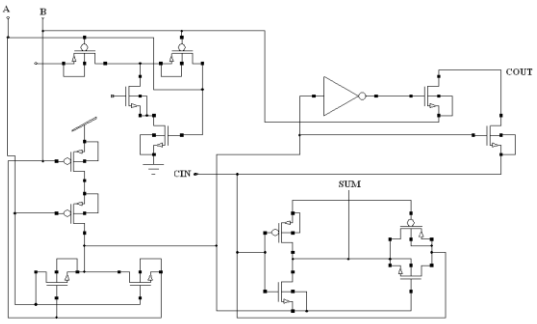



**Fig.13 Hybrid B full adder schematic**

## 3.14 LPHS Full Adder

A LPHS (low-power, high-speed) full adder , consists 15T, is presented as a classy method to decrease complexity and enhance the performance of the circuit. It includes very less transistor 60-75% less compare to others. The LPHS-FA is establish to provide a 20.5–21.3% power saving, a 12.2–67% delay time reduction and a 35–102% reduction in power delay product compared with the others FAs. An LPHS-FA is represented in this phase as a way to modify the circuit architecture and hence improve the performance. In contrast to other types an LPHS-FA is excellent among all types and can be suitable in many practical applications [19].

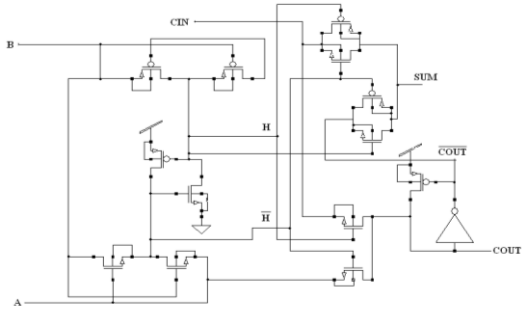



**Fig.14 LPHS full adder schematic**

## 3.15 Hybrid C Full Adder

In a hybrid 1-bit full adder designs both CMOS logic and transmission gate logic is publicized. Firstly the circuit design was executed for 1 bit on Cadence Virtuoso tool is used to implement this circuit. For 180nm (90nm) technology, the average power consumption is 4.1563µW (1.0176µW), was found low delay is 224ps (91.3ps)at 1.8V(1.2V) respectively. For 32 bit it was found to be working proficiently with only 5.578ns (2.45ns) delay and 112.79µW (53.36µW) power at 180nm (90nm) technology for 1.8V (1.2V) input voltage.while comparing with the existed full adder circuits, the present implementation was establish to offer prominent improvement in view of speed and power consumption [20].

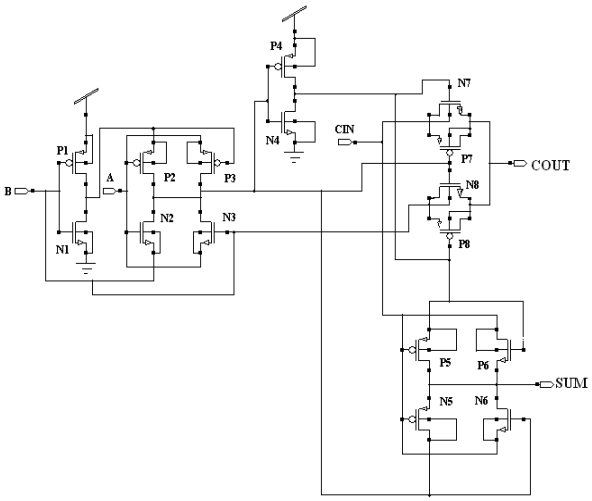



**Fig.15 Hybrid-C full adder schematic**

# 4. COMPARISON OF SIMULATIONS OF VARIOUS ADDERS

Simulation results of various full adders has been depicts in Table 1 and Table 2 at 180nm and 90nm corresponding.

**Table 1 Simulation Results for Full Adders in 180nm**

| Design | Delay (ps) | Power consumption (µw) | PDP (fj) | TC |
|---|---|---|---|---|
| CCMOS | 292.1 | 6.2199 | 1.8168 | 28 |
| CPL | 183.97 | 7.7198 | 1.4202 | 32 |
| TFA | 287.1 | 802491 | 2.368 | 16 |
| 10T | 132.59 | 14.345 | 1.902 | 10 |
| HPSC | 273.7 | 6.3798 | 1.746 | 22 |
| TGA | 293.9 | 8.4719 | 2.899 | 20 |
| 14T | 381.7 | 12.7252 | 4.856 | 14 |
| Hybrid CMOS | 252.3 | 5.978 | 1.508 | 24 |
| 24T | 314.2 | 15.91 | 4.998 | 24 |
| GDI _FA | $50\times10^{3}$ | 0.780 | 39.0 | 24 |
| LPFA_DPL | 226.6 | 19.56 | 4.432 | 22 |
| LPFA_SR-CPL | 220.65 | 20.78 | 4.585 | 20 |
| LPHS | 179.5 | 5.736 | 1.026 | 15 |
| Hybrid C | 224 | 4.1563 | 0.931 | 16 |

# 5. CONCLUSION

The performance characteristics of various full adders given in Table-1 and Table-2 corresponding to 180nm and 90nm .Tables shows that various adders have various parameter values, no single adder have less delay, power and Power-Delay product. According to this, there is a trade off between these all parameters. On the basis of results we can select adder according to a specific application.

**Table 2 Simulation results for fulladders in 90nm**

| Design | Input Voltage (v) | Delay (ps) | APC (µw) | PDP (fJ) | TC |
|---|---|---|---|---|---|
| CCMOS | 1.2 | 0.1269 | 1.5799 | 0.2005 | 28 |
| CPL | 1.2 | 0.0791 | 1.7598 | 0.1392 | 32 |
| TFA | 1.2 | 0.3198 | 1.7363 | 0.5552 | 16 |
| HPSC | 1.2 | 0.2207 | 1.56 | 0.3443 | 22 |
| TGA | 1.2 | 0.2317 | 1.7619 | 0.4082 | 20 |
| 14T | 1.2 | 0.3389 | 3.3297 | 1.1284 | 14 |
| Hybrid CMOS | 1.2 | 0.1430 | 6.21 | 0.8888 | 24 |
| 24T | 1.2 | 0.1406 | 7.707 | 1.0836 | 24 |
| LPFA DPL | 1.2 | 0.254 | 7.34 | 1.864 | 22 |
| LPFA SR-CPL | 1.2 | 0.167 | 7.4 | 1.235 | 20 |
| Hybrid A | 1 | 0.06 | 1.61 | $0.59\times10^{-3}$ | 12 |
| Hybrid B | 1 | 0.37 | 0.67 | $4.02\times10^{-3}$ | 16 |
| Hybrid C | 1.2 | 0.0913 | 1.1764 | 0.1074 | 16 |

Where: APC=Average power consumption,TC=transistor count

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