Comparative Study of Technology in Semiconductor Memories-A Review

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ABSTRACT
In this paper we will present a review on the development of semiconductor Memories through the most recent decade. Starting demands of low power devices is extending therefore; this is the reason for scaling of CMOS advancement. In view of the scaling, size of the chip diminishments and number of transistor in structure on chip increases. Generally the amount of transistors utilized as a piece of chip to store data so, in future the need of low power memories is growing. The extended enthusiasm for mobile phones has incited amazing examination attempts in the setup and progression of low power circuits. Memories are the critical section in present day for automated systems, for instance, chip and Digital Signal Processors (DSPs) that are utilized as a piece of mobile phones. This paper will give a comparison of SRAM memories cell on the basis of their architecture.

Keywords
SRAM cell; low power; noise margin; leakage current

1. INTRODUCTION
Semiconductor memory development is a key part of today's equipment. Frequently based around semiconductor advancement, memory is utilized as a part of any equipment that utilizes a processor of some structure. With the fast improvement in the need for semiconductor memories there have been different progressions and sorts of memory that have risen. Names, for instance, ROM, RAM, EPROM, EEPROM, Flash memory, DRAM, SRAM, SDRAM, and the new MRAM can now be found in the equipment composing. Each one has its own specific great circumstances and reach in which it may be utilized. Since 1965, it is the Moore's law, scaling the innovation and in results, the execution of VLSI composition is come to at the level of the five sequence of extent in the most recent four decades [1]. Moore's law, expresses that the doubling of the quantity of transistors per era on an integrated circuit almost every 2 years (normally 18–24 months) [2]. Nowadays, The semiconductor industry, is so far endeavoring to facilitate the speed of scaling the development as demonstrated by the Moore's Law, and it is a direct result of shrieked transistors and by the overcoming the control of innovation scaling.VLSI innovation has tremendous in recent years and scaling of chip in VLSI innovation diminishes quickly whose outcome is that multifaceted nature and thickness of chip has expanded. So the low power devices are the main decision of VLSI originators and these low power devices satisfy the objective of the frameworks.

The enthusiasm of battery worked quick helpful devices like diary, advanced mobile phones, mechanized associates, PDAs; etc.Quick conservative devices require crucial memory that responds speedier. Therefore, static random access memory (SRAM) is utilized, which is speedier. Dynamic power scattering and leakage current are the essential issues of quick SRAM cells since this undesirable power leakage diminishes the battery life of adaptable devices. So it is required to have a SRAM cell arrangement, having both low static and component power leakage. Supply voltage is scaled to keep up the power utilize within most distant point. Nevertheless, scaling of supply voltage is confined by the prevalent need. Accordingly, the scaling of supply voltage just may not be satisfactory to keep up the power thickness within purpose of repression, which is required for power fragile applications. Circuit methodologies and structure level strategies are moreover required close by supply voltage scaling to fulfill low power plot. So, in this paper we will analyze the multiple semiconductor memories and see the comparison between volatile and non volatile memories. Furthermore, we will focus on architecture of SRAM bit cell (4T, 5T, 6T).

2. MEMORIES OVERVIEW
2.1 Existance of Semiconconductor Memories
In this section we will discuss the existence of memories. On the study of the different search paper we got the memory reviews. The primary type of RAM came to utilize in 1947 with the utilization of the Williams tube. It utilized a cathode beam tube (CRT) and information was keep on the face of the CRT as electrically charged spots.

The second broadly utilized type of RAM was magnetic-core memory, discovered in 1947. Frederick Viehe is credited with a significant part of the work, having filed for several patents relating to the design magnetic-core memory works using minor metal rings and wires associating with every ring. One piece of information could be put away per ring and access at any time.

Semiconductor memory also has much faster get to times than various sorts of data collection; a byte of data can be created to or read from semiconductor memory within several nanoseconds, while access time for turning collection. In this manner it is utilized for principle PC memory.

2.2 Classification of semiconconductor memories
Electronic semiconductor memory development can be part into two arrangements, according to the course in which the memory works:

1. ROM(Read only memory)
2. RAM(Random access memory)

2.3 Read Only Memory
Basically ROM is non volatile memory which shows that the information stored in it, is not lost even if the power supply goes off. It's utilized for the permanent storage of information. It also posses random access property. Information cannot be written

into a ROM by the programmers. Read only memory (ROM) is class of capacity medium utilized as a part of PCs and other electronic devices [13].Information put away in ROM must be adjusted gradually, with trouble, or not in the slightest degree, so it is principally utilized to appropriate firmware.

a) Classifications of ROM

1. PROM (Programmable read only memory).
2. EPROM (Erasable programmable read only memory).
3. EEPROM (Electrically erasable programmable read only memory).

1. PROM

It is one-time programmable non-volatile memory is a type of digital memory where the setting of every bit is bolted by a circuit. They are a kind of ROM (read-only memory) which means the information in them is lasting and can't be changed. PROMs are utilized as a part of digital electronic devices to store perpetual information, normally low level programs, for example, firmware [14].The key disparity from a standard ROM is that the information is built into a ROM amid manufacture, while with a PROM the information is customized into them after manufacture. Along these lines, ROMs have a tendency to be utilized just for vast generation keeps running with very much checked information, while PROMs are utilized to permit organizations to test on a subset of the devices in a request before burning information into every one of them.

2. EPROM

An EPROM or erasable programmable read-only memory is a sort of memory chip that holds its information when its power supply is exchanged off thus, it is non-volatile. It is an array of floating-gate transistors independently customized by an electronic device that supplies higher voltages than those regularly utilized as a part of digital circuits. Once programmed, an EPROM can be erased by presenting it to highly ultraviolet light source, (for example, from a mercury-vapor light). EPROMs are effortlessly recognizable by the straightforward quartz window in the highest point of the package, through which the silicon chip is noticeable, and which allows presentation to ultraviolet light light amid eradicating.

Every capacity area of an EPROM comprises of a single field-effect transistor. Every field-effect transistor comprises of a channel in the semiconductor body of the device. Source and drain contacts are made to districts toward the end of the channel [14]. A protecting layer of oxide is become over the channel, then a conductive (silicon or aluminum) gate terminal is deposited, and a further thick layer of oxide is put over the gate terminal. The drifting gate terminal has no associations with different parts of the integrated circuit and is totally protected by the encompassing layers of oxide. A control gate terminal is deposited and further oxide covers it.

3. EEPROM

EEPROM (also written E2PROM and pronounced "e-e-prom", "double-e prom", "e-squared", or simply "e-prom") stands for Electrically Erasable Programmable Read-Only Memory and is a kind of non-volatile memory utilized in computers and other electronic devices to keep small amounts of information that must be saved when power is removed. Unlike bytes in most other types of non-volatile memory, individual bytes in a traditional EEPROM can be independently read, erased, and re-written. When larger amounts of static data are to be stored (such as in USB flash drives) a specific kind of EEPROM such as flash memory is more economical than traditional EEPROM devices. EEPROMs are organized as arrays of floating-gate transistors.

An EPROM normally should be expelled from the device for deleting and programming, while EEPROMs can be modified and eradicated in-circuit, by applying extraordinary programming signals. Initially, EEPROMs were constrained to single byte operations which made them slower; however modern EEPROMs permit multi-byte page operations [14]. It additionally has a restricted life - that is, the quantity of times it could be reprogrammed was constrained to tens or a huge number of times. That constraint has been stretched out to a million compose operations in modern EEPROMs. In an EEPROM that is frequently reprogrammed while the PC is being utilized, the life of the EEPROM can be an important design consideration. It is consequently that EEPROMs were utilized for configuration information, instead of random access memory.

2.4 Random Access Memory

The RAM is a volatile memory, when the power is off, it cannot be accessed. So this mean RAM PC memory basically empty.RAM holds information and handling instructions incidentally until the CPU needs it.RAM is the place in a PC where the working framework, application program, and information are kept with the goal that they can be immediately come to by the PC's processor. RAM is much quicker to read and write. RAM loses its information, when you turn your PC. RAM is called “random access “since it utilizes any storage area can be accessed directly.

b) Classification of Random access memory

1. SRAM (Static Random Access Memory).
2. DRAM (Dynamic Random Access Memory).
3. MRAM

1. SRAM

Static random-access memory (SRAM or static RAM) is a sort of semiconductor memory that utilizes bistable latching hardware (flip-flop) to store every piece of information. It is still unpredictable in the ordinary sense that information is in the end lost when the memory is not powered. The first reasonable type of random-access memory was the Williams tube beginning in 1947. It put away information as electrically charged spots on the substance of a cathode beam tube. Since the electron light of the CRT could read and write the spots on the tube in any order. The limit of the Williams tube was a couple of hundred to around a thousand bits, however it was much littler, speedier, and more power-productive than utilizing singular vacuum tube latches[13].In basic SRAM, a bit of information is put away utilizing the condition of a four transistor memory cell. This type of RAM is more costly to create, but, it is quicker and requires less power than DRAM and, in present day PCs, is frequently utilized as reserve memory for the CPU. DRAM stores a piece of information utilizing a transistor and capacitor pair, which together contains a DRAM memory cell. The capacitor holds a high or low charge (1 or 0, separately).In other hand, we can say that static memory circuits store a logic values utilizing two consecutive inverters. Static memory devices don't should be refreshed, and they can work much quicker than dynamic circuits. But, since they require far greater chip area than dynamic memory cells, they are utilized just where they are most required in speed.

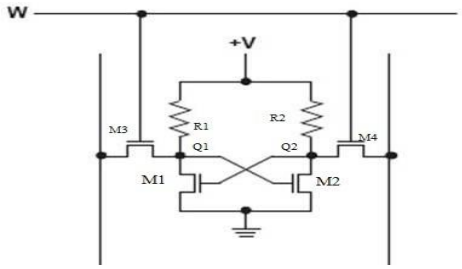

Fig 1. SRAM cell [13]

a. Operation:

There are the four basic operation is performed by the basic cell (4T) of the SRAM. The following operation is as:

1. Read 0
2. Read 1
3. Write 0
4. W*rite 1*

a. Precharge: we are having with three lines. So firstly precharge these line as shown below.

Table I. Precharge Voltage

S.No.	Operation	Bit Line	Bit line bar	Word Line
1	Read 0	5v	5v	5v
2	Read 1	5 V	5v	5v
3	Write 0	0v	5v	5v
4	Write 1	5v	0v	5v

b. Transistor status:On the basis of lines we can determine the transistor state.

Table II. Transistor status on different Operation

Operation	M10	M2	M3	M4
Read 0	On	Off	On	Off
Read 1	Off	On	Off	On
Write 0	Off	On	On	on
Write 1	On	Off	On	On

2. DRAM

Dynamic random-access memory (DRAM) is a kind of memory that stores each piece of information in a capacitor within integrated circuit. So, the capacitor can be either charged or released; these two states are taken to represent the two value set of a bit, ordinarily called 0 and 1. Since even "non conducting" transistors always release a small amount, the capacitors will gradually released, and the information eventually fades unless the capacitor charge is refreshed periodically. Hence refresh circuitry is use so that requirement it is a dynamic memory [13].

It is the RAM in desktops, minimal PCs and workstation PCs furthermore a parcel of the RAM of videogames consoles. Interestingly, SRAM, which is speedier and more expensive than DRAM, is frequently used for CPU stores.

The primary memory (the "RAM") in PCs is dynamic RAM (DRAM). It is the RAM in desktops, portable PCs and workstation PCs and in addition a portion of the RAM of videogames consoles. Interestingly, SRAM, which is speedier and more costly than DRAM, is regularly utilized for CPU caches.

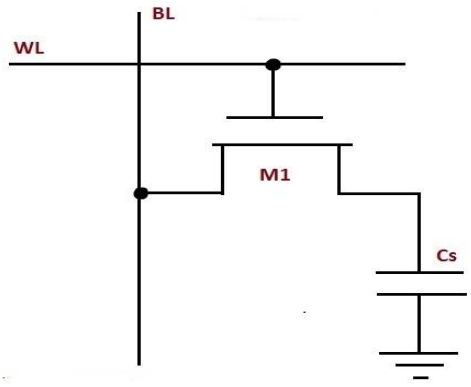

Fig 2. 1T DRAM CELL [14]

3. MRAM (Magneto resistive Random Access Memory)

MRAM stand for Magneto resistive Random Access Memory. It stores information utilizing attractive charges rather than electrical charges. MRAM utilizes far less power than other RAM innovations so it is perfect for versatile devices. It likewise has more prominent stockpiling limit. It has speedier access time than RAM. It holds its substance when the force is expelled from PC.

2.5 Comparison between RAM and ROM

Table III. Difference between RAM and ROM

S. No.	Features	RAM	ROM
1.	Stand for	Random access memory	Read only memory
2.	Volatility	Volatile Its contents are lost when the device is powered off.	Non-volatile Its contents are retained even when the device is powered off.
3.	Types	1. SRAM 2. RAM	1. PROM 2. EPROM 3. EEPROM.
4.	Operation	Allows reading and writing.	Allows reading.
5.	Cost	Expensive	Cheap

2.6 Comparison Between SRAM And DRAM

Table IV. Difference between SRAM and DRAM

S. No.	Features	SRAM	DRAM
1.	Type	Static	Dynamic
2	Speed	Fast	Slow
3	Power Consumption	Less	High
4	Cost	Expensive	Cheap

5	Operation	No Refreshment after read operation	Refreshed after each read operation.
6	Utilize	Cache memory	Main memory

3. SURVEYED DESIGNS

On the bases of the literature survey we analyze the SRAM with help of their various cell transistors and topologies .The initially MOSFET based memory showed up in seventies. In 1968 [3], Robert Dennard illuminated the thought of component memory cell with a singular MOSFET and a capacitor at IBM and progressively, MOSFET based component dynamic random access memory (DRAM) chip with 2k-bits showed up with controlled leakage current in 1971. Regardless, execution of DRAM has not facilitated the pace with the execution of the processors because of long get to time and because of necessity of more power and there is moreover essential to resuscitate sometimes for utilize data without lose in memory cells [4, 5]. Despite the fact that, SRAMs overwhelm in execution yet SRAMs of high limit can't be installed, because of range impediment on chip and the high cost per bit. Most recent patterns demonstrates that the rate of inserted SRAM in System-on-Chip (SoC) items will increment encourage from the current 84% to as high as 94% by the year 2014 [6]. In addition, there is a eminent interest of reserve memory in present day PC frameworks as microchips outline has been moved to multi-center designs and the offer of SRAM on a chip has radically expanded from 20% in 1999 to 94% in 2014[1]

3.1 Architecture Of SRAM Bit Cell

1. 4T load less SRAM Cell

Figure 3 demonstrates the load less 4T SRAM which utilizes NMOS transistors as get to transistors [15]. In this design bit lines are pre-charged to ground (0 Volts) rather than VDD (1.2 volts). The two PMOS transistors appeared in Figure are utilized as drivers for the cell. The cell works with great stability. It is a promising possibility for speed and high-thickness SRAMs inserted in any logic devices, and additionally for standalone SRAM applications [15].

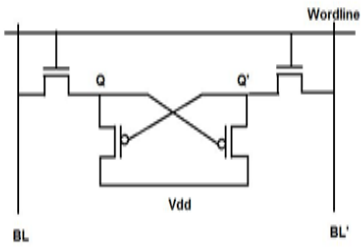

Fig 3. Schematic of 4T Load less SRAM [15]

2. 5T SRAM Bit cell Topology

It is a high thickness low leakage current five transistor (5T) SRAM bit cell as appeared in figure [7] which has only one bit line to perform read and write operations through a single pass gate device M1.Writing into 5T bit cell enables by interfacing the bit line to V_{DD} or V_{SS} respectively, when the word line is high or associated with $V_{DD.}$

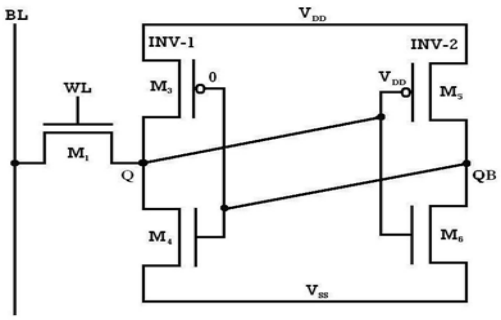

Fig 4. 5T SRAM Bit Cell [7]

But correct sizing of the transistors is required to assure suitable WAM and read- SNM. However, these designs takes 15-21% less area for various procedures, lower bit line leakage to 75%, and has a comparable read/ write performance to standard 6T bit cell but it has weak static noise margin and need a on-chip DC-DC to generate a Pre-charge voltage of bit line. Thus, In 5T SRAM bit cell read operation needs a pre-charge voltage where $V_{SS} < V_{PC} < V_{DD}$. But in the standard 6T SRAM pre-charged at V_{DD} before a read and write operation. Subsequently, a conceivable bit line pre-charge voltage V_{PC} grade for 5T SRAM bit is watched 340–860mV for worst scenario. A V_{PC} of 600mV has been accounted for as the bit line pre-charge voltage level for a 0.18 μm CMOS Technology [1].

3. 6T SRAM cell

The 6T SRAM setup often known as the CMOS standard SRAM cell has the attractive properties of low power dissipation, high exchanging speed, and great noise margin. The cross coupled latch framed by transistor M1 and M3 shapes the center of the SRAM cell. This transistor pair can be in one of the two stable states. These two stable states form the 1-bit data that one can store in this transistor pair.

Conventional 6T SRAM bit cell structure as shown in figure, is the generally utilized bit cell for cache memory in high microchips. There are a few topologies have been produced with the point of various goals like least bit cell area, low static and dynamic power dissipation, sublime execution and better parametric results in terms of Static-Noise-Margin (SNM) and Write-Ability-Margin (WAM).

Different strategies like boosting the supply voltage, read and write assist hardware in SRAMs have additionally been proposed to accomplish more steady information maintenance amid read operations [8, 9]. The principle concern in SRAM bit cell design is a trade off among these design measurements. For instance, in sub-threshold SRAMs, noise margin is the key design parameter and not speed [10, 11]. So ,on the premise of these bit cell topologies are comprehensively partitioned into two classifications:

- Non-isolated read port SRAM bit cell topologies (less robust),
- Isolated read-port SRAM bit cell topologies (highly robust).

Kim TH, Liu J, Keane J, Kim CH. 2008 proposes 6T Figure 5 demonstrates the circuit outlines of a conventional SRAM cell [16]. Before to the read operation starts, the bit line (BL) and bit bar line (BLB) are precharged to as high as supply voltage Vdd. At the point when the word line (WL) is chosen, the access transistors are turned on.

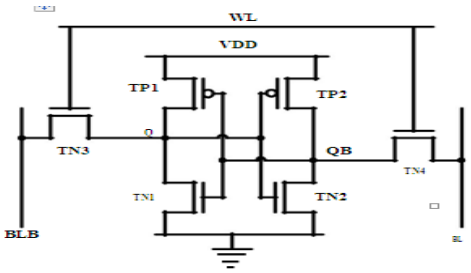

Fig 5. 6T SRAM Bit Cell [16]

This will bring about a current to flow from supply voltage through the pull up transistor M2 of the node putting away "1". On the other side, current will flow out of the precharged bit bar line to ground, accordingly releasing bit bar line. In this manner, a differential voltage creates between the BL and BL. This little potential difference between the bit lines is detected and amplified by the sense amplifiers at the data output. [16].

Static Random Access Memory (SRAM) is an imperative memory device which stores information on a chip. SRAM acts as a Cache memory furnishing an immediate interface with the CPU at a speed which can never be achieved by DRAMs. The applet on this page shows the run of the mill six-transistor cell utilized for CMOS static arbitrary get to recollections (SRAM). The cell comprises of two cross-coupled CMOS inverters that store one bit of data, and two N-type transistors that associate the cell to the bit lines. To read the data, the word line is activated while the outer bit line drivers are switched off. Thus, the inverters inside the SRAM cell drive the bit lines, whose value can be read out by outer logic. To write new information into the cell, the tristate drivers are activated to drive the bit lines. Next, the word line transistors are enabled. Since the outer drivers are much greater than the little transistors utilized as a part of the 6T SRAM cell, they effortlessly override the past condition of the cross-coupled inverters.

4. CONCLUSION

In this paper we have analyzed the semiconductor memories with low power SRAM cell. A broad overview has been done for different design of Static Random Access Memory. These designs are all around favored for different low power applications. Different methods to lessen the power dissipation have been created and it can be utilized for low power and fast applications.

The most conventional way to reduce the power dissipation is the reduction of the supply voltage, reduce the size of MOS and insert tail transistor in SRAM cell. The power dissipation reduction in SRAM depends on supply voltage. Recently, silicon technology scaling demands a decrease in both Vdd and Vth to sustain delay reduction.

So, we analyzed and compared the SNM, power dissipation, area, read and write operation of three different SRAM cell topologies. It is oberserved that low power and high speed SRAM cell required for SRAM array. Hence the performance of SRAM can be improved further dynamic supply voltage scaling, which improves speed and power consumption. SRAM has become a major component in many VLSI Chips due to their large storage capacity and little access time. SRAM has become the theme of significant research because of the fast advancement for low power, low voltage memory design during recent years due to increase demand for notebooks, laptops, IC memory cards and handy communication devices. SRAMs are broadly utilized for portable applications as both on chip and off-chip memories, because of their simplicity of use and low standby leakage.

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