

Performance Analysis of Graded Channel Double-Gate MOSFET in Nano-Regime using TCAD Simulation

Aakanksha Lakhanpal, Shashi B. Rana
Department of Electronics and Communication Engg.
Guru Nanak Dev University, Regional Campus
Gurdaspur Gurdaspur, Punjab India-143521

Ashwani K. Rana
Department of Electronics and Communication Engg.
National Institute of Technology, Hamirpur Hamirpur,
H.P. India-177005

ABSTRACT

Double-gate (DG) MOSFET has emerged as one of the most promising architecture for scaling CMOS devices down to nanometer size as compared to the planar single-gate MOSFETs. In this work, the impact of channel engineering on double gate MOSFET has been investigated. Further, the comparison of double-gate MOSFETs with the graded channel double-gate MOSFETs has been done in terms of performance parameters such as I-V characteristics, electric field, electron current density, space charge density using TCAD Simulator.

Keywords

DG-MOSFET, MOSFET scaling, Very Large Scale Integration (VLSI), SCEs, Graded Channel (GC)

1. INTRODUCTION

Along with the improvement in the device performance, the scaling is also an important goal of the VLSI industry. According to Moore's Law, the number of transistors per chip in a dense integrated circuit has doubled approximately every two years[1]. From past few years, many researchers are ardently focusing on channel material engineering of MOSFET to deal with its performance degradation due to scaling[2]. The ability of the gate electrode to control the potential distribution and flow of current in the channel reduces due to the scaling of the channel length of the device. On scaling, short channel effects (SCEs) become dominant due to the increase in the electrostatic effect of the source/drain electrodes on the channel. As a result, impact-ionization at the drain side occurs due to which electron experiences a greater force and may sometimes lead to the damage of the device. In order to reduce SCEs, the gate to channel coupling with respect to source/drain coupling must be increased. Previous studies shows that the convention bulk MOSFET already reached to its scaling limits which suggests the need for alternate device to keep pace with scaling scenario [3]. Various structures have been deployed to overcome the scaling issue of bulk MOSFET (e.g. SOI structure, multi-gate structures). For better gate controllability, multiple gate structure is used. In this paper, the double-gate MOSFET structure is considered. Due to one extra gate as compare to conventional MOS structure, the gate to channel coupling is doubled and thus reducing of SCEs. The two gates in DG-MOSFETs result in better electrostatic control over the channel and therefore, improve the scalability of the device. DG-MOSFET has higher current density as compared to conventional bulk MOSFET[4]. Many authors have reported the channel engineering i.e. graded channel (GC), as a possible solution to further improves the SCEs in nanoscale regime[5,6,7]. In this work, the graded channel double-gate (DG) MOSFETs is considered and compared with simple DG-MOSFET

structure. GC DG-MOSFET structure is analyzed in terms of hot-electron degradation and impact-ionization. In graded channel, low-high-low doping profile is taken. The higher doping at the center ensures the threshold voltage maintenance, while low doping near the source and drain ensures reduced electric field and impact-ionization.

2. DEVICE DESIGN & SIMULATION SETUP

DG-MOSFET uses two gates which are placed in symmetry at the top and bottom of the channel. The conduction channel is formed near both the gates. Both the gates are of same dimensions as well as have work function and also both are connected to the same potential so it is known as symmetric DG-MOSFET. The presence of double gate reduces the impact of the drain field line over the channel potential distribution that lowers the SCEs. Leakage current is reduced because the substrate is replaced by the second gate[8].

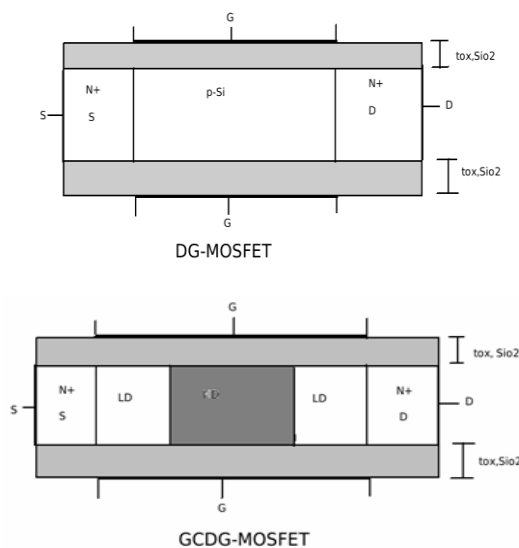


Fig. 1 Top view of DG-MOSFET and GCDG-MOSFET

For graded channel double-gate MOSFETs, the threshold voltage (V_t) implantation is performed at the source side only. The lightly doped region presents negative threshold voltage and acts as extension of the drain region under the gate, reducing the effective channel length [9].

The metal gate symmetric DG-MOSFET and GCDG-MOSFET with n channel are designed using TCAD simulator. The parameters and dimensions are shown in Table I.

2.1 Transport Description

- Drift-diffusion model

This model is based on isothermal simulation. It is widely suitable for devices with low power density and having long active regions. It is used for simulation of carrier transport in semiconductors [10]. Current density for an electron is given by:

$$J_n = qu_n E + qD_n \frac{dn}{dx} \quad (1)$$

Current density for holes is given by:

$$J_p = qp u_p E - qD_p \frac{dp}{dx} \quad (2)$$

Table 1. Device Parameters Taken for Design of DG-MOSFET and GCDG-MOSFET

S. No	Parameter	DG-MOSFET	GCDG-MOSFET
1.	Gate	10nm	10nm
2.	Gate Oxide	0.8nm	0.8nm
3.	Silicon Film	5nm	5nm
4.	Source/ Drain	$4 \times 10^{19} \text{ cm}^{-3}$	4×10^{21}
5.	Channel Doping	-	1×10^{17}
6.	Channel Doping	-	2×10^{19}
7.	Channel Doping	$2 \times 10^{16} \text{ cm}^{-3}$	-

3. RESULTS AND DISCUSSION

3.1 Electron Current Density

Current Density is defined as the amount of charges per unit area per unit time flowing in a particular direction. It is a measure of the density of the electric current [11].

Fig. 2(a) and Fig. 2(b) show the variation of electron current density in silicon film of DG-MOSFET and GCDG-MOSFET. From Fig. 2(a) it has been observed that electron current density is higher at the top and bottom of the film which forms the two conduction channel in DG-MOSFET. For Fig. 2(b) electron current density is higher in the middle of the film of GCDG-MOSFET that has good drive current than DG-MOSFET.

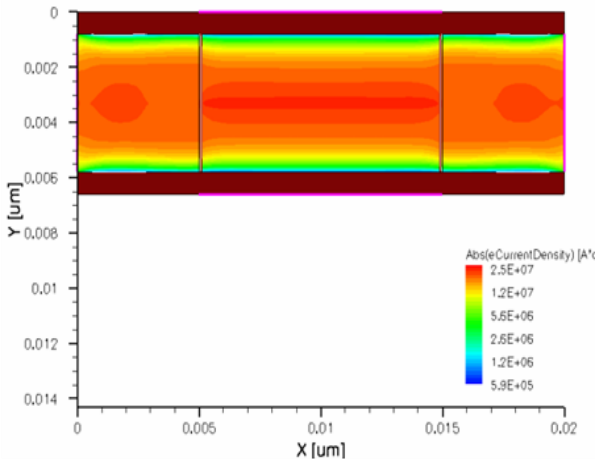


Fig 2(a). Electron Current Density in Silicon film of DG-MOSFET

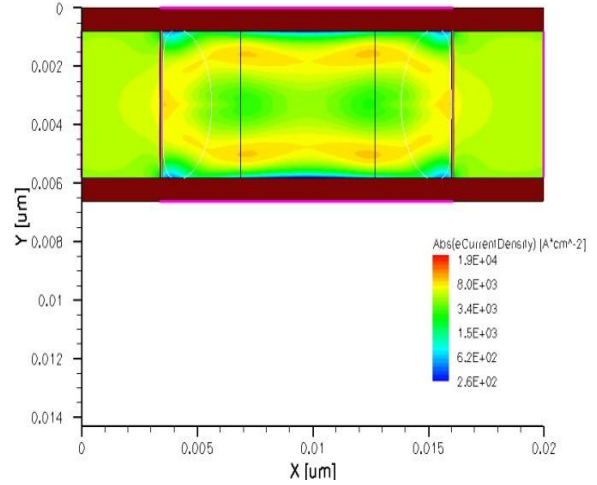


Fig 2(b). Electron Current Density in Silicon film of GCDG-MOSFET

3.2 Electric Field

Electric field is defined as the electric force per unit charge. It is the measure of intensity of electric field at a particular location. Fig. 3(a) and 3(b) shows the variation of electric field in DG-MOSFET and GCDG-MOSFET. Fig. 3(a) shows that Double gates electrically shield the channel. Fig 3(b) shows the variation of electric field in Silicon film of graded channel DG-MOSFET.

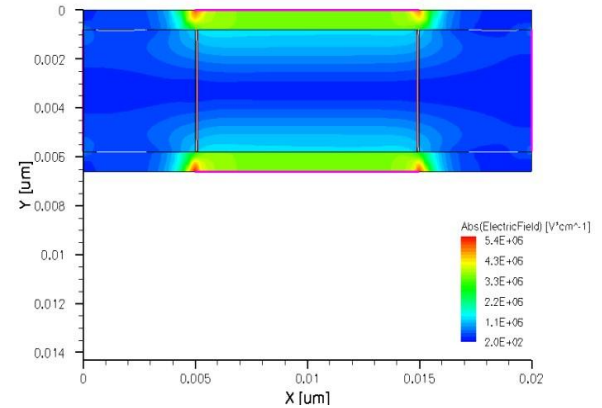


Fig. 3(a). Electric Field in Silicon film in DG-MOSFET

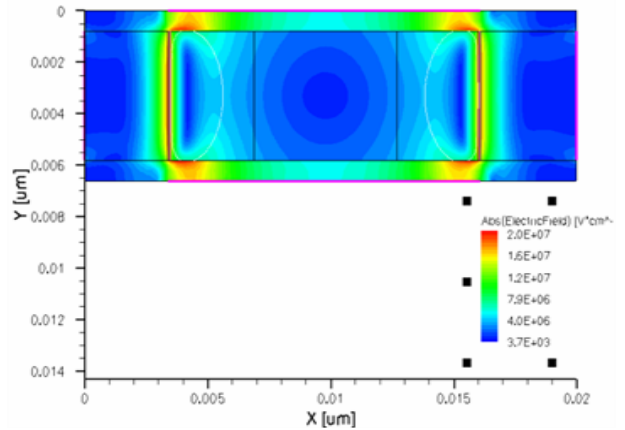


Fig. 3(b). Electric field in Silicon film of GCDG-MOSFET

3.3 I-V Characteristics

I-V Characteristics curves show the relationship between the current flowing through the electronic device and the applied voltage across the terminals. These characteristics are used as a tool to understand the basic parameters of a component.

Fig. 4(a) shows the I-V characteristics of DG-MOSFET. The presence of double gate drives the drain current to higher values. The DG-MOSFET has lower resistance and movements of ions are more due to the voltage applied from two gate terminals. Fig. 4(b) shows the I-V characteristics of graded channel DG-MOSFET. The graded channel exhibit higher drain current with lower doping on source and drain ends in comparison with DG-MOSFET because when the device gets ON, the effective channel length is determined by highly doped region, which is shorter than the physical length of the device.

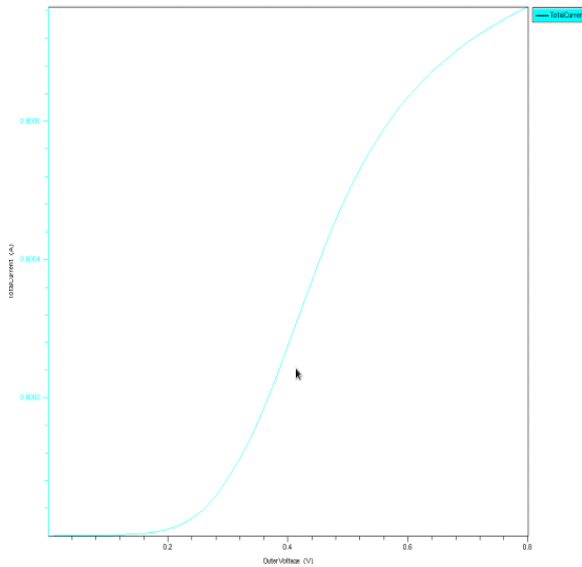


Fig. 4. I-V Characteristics of DG-MOSFET

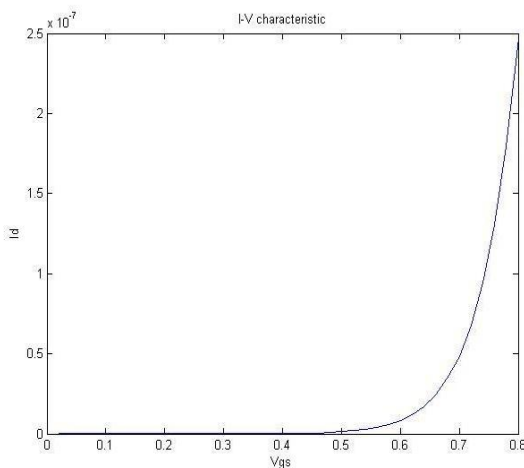


Fig. 4(b). I-V Characteristics of GCDG-MOSFET

3.4 Space Charge Density

Space charge density is the charge density that exists in free space.

Fig. 5(a) and 5(b) shows the variation of space charge density in the DG-MOSFET and GCDG-MOSFET. Fig 5(b) shows that there is a decrease in the space charge density at the source and drain side as compared to DG-MOSFET [12]. This

allows the lower electric field which enables the electron to move with lesser velocity through the channel thus reducing impact-ionization [13].

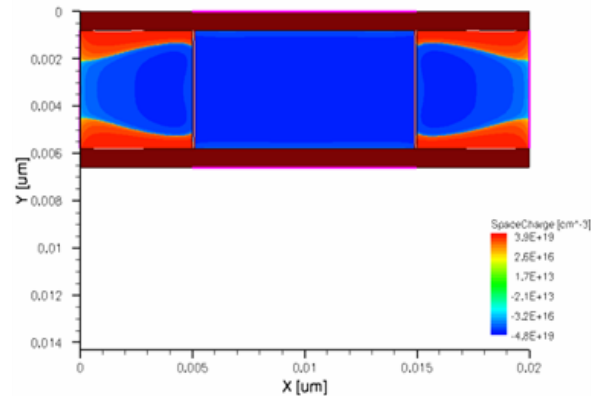


Fig. 5(a). Space charge density in Silicon film of DG-MOSFET

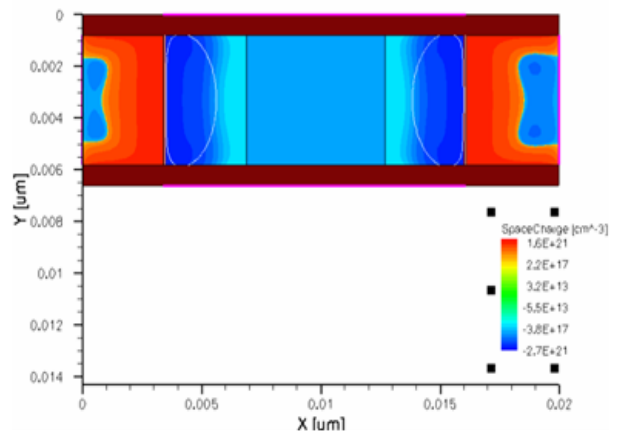


Fig. 5(b). Space charge density in Silicon film of GCDG-MOSFET

4. CONCLUSION

From the above discussions, it has been concluded that GCDG-MOSFET is more superior in terms of space charge density, I-V characteristics in comparison to the DG-MOSFET. The channel engineering is allowed only in permissible limits. The channel doping cannot be increased beyond a certain limit as some parameters like sub threshold swing and drain induced barrier lowering may degrade. Also impact ionization is reduced with the doping in the channel region.

5. ACKNOWLEDGEMENT

The author acknowledges with gratitude the technical support from NIT Hamirpur and GNDU Regional Campus Gurdaspur.

6. REFERENCES

- [1] G. Moore "Cramming more components onto integrated circuits" Electronics 38,114(1965).
- [2] D. G. Borse, K. N. M. Rani, N. K. Jha, A. N. Chandorkar, J. Vasi, V. R. Rao, B. Cheng, and J. C. S. Woo, "Optimization and realization of sub-100nm channel length single halo p MOSFETs" IEEE Trans. Electron Devices, vol. 49, no. 6, pp. 1077-1079, Jun. 2002.
- [3] G. Nicholas, T. J. Grasby, E. H. C. Parker, T. E. Whall, and T. Skotnicki, "Evidence of reduced self-heating in strained Si MOSFETs," IEEE Electron Device Lett., vol. 26, no. 9, pp. 684-686, Sep. 2005.

- [4] M. Jeong, H. S. P. Wong, E. Nowak, J. Kedzierski and E. C. Jones, "High performance double-gate device technology challenges and opportunities" Proc. Int.Symp. On Quality Electronic Design, pp. 492- 495, 2002.
- [5] M. A. Pavanello, J. A. Martino, V. Dessard, D. Flandre, "Analog performance and application of graded-channel fully depleted SOI MOSFETs," Solid State Electron, vol.44, no.7, pp. 1219-1222, Jul.2000.
- [6] M. A. Pavanello, J. A. Martino, D. Flandre, "Graded-channel fully depleted silicon-on-insulator n-MOSFET for reducing the parasitic bipolar effects," Solid-State Electron, vol.44, no.7, pp. 917-922, Jun. 2000.
- [7] M. A. Pavanello, J. A. Martino, J. P Raskin, D. Flandre, "High performance analog operation of double gate transistors with the graded- channel architecture at low temperatures," Solid-State Electron, vol. 49, no.10, pp. 1569-1575, Oct. 2005.
- [8] I. D. Mayergoyz, "Solution of the non-linear Poisson equation of semiconductor device theory," J.Appl.Phys., 59, pp. 195-199, 1986.
- [9] E. Contreras, A. Cerdeira, M. A. Pavanello, "Application of the symmetric doped double-gate model in circuit simulation containing double-gate graded-channel transistors," Solid-State Electronics, vol. 52, pp. 830-837, 2008.
- [10] "Sentaurus Device User Guide", Version A-2008.09, September 2008, Synopsys International.
- [11] ISE TCAD:Synopsys Sentaurus Device simulator.
- [12] R. K. Sharma, Mridul Gupta, "TCAD assessment of device design technologies for enhanced performance of nanoscale DG-MOSFET," IEEE Trans. on Electron Devices, vol. 58, no. 9, Sept. 2011.
- [13] J. Lyu, B. G. Park, K. Chun, J. D. Lee, "Reduction of hot-carrier generation in 0.1 μ m recessed channel n-MOSFET with laterally graded channel doping," IEEE Trans. Electronic Devices Lett., vol. 18, no.11, pp. 1962-1967, Nov.2002.