Performance Optimization of CP-PLL for SoC Applications

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ABSTRACT
Phase locked loops (PLLs) are integral parts of communication devices used in various applications such as frequency synthesizer, clock recovery circuits, synchronization for digital communications, carrier phase, frequency tracking, etc. The non-ideal effects in PLL such as jitter, phase noise, reference spurs, phase error, etc. influence the PLL performance which significantly affects the overall system. For example, a 10% performance degradation of PLL leads to approximately 20% performance degradation of frequency synthesizers. In conventional CMOS charge pump circuit, phase error is caused due to leakage current, timing mismatch and current mismatch. The phase error due to current mismatch is more significant as compared to phase error due to timing mismatch and leakage current. Thus, in this work, two charge pump circuits with minimum area are designed in Matlab Simulink environment to reduce current mismatch. The designed charge pump using basic current mirror is compared with the ideal current mirror. Simulated results show that current mismatch and phase error for basic current mirror are approximately 12.19 % and 0.3480 rad. respectively. This set up can be easily utilized to design various charge pump to achieve minimum current mismatch for SoC applications.

General Terms
Charge Pump PLL, Matlab Simulink

Keywords
Charge Pump, Current Mismatch, Current Mirror, Design and performance of Charge Pump.

1. INTRODUCTION
CP-PLL (Charge Pump PLL) is currently the most commonly used PLL architecture for SoC environment. CP-PLLs are used in many areas such as communications, wireless systems, consumer electronics, and motor control. The typical communication applications of CP-PLL include frequency synthesizer, clock recovery circuits, synchronization for digital communications, carrier phase and frequency tracking, etc.

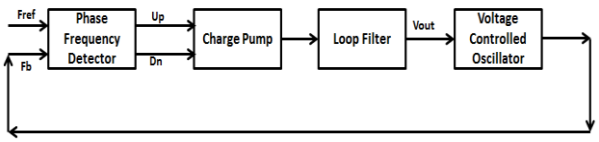

Fig 1: Block diagram of CP-PLL

A conventional CP-PLL consists of a phase/frequency detector (PFD), a charge pump (CP), a loop filter (LF) and a voltage-controlled oscillator (VCO) as shown in figure 1. CP-PLL is responsible for synchronizing the output signal of the VCO(Fb) against a reference signal (Fref) in both frequency and phase[1].A CP-PLL is a mixed-signal circuit, involving the co-design of RF, digital, and analog building blocks. PFD is a digital circuit which generates pulses based on differences in frequency and phase between a reference signal and a feedback signal and outputs a digital pulse (Up or Dn) whose width is proportional to the phase error. Up signal is generated when phase of Fref leads phase of Fb and a Dn signal is generated when phase of Fb leads phase of Fref. CP circuit converts digital error pulse to analog error current. CP is an electronic switch controlled by the PFD, which delivers current according to the Up and Dn signals. The LF converts the CP current into a voltage Vout. The VCO receives the loop filter voltage and generates an output signal whose frequency is based on the loop filter voltage. The control voltage moves the oscillator frequency in the direction of eliminating the phase difference between Fref and Fb. As the voltage on the loop filter increases the frequency of the VCO increases to cause the phase of Fb to increase and align with Fref, which causes the output signal (Fb) to synchronize with the input signal (Fref). In CP-PLL, CP is a small circuit part but it plays an important role in determining the overall performance of CP-PLL. The basic charge pump circuit is shown in figure 2.

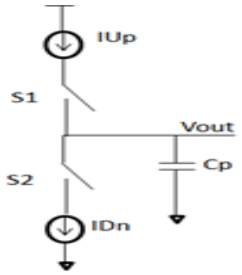

Fig 2: Basic Charge Pump

The CP circuit consists of two switched current sources IUp (charging current source) and IDn (discharging current source), implemented using MOS transistors. Ideally, the charge pump currents IUp and IDn need to be equal in magnitude but the inherent mismatches between the PMOS and NMOS transistors result in mismatching between the current sources. The mismatch between charging and discharging current is known as current mismatch and it degrades the performance of CP[2].As the performance of CP-PLL determines the performance of SoC application, proper designing of CP for faithful response is desired. The table below shows the application and the different performance parameters of CP-PLL.

Table 1. Application of CP-PLL

S. No.	Parameters	Application of PLL				
		Frequency Synthesizer [3]	Clock and Data Recovery Circuit [4],[5]		PLL for clock multiplication [6],[7]	
1	Process (µm)	0.18	0.4	0.18	0.4	0.6
2	Supply Voltage (V)	1.8	3.3	2.5	2.5	3-5.5
3	CP current Mismatch (%)	0.4	-	-	-	-
5	CP current (µA)	100	-	-	-	-
6	Reference Spur (dBc/Hz)	-	-80	-	-	-
7	Power Consumption (mW)	0.9-3.6	33.5	72	<100	-
8	Jitter (ps)	-	10.8	1	10	3.1
9	Frequency (MHz)	-	-	-	-	300 - 400

The range of parameters specified in the table 1 varies depending on the application and the frequency. To remove the non-ideal effects in CP, different architectures are proposed. Charge pump are broadly classified into two categories: "Single ended charge pump" and "Differential charge pump". In this work, single ended topology is considered over to a differential CP topology in order to reduce the area and power consumption[8]. Hence, in single ended topology, a good design of current mirror and switch will reduce the total phase error of the CP-PLL.

The paper is organized as follows. In section 2,non-ideal effects of CP are discussed. In section 3,design of current mirror and switch for CP in Matlab /Simulink /Simscape /Simelectronics environment is presented. In section 4, simulation results are reported and the effects of current mismatch are investigated.

2. NON IDEAL EFFECTS IN CP CIRCUIT

In CP-PLL phase error and reference spurs are present due to non-idealities in CP. The different non ideal effects present in CP are as given below (refer figure 2):

1. Leakage current

This is a common non-ideal phenomenon in submicron CMOS technology. The output leakage current in the charge pump causes spikes on the VCO control voltage. Phase error due to leakage current is given by:

$$\Delta\emptyset leakage = 2\pi \frac{Ileakage}{Icp} \quad \ldots\ldots (1)$$

Where $Ileakage$ - leakage current

Typically, the phase error due to leakage current can be ignored because the average level of $Ileakage$ is at a magnitude of pA.

2. Timing Mismatch

Timing mismatch consists of a) propagation delay between the logical output of PFD and the CP switches, b) Propagation delay for the CP switches to change the state, c) Dead Zone of PFD. This delay introduces a certain amount of phase error given by:

$$\Delta\emptyset timing = 2\pi \frac{\Delta Tdelay \cdot Ton}{Tref^2} \quad \ldots\ldots (2)$$

Where $\Delta Tdelay$ - propagation delay due to connectionbetween PFD and CP switch and propagation delay for CP switch to change state and Dead Zone, $Tref$ - reference cycle time, Ton - turn-on time of the PFD.

3. Current Mismatch

Current mismatch consists of a) Mismatch between the drain currents of the current sources, b) Mismatches due to switch non-idealities such as charge sharing, charge injection, clock feed through. The current sources present in CP are designed using MOS transistors. Due to the inherent mismatches present in transistors such as 2nd order effects and random device mismatches, CP suffers from current mismatches [9].Current mismatching refers to the magnitude difference of charging and discharging currents. Phase error due to charge pump current mismatch is given by:

$$\Delta\emptyset mismatch = 2\pi \frac{\Delta i}{Icp} \cdot \frac{Ton}{Tref} \quad \ldots\ldots (3)$$

Where Icp - rating current of CPs, $Tref$ - reference cycle time, Ton - turn-on time of the PFD and Δi - mismatching of currents due to current mirror and due to switches.

The propagation delay for the CP switches discussed in timing mismatch i.e time taken to change the state by switches and current mismatch are interlinked as both the circuits are made of MOS transistors. Hence the non-idealities contributing to these phenomenon are discussed separately in further points.

4. Charge Sharing

The capacitors at nodes 'a' and 'b' consist of the parasitic source/drain capacitances of MOS transistor. As shown in figure 3, when the switching transistors are open, the charges on the nodes 'a' and 'b' move towards VDD and GND respectively. When the switches close instantaneously, some of the charge stored on these parasitic capacitors will be transferred to the LF, and cause voltage spikes on the VCO control line.

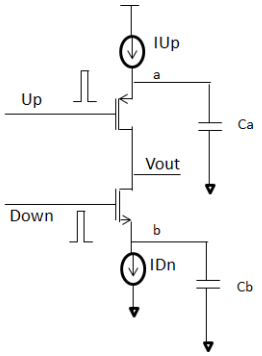

Fig 3: Charge Sharing in CP

5. Clock feedthrough

When the Up and Dn signals change their logic levels, due to the gate-drain capacitance of the MOS transistors, some charges are coupled to the LF which causes spikes on the control voltage which leads to reference spurs at the output.

6. Charge Injection

Charge injection is a phenomenon that arises due to leakage of charge into a capacitive node during the turn on and turn off

of a switch that is connected to that node. Charge injection and clock feed through is directly proportional to gate capacitance. Therefore, a small sized switch is required to reduce the effects of charge injection and clock feed through.

The total phase error $\Delta\emptyset tot$ caused by these non-idealities can be approximated as:

$$\Delta\emptyset tot = 2\pi\ (\Delta\emptyset leakage + \Delta\emptyset mismatch + \Delta\emptyset timing)..(4)$$

The phase error due to leakage current accounts to 1% of the total phase error. Therefore the phase error is dominant due to the current mismatch and timing mismatch[3].

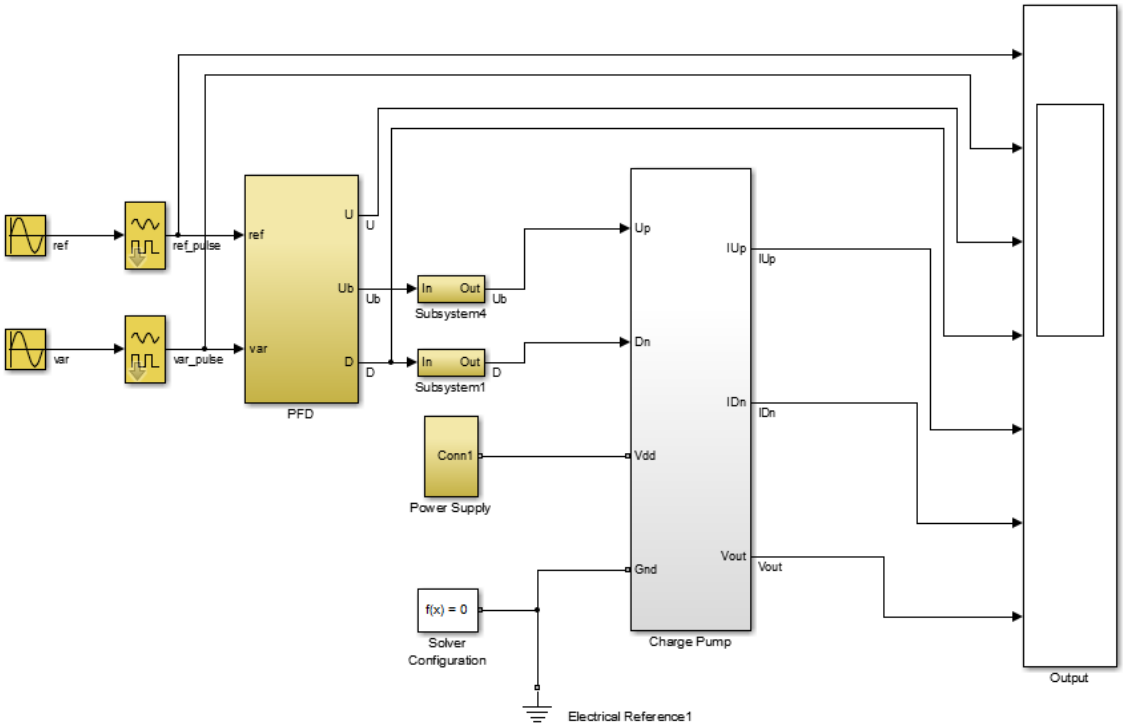

Fig 4: Phase detector circuit used in CP-PLL

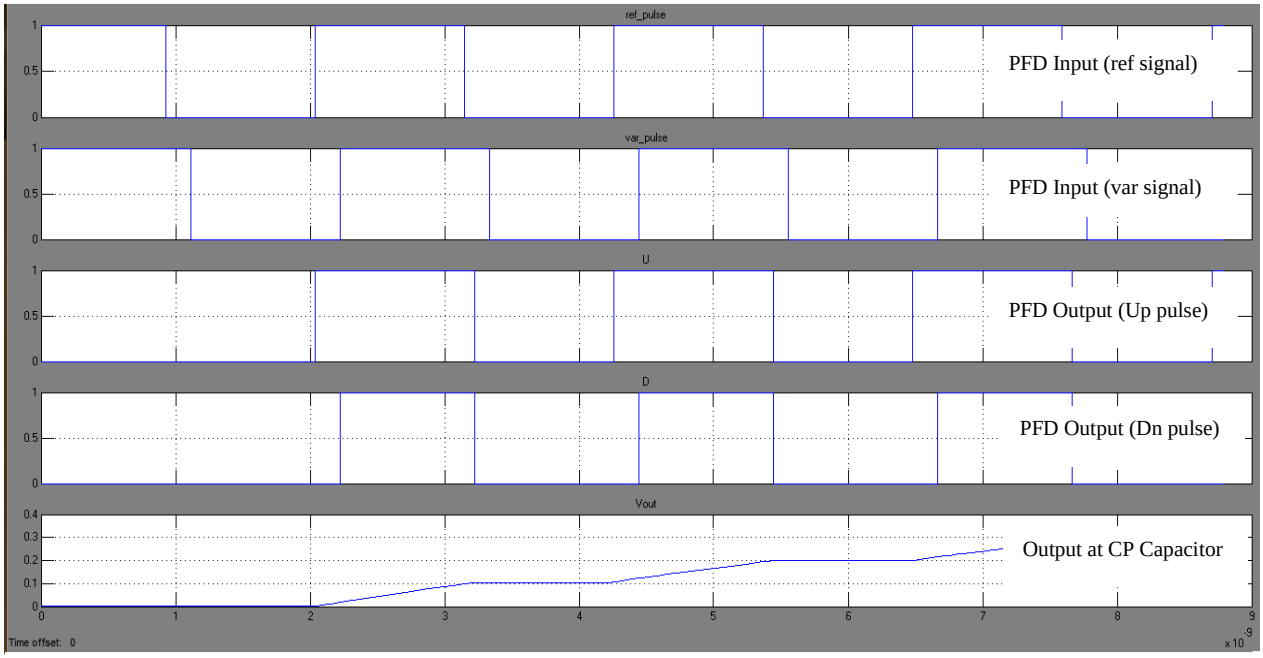

Fig 5: CP response for Reference signal leading variable signal

3. CHARGE PUMP CIRCUIT DESIGN

The set up for phase detector circuit used in CP-PLL circuitis designed in Matlab Simulink Simelectronics, Spice compatible environment by using 0.18 μmlevel 3 CMOS model with 3.3V supply as shown in figure 4. The output of the CP is captured on scope. The designed CP system is combination of two main sub system PFD and a single ended CP. The subsystem gives the flexibility to reduce the complexity and size of the circuit [11].The design of sub

system PFD is shown in figure 6. The PFD subsystem consists of two edge-triggered, resettable D Flip-Flops (DFF) with their D inputs connected to logic "1". When one of the PFD inputs rises, the corresponding output becomes high. The phase or frequency difference information is stored in the capacitor which is used to tune the VCO.

The design of single ended CP subsystem is shown in figure 7. CP subsystem consists of PMOS and NMOS current mirror subsystem (refer figure 8 and 9 respectively) with Up switch and Dn switch.

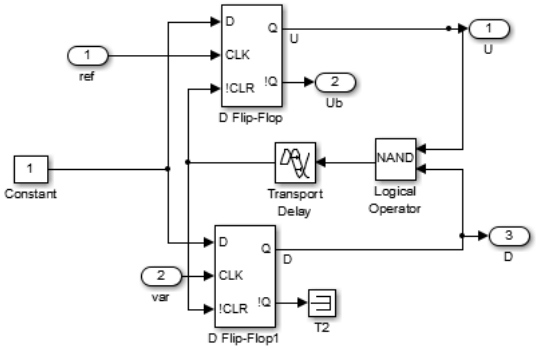

Fig 6: PFD subsystem

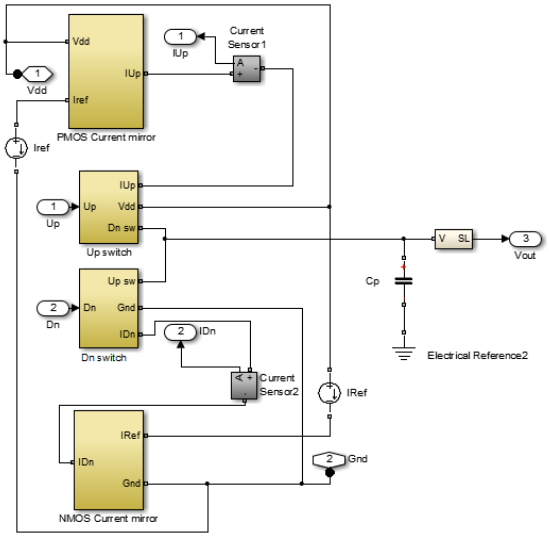

Fig 7: CP subsystem

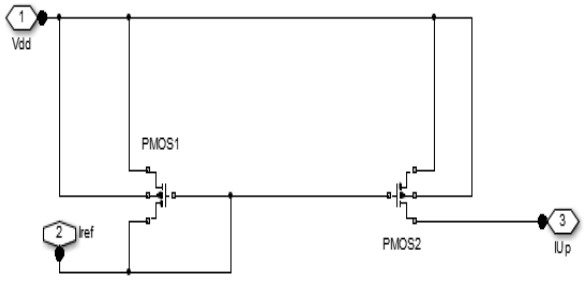

Fig 8: PMOS current mirror subsystem

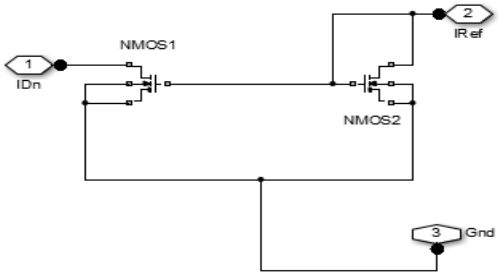

Fig 9: NMOS current mirror subsystem

3.1 Current Mirror Design

The current sources in CP are designed using current mirror circuits. The current mirror circuit uses the principle that if the gate-source potentials of two identical MOS transistors are equal, then the current flowing through their drain terminals should be the same. The PMOS and NMOS current mirror subsystem are shown in figure 8 and 9 respectively. The W/L ratios of the MOS transistors are designed using the drain current equation 5.

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \quad \text{..... (5)}$$

Where

I_D= Drain current
μ_n= Surface Mobility
C_{ox}= Oxide Capacitance per unit area
W= Width of the MOS transistor
L= Length of the MOS transistor
V_{GS}= Gate to source voltage
V_T = Threshold voltage
λ = Channel length modulation coefficient
V_{DS} = Drain to source voltage

3.2 Switch Design

Up switch and Dn switch as shown in figure 7 are used to supply current according to the PFD signals. To reduce the charge injection and clock feed through the switch size should be minimized. The switch on state resistance (R_{on}) is given by

$$R_{on} = \frac{1}{\left(\frac{W}{L}\right)\frac{\mu_n C_{ox}}{2}(V_{GS} - V_T)} \quad \text{..... (6)}$$

Increased switch size results in glitches at the output and slow switch operation.

By proper design of current mirror circuit and switch used in CP, the phase error and the reference spurs of CP-PLL are reduced significantly.

4. SIMULATION RESULTS AND DISCUSSIONS

When the ref signal leads the var signal, the PFD detects a rising edge on the reference frequency and produces an Up signal. This Up signal from the PFD will turn the Up switch on. This Up pulse will turn on the charging current source and it will cause the CP to inject current into the LF, thus increasing Vout. The obtained simulated result is shown in figure 5.

The variation of output current against the W/L ratio of MOS transistors used in current mirror circuit is shown in figure 10. It is observed that, the output current varies linearly to the input current and saturates at higher aspect ratios. Hence to achieve Ip=100uA with minimum area, the W/L ratio of MOS transistors in current mirror is chosen to 25.

The current transfer characteristics of basic current mirror for the chosen W/L ratio of MOS transistors in current mirror is shown in the figure 11. From the waveform it is concluded that output current almost tracks the input current.

The output characteristics plot of the same is shown in figure 12. It shows that, after 3V a steady output current of 100uA is achieved. To lower R_{on}, of switch, W/L ratio of MOS transistors must be increased but there exists a tradeoff between R_{on} and switch non-linearities [2], [11].

Therefore, switch size should be optimized to minimize R_{on} and glitches. The variation in the on-state resistance (R_{on}) due to W/L ratio of MOS transistor switches is shown in figure 13 with the process transconductance parameters are fixed.

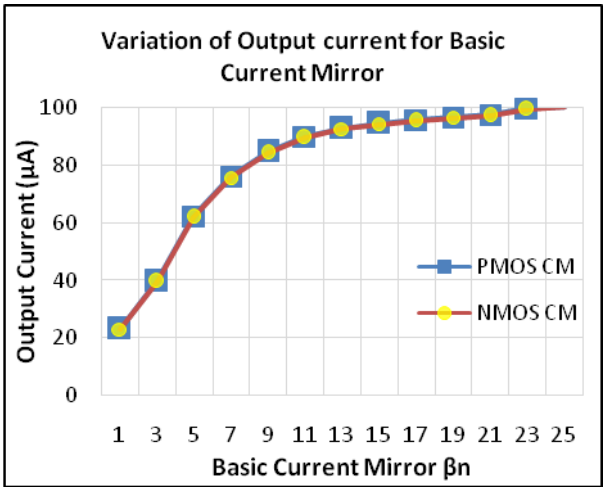

Fig 10: Variation of Output current with respect to W/L

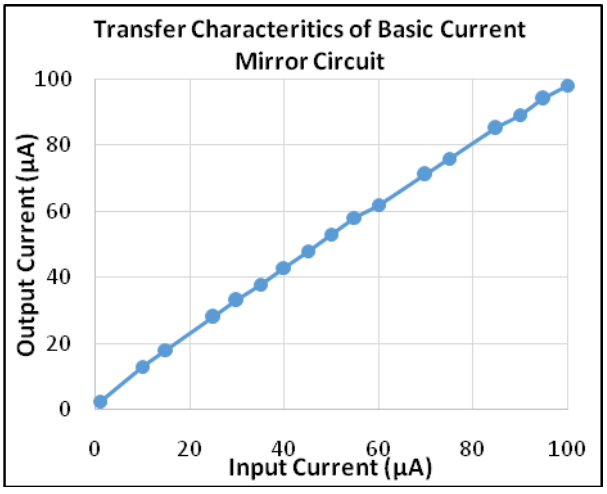

Fig 11: Transfer Characteristics of Basic Current Mirror

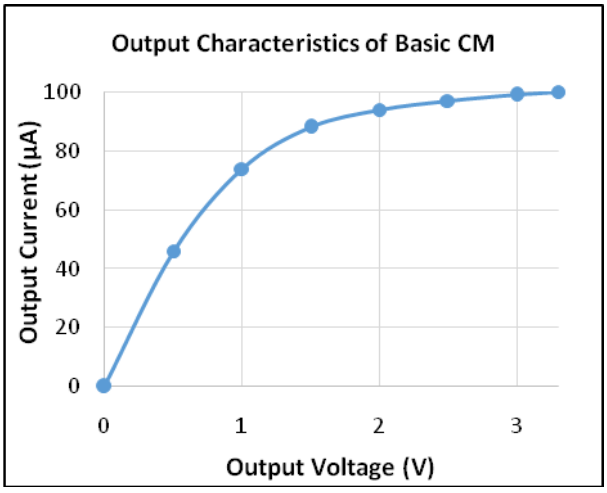

Fig 12: Output Characteristics of Basic Current Mirror

The designed set up for phase detector of CP-PLL is simulated at 450 MHz with two different current sources and MOS designed switches. The obtained phase error with respect to the current mismatch is listed in table 2.

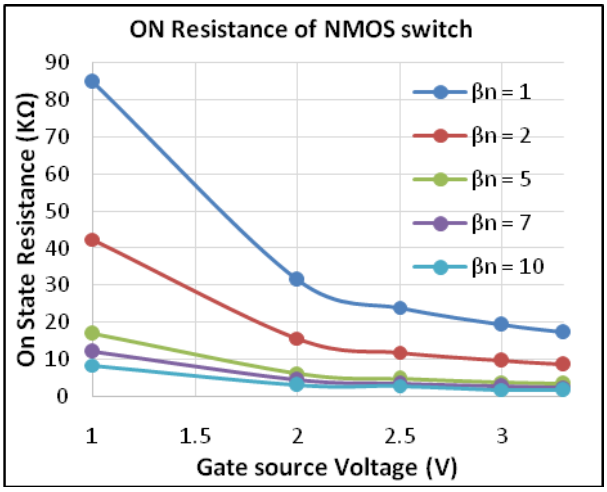

Fig 13: Variation of Ron with respect to W/L

From figure 10 and 13, it is concluded that the individual sub system is designed to achieve desired results. But, when the all individual sub systems are combined, it is concluded that the non-ideal effects contribute to current mismatch leading to an equivalent phase error.

Table 2. Comparison of phase error due to current mismatch

Sr. No.	Current Mirror Circuit	Current Mismatch (%)	Phase error due to current mismatch (rad.)
1.	Ideal current source	0 μA	0
2.	Basic current mirror	12.19 μA	0.3480

5. CONCLUSION

A CP circuit design for current mirror and switch in phase detector CP-PLL is proposed. The complete set up is designed and simulated in Matlab Simulink Simelectronics in 0.18 um CMOS technology. It is concluded that CP circuit requires the combination of various sub systems to achieve the desired results. To reduce the non-linearities of CP, an efficient combined design of current mirror and switch is required. The current mismatch of the CP can be reduced by increasing the output resistance of CP circuit which in turn will improve the performance of CP-PLL. In future, the improved current match circuit will be designed to reduce the static phase offset and reference spurs of a charge pump PLL.

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