A Novel Method to Design Power Converter for Energy Harvesting System

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ABSTRACT

In today's world, there is a huge demand for portable electronic systems such as RFID cards, PDA, watches, calculators, cell phones, flash memories, MEMS, LCD drivers etc. The limited battery lifetime is the main concern of many portable systems. Energy harvesting system overcomes these problems by converting non-conventional energy into useful energy. The power converter plays an important role in boosting low voltage available from transducer hence; they are key element in energy harvesting system. The topologies and design specification such as low on-chip power requirement, high power efficiency, less area etc. of power converter varies widely as per the application.

In this work, a new method is proposed to design power converters of desired specifications. This method is designed in MATLAB Simulink and Orcad environment and helps user to optimize the parameters such as boosting capacitance value, transistor sizing value, number of stages etc. This method can be used by designers as the first step to evaluate all the performance parameters before actual chip fabrication. Thus it will give user confidence in its design, save valuable time and overall design cost. The various topologies of power converters such as Basic Dickson, Modified Dickson and Cross-Coupled Voltage Doubler are designed using this method and shows better performance results.

General Terms

VLSI Design, Renewable Energy

Keywords

Power Converter, Energy Harvesting, CTS (Charge Transfer Switch), MOS.

1. INTRODUCTION

The non renewable sources of energy like coal, lignite, oil, and gases are limited and their reserves are diminishing drastically. Therefore, there is an urgent need of Energy Harvesting, the process of converting ambient energy from environment renewable sources like solar, wind, biomass, tidal, fuel cell, vibration etc. into electrical energy [1]. The harvested energy is used to either drive a low power circuit or the energy is stored for later use. Over the last 10 years, Energy Harvesting has become popular and adopted by various industries in many applications such as wireless sensor networks, health monitoring system, defense etc. to extend the lifetime of battery or to make these battery operated systems self autonomous [2].

The block diagram of energy harvesting system is shown in figure 1. The energy harvesting system consists of three crucial blocks energy generators, power converter and the required application or energy buffer.
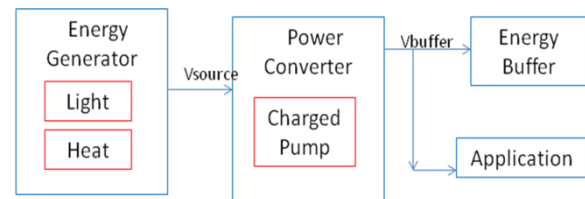

Fig 1: Block Diagram of Energy Harvesting System [4]

In energy harvesting systems, transducers are used to convert the natural energy into electrical energy but the converted energy is not sufficiently high to drive the load therefore there is a need to design DC-DC power converter which will boost the energy supplied by natural energy sources [4].

Power converters are broadly classified as Inductive and Inductor-less power converter. Inductor-less power converters require only capacitors to store charge and switches to transfer these charges to output stage for producing higher voltages. Thus, Inductor-less power converters have reduced weight compared to transformers and amplifiers i.e. it has less electro-magnetic interference (EMI) as well as it can be integrated easily in system-on-chip IC's [5].

There are various topologies available for power converters which are broadly categorized as Dickson, Cross-Coupled Voltage Doubler, Makowski power converters etc. Makowski power converter has large gain whereas, it suffers due to very complex circuit designs as its structure changes for low and high gains and it requires more number of clocks and MOSFETs therefore its area also increases [6]. Dickson power converters have simple control method, it is easy to design therefore most of the conventional power converters are based on the topology proposed by Dickson [7]. But it suffers the threshold voltage drop at each stage. Cross-Coupled Voltage Doubler gives better power efficiency and output voltage with no threshold drop.

Power converter is the intermediate circuit in an energy harvesting system and its design generally keeps on changing with respect to design and performance parameters. To change any parameter, the designer needs to do modification at the device level, which is very difficult and time consuming. Thus, power converter design must be automatic and realistic. Researchers have designed power converter circuit in electronic circuit tools like HSpice, PSIM, PSpice, AMS etc. As these software packages cannot simulate control algorithms therefore it is required to use other tool for the simulation of control algorithms. It is also possible to design complete energy harvesting system in MATLAB tool including non-conventional energy source, power converter and the required application [8][9][10] but MATLAB tool is

not able to model electronic components accurately. The major disadvantages of previous methods are they are not platform independent and the modifications of designs were not automatic. Thus, the designer requirement is a method which is platform independent and automated.

In this paper a novel design method is described and the three important topologies Basic Dickson, Modified Dickson and Cross-Coupled Voltage Doubler power converters are designed using the novel methodology discussed in section 2 and results are compared in section 6.

2. A NEW APPROACH TO DESIGN POWER CONVERTER

Although the modern analog and mixed signal designs CAD tools have accelerated the designed process by continuously upgrading the CAD tools. Each tool doesn't satisfy all required design features. In order to make the system automatic and fast, designer has to employ a new approach in which two platforms can be interfaced to produce the final output. O.A. Ahmed has discussed about two co-simulation tools which co-simulate PLECS and PSpice with MATLAB Simulink. The reference discussed that PLECS co-simulation does not give a realistic simulation because it does not consist of realistic models of components. Whereas PSpice and MATLAB co-simulation via SLPS interface gives the designer confidence to predict the real behavior of system as PSpice consists of realistic models [11].

In this work, an automated design is carried out. An automated program is written using design equations which are discussed in section 3 in MATLAB m-file. The performance parameters are taken as input i.e. the designer can enter the required performance parameter values such as output voltage, input voltage, allowed ripple voltage, load resistance and frequency of operation. The automated program suggests the different topologies. The design parameters will be given as output result based on the chosen topology. The obtained output results are useful to design and modify the device level design (PSpice model) for e.g. length and width of MOS.

```
enter output voltage 12

Vout =

     12

enter input voltage3.3

Vin =

     3.3000

enter allowed ripple0.1

Vr =

     0.1000

enter load resistance1e7

R1 =

     10000000

enter frequency of operation1e7

f =

     10000000
```

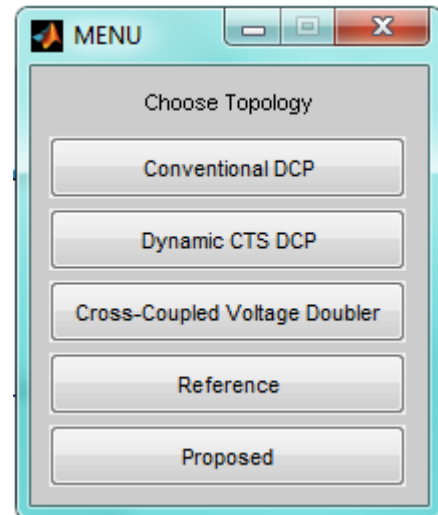**Fig 2: Assigning Performance Parameters as Input to Automated Program**

Fig 3: Choice Menu of Automated Program

```
Topology is Conventional DCP
width w=4um and length l=0.18um
value of Boosting Capacitor is 8.000000e-013
Number of Stages is N= 4
value of Output Capacitor is Cout= 1.200000e-012
value of Output Current is Iout= 1.200000e-006
Efficiency of this topology is n= 2.131939e+001
Output Power of this topology is Pout= 1.440000e-005
>> |
```

Fig 4: Design Parameters obtained as Output from Automated Program

2.1 Co-Simulation of MATLAB and Orcad through SLPS Interface

To co-simulate PSpice and MATLAB, the SLPS (SimuLink PSpice) interface has been co-developed by Cadence and Cybernet Systems [11]. For the evaluation of system, the transistor level model is firstly designed and analyzed in PSpice and project file is to be created in Orcad environment. After that, the PSpice model is embedded in MATLAB SIMULINK model as a sub-circuit block using SLPS interface. Input and output signals must be defined in SLPS to get the output result.

The figure shows how PSpice model is embedded in MATLAB Simulink through SLPS interface. The PSpice model is enclosed in SLPS block. The input and output signals are defined based on the requirement.

Fig 2: Co-Simulation Model in Simulink using SLPS Block

The project file which is created in Orcad is to be browsed from MATLAB Simulink environment and then the PSpice circuit file automatically gets selected. To specify input the corresponding node on which input is to be given is added using select button of input key. The node from which output is seen is added using select button of output key.
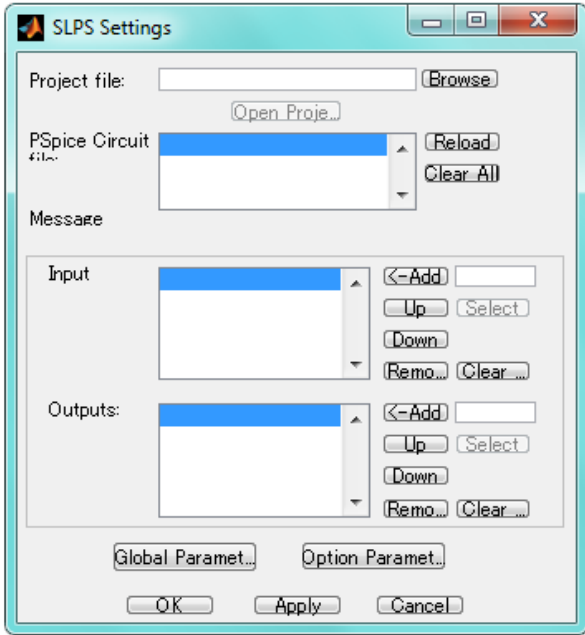
Fig 3: Assigning Input and Output nodes to SLPS Block

2.2 Advantages of Co-Simulation

The method of co-simulation is discussed in section 3.1. The simulation of PSpice model with Simulink is run in MATLAB environment. As it is said the design of power converter keeps on changing therefore an automatic code is written in MATLAB m-file which gives design parameters as a result based on the specified performance parameters. Thus, a complete system can be simulated on one platform and the designer can evaluate the design process before the actual fabrication.

The advantages of this method are [11]:

- For co-simulation, the step time in PSpice and Simulink need not be same.
- Designers can also design and simulate electro-mechanical and hydraulic designs using SLPS interface.
- This new simulation performance technology saves time, improves reliability and provides enhanced designs.
- It simplifies viewing of simulation results (both analog and digital) by having a single display for the mixed signal analysis results.
- This technique allows system-level interfaces to be tested with actual electrical designs emulating real-world applications.

Three topologies are designed using above method which is discussed in section 3, 4 and 5.

3. BASIC DICKSON POWER CONVERTER DESIGN

The basic configuration of a Dickson power converter is shown in Fig. 1. This is the topology which is highly used in industries. It consists of number of identical stages. Each stage consists of MOS switch to transfer energy from one stage to other and capacitor to store the energy. Each capacitor is connected to pumping clock. Two pumping clocks are used *clk* and *clk_bar*, which are anti-phase and have voltage amplitude equal to supply voltage *Vin*. The number of stages can be adjusted depending upon the required output voltage.
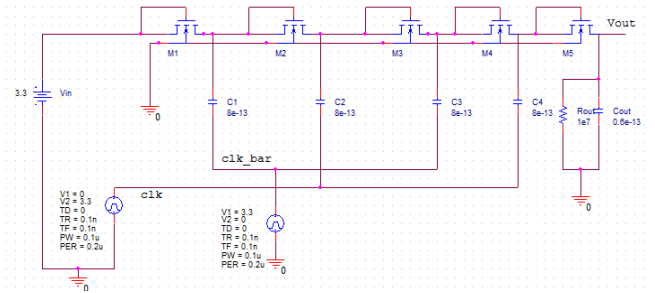

Fig 4: A Four-Stage Conventional Dickson Power Converter

When *clk* is low and *clk_bar* is high then NMOS *M1* conducts till voltage at node1 becomes equal to *Vin-Vth*. Now when clk is high and *clk_bar* is low then total voltage at node1 appears to be [6]

$$Vin - Vth + Vclk \qquad (1)$$

Therefore total voltage at node1 at end of first cycle is

$$Vin + Vclk - Vth \qquad (2)$$

This causes NMOS *M2* to conduct when *clk* is high and *clk_bar* is low until voltage at node2 becomes equal to

$$Vin + Vclk - Vth - Vth$$
$$= Vin + (Vclk - Vth) - Vth \qquad (3)$$

So, the output voltage after N stages is given by:

$$Vout = Vin + N(Vclk - Vth) - Vth \qquad (4)$$

If the load is connected and it draws current *Iout* then the output voltage is given by [7]:

$$Vout = Vin + N(\left(\frac{c}{c+cs}\right)Vclk - Vth - \left(\frac{Iout}{(c+cs)*f}\right)) - Vth \qquad (5)$$

Where, *Vout* is Output Voltage, *Vin* is input supply voltage, *N* is number of stages, *c* is boosting capacitor, *cs* is parasitic capacitor, *f* is clock frequency, *Vth* is MOS threshold voltage , *Iout* is output load current and *Vclk* is clock amplitude.

The basic Dickson power converter circuit is easy to implement, low cost, easily integrated in system-on-chip IC's but the disadvantages of this circuit limits its usage in industrial applications. The disadvantages are its output voltage gain decreases due to body effect because at each stage threshold voltage increases so as to subtract higher value from resulting output voltage [12, 13] and the NMOS switches cannot be completely turn off which results in energy loss and the final output voltage decreases.

4. MODIFIED DICKSON POWER CONVERTER CIRCUIT DESIGN

Due to the disadvantages of basic Dickson Power Converter Circuit a modified DCP was designed with charge transfer switches with dynamic control. This circuit is also based on Dickson topology only the single NMOS switches in each stage is replaced by CTS switches with dynamic control. For

dynamically controlling CTS switches, CMOS inverters (MNi's and MPi's) are used which make sure that charge sharing doesn't occur by properly turning on and off NMOS MSi [7, 8]. Therefore, it gives better performance.
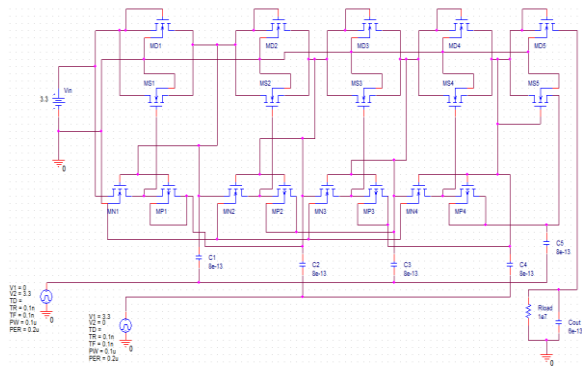

Fig 5: A Four-Stage Modified Dickson Power Converter

The threshold voltage drop problem in Basic DCP is overcome by this modified circuit but the output stage still consists of diode configuration therefore voltage drops at output stage.

5. CROSS-COUPLED VOLTAGE DOUBLER POWER CONVERTER CIRCUIT DESIGN

If the problem of diode configured output stage can be overcome then the pumping performance will increase therefore one more topology is designed Cross-Coupled Voltage Doubler. In this topology NMOS and PMOS switches are connected in cross-coupled form and the bulks are connected to their sources to avoid body effect [14]. In each stage this topology requires 2 NMOS and 2 PMOS therefore total number of switches required for their topology is 2N NMOS switches and 2N PMOS switches i.e. 4N switches and 2N boosting capacitors.

In Cross-Coupled Voltage Doubler, two stages get connected in one clock cycle for transferring charges to the next stage. For example, when *clk=0*, MP5 and MN7 conduct and transfer charges from stage 1 to stage 2. MOS MN5, MP1, MN2 and MP6 are turned off to block the charges from going back to the previous stage.
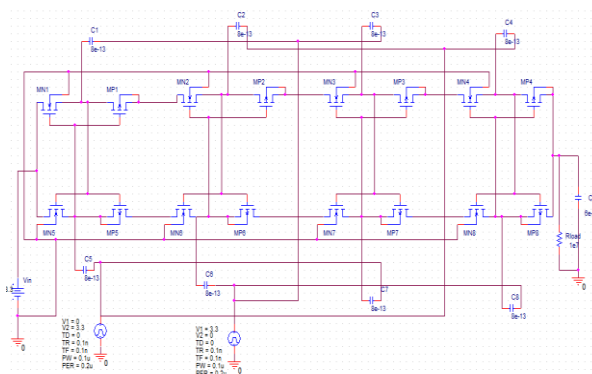

Fig 6: A Four-Stage Cross-Coupled Voltage Doubler Power Converter

6. SIMULATION RESULTS

The three topologies are designed in Orcad 16.5 software using 0.18μm level 3 CMOS process parameters. All the simulations are carried out at 10MHz frequency with clock voltage equal to *Vin*=3.3V. The values of boosting capacitors for each stage and each topology are same and equal to 0.8pF. The number of pumping stages is N=4 with the output capacitor value 0.6pF.

The output voltage waveforms for Basic, Modified Dickson and Cross-Coupled Voltage Doubler designs are shown in figures 7, 8 and 9. Amplitude of non-overlapping clocks are same for all the circuits as seen in figure and output voltage for Basic Dickson is 12V, Modified Dickson is 13.763Vand Cross-Coupled Voltage Doubler is15.457V. The comparison of maximum output voltages for all three topologies are shown in fig 10. It is seen that Cross-Coupled Voltage Doubler gives the higher output voltage for the same number of stages. The variation of supply voltage versus output voltage graph is shown in fig 11. From the result it is observed that at every input supply voltage Cross-Coupled Voltage Doubler gives highest output voltage. The graph between frequency and power efficiency is shown in fig 12. It is observed that power efficiency increased first then it is almost constant with increasing frequency for all the three topologies. The graph between boosting capacitor and output voltage is shown in fig 13. It is seen that as value of boosting capacitor increase output voltage enhances. In this graph conventional DCP gives poor performance and Cross-Coupled Voltage Doubler has better performance. Cross-Coupled Voltage Doubler gives high value of output voltage when all the three topologies are compared for same number of stages and values of input voltage, clock frequency, boosting capacitor values are same. The graph of time versus output voltage is shown in fig 14 for all the three topologies. It is seen that after some time the graph becomes steady for all three topologies and Cross-Coupled Voltage Doubler gives the higher output.
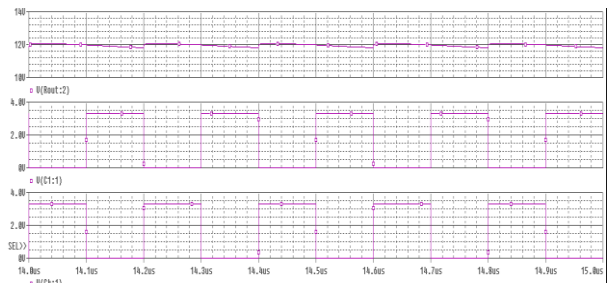

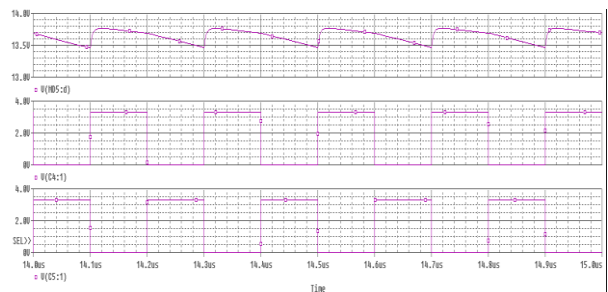**Fig 7: Output Voltage Waveform of Four-Stage Conventional Dickson Power Converter**

Fig 8: Output Voltage Waveform of Four-Stage Modified Dickson Power Converter
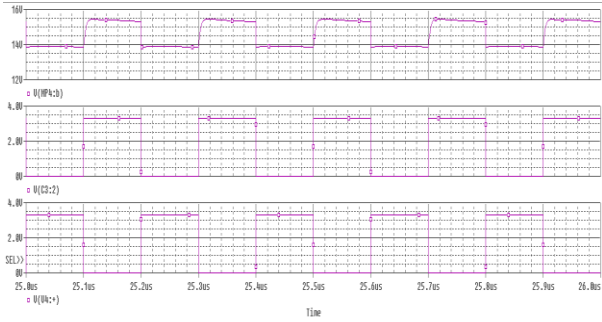
Fig 9: Output Voltage Waveform of Four-Stage Cross-Coupled Voltage Doubler Power Converter
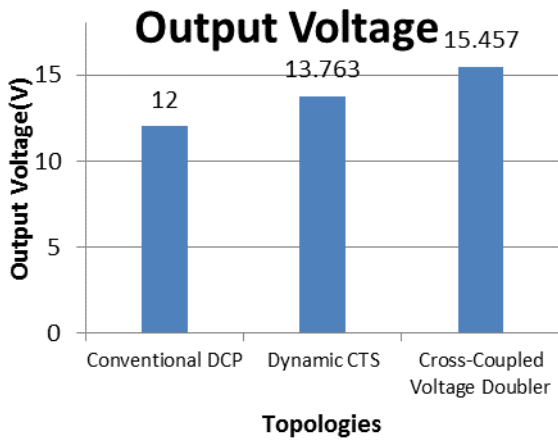

Fig 10: Comparison of Maximum Output Voltages for different Topologies at N=4
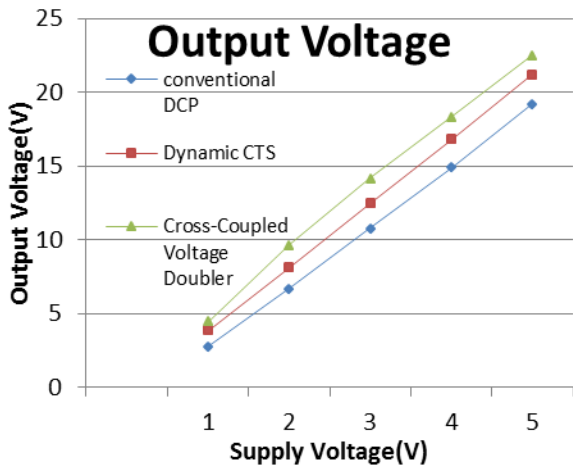

Fig 11: Variation of Output Voltage for different Supply Voltages at N=4

Output results of the three topologies are compared in Table 1. Cross-Coupled Voltage Doubler gives highest value of output voltage and power efficiency for the same values of input supply, boosting capacitance, output capacitance and clock frequency for all the three topologies.
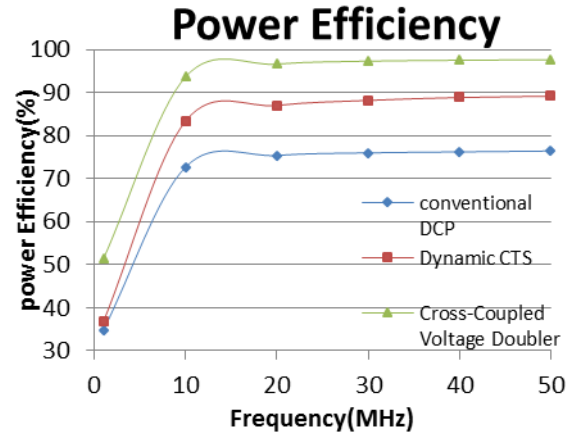

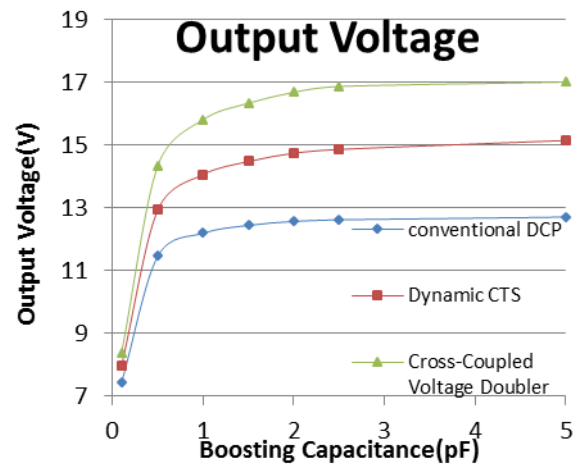**Fig 12: Variation of Power Efficiency for different Frequency**

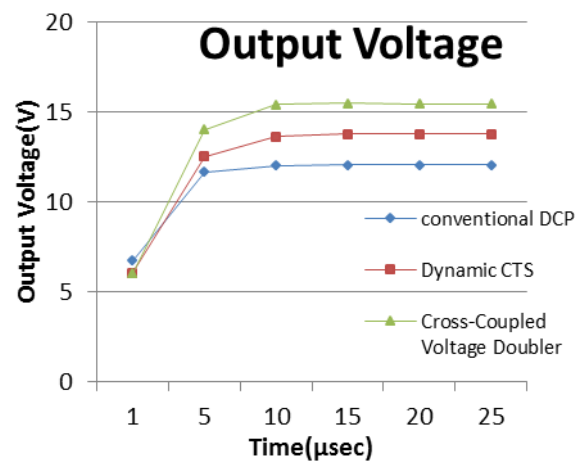**Fig 13: Variation of Output Voltage at different Boosting Capacitor Values at N=4**

Fig 14: Comparison of Output Voltage for different Topologies for N=4

Table 1: Simulation Results

	Fig.1	Fig.2	Fig.3
Input Supply	3.3V		
Value of Boosting Capacitor	0.8μF		
Clock Frequency	10MHZ		
Output voltage	12	13.763	15.457
Power Efficiency	72.73%	83.41%	93.68%

7. CONCLUSION

Energy harvesting from non-traditional energy sources is increasing day by day in applications like embedded systems, RFID tags, wireless sensor nodes, health monitoring systems etc. and the most important circuit in energy harvesting system is power converter and therefore automation for its design is very crucial.

This paper presented a novel method to design power converter, which uses co-simulation of PSpice and MATLAB using SLPS interface. Thus, the evaluation of all the design and performance parameters of power converter is possible before the actual fabrication of chip. This methodology makes possible to simulate a device level model i.e. PSpice model in MATLAB. Thus, the system becomes platform independent and automatic. Basic Dickson, Modified Dickson and Cross-Coupled Voltage Doubler are designed using the above methodology. It is observed that cross-coupled topology is more suitable for energy harvesting systems because it produces higher output voltage and power efficiency compared to other circuits for the same number of stages.

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