Low Power Error Detector Design by using Low Power Flip Flops Logic

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Abstract
Low-power design is becoming a crucial design objective for the chip design engineer due to the growing demand on portable application and the increasing difficulties in cooling and heat removal. In the integrated circuits power consumption is one of the challenges like area and speed .In this paper a novel technique is proposed to design an error detector for the lower power consumption. Here the work has done by using two low power flip flops (1)have considered SVL5T TSPC FF method and(2) low power DFF . In the proposed system reduction of power is about 50 % - 70%.Some of the low power flip flop is also used in multimedia and phase detector application.

Keywords
Flip Flop, low power logic, TSPC, double edge triggering, SVL, Error detector.

1. INTRODUCTION
In current scenario the requirement of portable equipment is increasing rapidly like Pocket calculators, Hearing aids, Wristwatches etc. Portability is achieved by System-on-chip designs (SoC), which hold multiple functions "systems" on a single silicon chip like processor, bus and otherelements on a single monolithic substrate. Next approach for portability is battery. For someapplications, heavy battery pack up is not possible in practice and frequent recharge is inconvenient.Aggressive design rules will increase circuit density, and improve overall chip performance. If design rules are too aggressive then complexity arises in manufacturing. On the other hand, slack design rules may result in increased die size, delays, and lower chip performance. If density of chip goes on increasing means heat will be dissipated due to the high powerconsumption. Some cooling systems like heat sinks, refrigeration cooling systems, and water cooled heat exchanger are used to reduce the heat. It has limited ability to remove the excess heat. The requirement of sophisticated cooling systems and high cost battery is reduced linearly, if we are reducing the interior power in integrated chip. From the high performance microprocessor design, clocking systems consumed 40% of the chip power; thermal management was a major concern Low power flip flop design will play a vital role in high performance system design. There is a wide variety of low power flip flops are available in the literature [2] – [7]. For example HLFF [2], SDFF [3] called as fastest flip flop but they are consuming large amount of power due to redundant switching activity in the internal nodes. Low swing clock double edge trigger flip flop (LSDFF [4]), using low swing voltage and double edge triggering method to reduce the power consumption. Clock gating techniques also used to reduce the flip flop power by disable the clock signal when particular block is idle condition[5].This paper organized as follows: Section II deals with power reduction techniques for existing flipflops. Section III presents existing flip flops. In Section IV, application of proposed flip flops is explained and Section V shows the simulation results. Section VI concludes this paper. Finally Section VII gives the future work.

2. LOW POWER FLIP FLOP DESIGN SURVEY
There are three source of power dissipation in digital complementary metal-oxide-semiconductor (CMOS) circuit.That is static power dissipation, dynamic power dissipation and short circuit power dissipation. Dynamic and short circuit power dissipation fall under the category of Transient Power Dissipation. Static power dissipation is due to leakage currents.

$$P=P_{dynamic} + P_{short\ circuit} + P_{leakage} \quad \text{eq(1)}$$

Dynamic Power is also called as switching Power. It is caused by continuous charging anddischarging of output parasitic capacitance. Short circuit power is the result when pull up and pull down network will conduct simultaneously. Leakage power dissipation arises when current flow takes place from supply to ground in idle condition. Power consumption is directly proportional to supply voltage, frequency and capacitance.

2.1. Low Power flip flop design Techniques
There are many low power techniques available to reduce the flip flop power like Low swing Voltage[4], Conditional operation [6], Double Edge triggering [7][8], Clock gating[5], Dual Vt / MTCMOS [9], Proposed Pulsed flip flop [17] and Reducing the capacity of clock load[10] etc. Inthis paper the SVL [11] methods is used to reduce the total power consumption of error detector because, it can reduce the leakage power.

2.1.1. Removal of Noise coupling Transistors
Sometimes, the flip flop will take wrong initial conditions due to noise coupling output, then false Output is the result with more glitches.To avoid those draw backs we can eliminate the noise coupling transistors in the output as well as the input.

2.1.2. Double Edge Triggering
Most of the flip flops are designed to operate in single clock edge i.e. either in positive edge ornegative edge. In double edge triggering [8] the flip flop is made to operate in both clock edges. With this method the opposite clock edge will not be wasted and speed of operation is increased.

2.1.3. Self Controllable Voltage Level Circuit
This SVL [11] method is implemented in memory circuits in prior papers to reduce the power consumption. In this paper the same SVL approach is applied to the error detector to reduce the leakage current and power which leads to total power reduction. Two blocks, Upper SVL and Lower SVL circuit will give the

maximum Vdd and minimum ground level to the flip flop(load) when active mode. In other hand it will give lower Vdd and higher ground level to the load in standby mode .The following sections will describe about existing flip flops and its application in the error detector circuit design in detail.

3. EXISTING FLIP FLOPS

3.1 5Transistors True single Phase Clocked Flip flop

The schematic of 5T-TSPC flip-flop is shown in figure 1. It consists of 3-NMOS and 2-PMOStransistor [13]. It is positive edge triggered D latch. When *clk=1*, *D=1*, then M2=M3=M4=ON andM1=M5=OFF, output becomes high [13]. The drawback of this flip flop is high leakage power in lower technology. The leakage power increases as technology is scaled down.

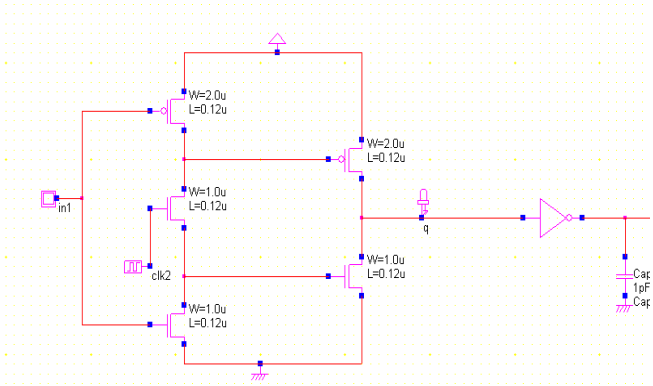


Fig 1: Schematic of 5 transistors TSPC FF

This leakage power is reduced by using best technique among all run time techniques. The newly developed leakage current reduction circuit called a "Self-controllable Voltage Level (SVL) [11]".circuit is implemented in proposed flip flop in order to reduce the leakage power. Formerly this SVL circuit is used for reducing the power in memory cell like SRAM. Now it can be applicable for flip-flops. Double edge triggering method also implemented to proposed flip flop.

3.2 Double Edge Triggered 5TTSPC Flip flop

This is the third proposed flip flop. The same double edge triggering [8] scheme is applied to the flip flop discussed in the Section 3.2. Then named as, **double edge triggered five** transistor true single phase clocked flip flop (DET-5TTSPC Flip Flop) the schematic as shown in figure 2. We can make the 5T-TSPC flip flop to operate in both the edge of the clock. The node X and Y act as a capacitor .When pulse=1 (N1 is ON) and d=0 (P1 is ON and N2 is OFF) the node Y is charged to Vddthrough P1 and N1 which is ON, q=0 in pre-charge phase.

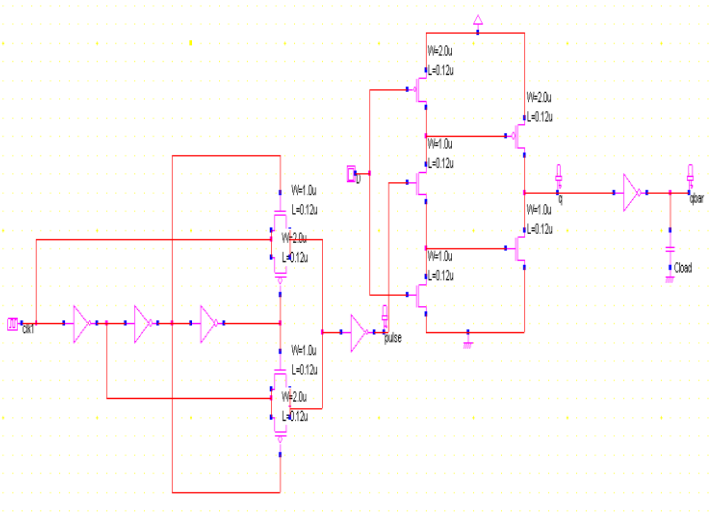


Fig 2: Schematic of DET TSPC FF

When pulse=d=1(N1 and N2 is ON), the node X is discharged to GND (P1 is OFF and P2 is ON), then q=1 in evaluation phase. This flip flop also a less power consumption than the other double edge triggering flip flop.

3.3 SVL-5TTSPC Flip Flop

In section 3.2 we discussed about the drawback of 5TTSPCFF like high leakage power in lowertechnology due to high leakage current.

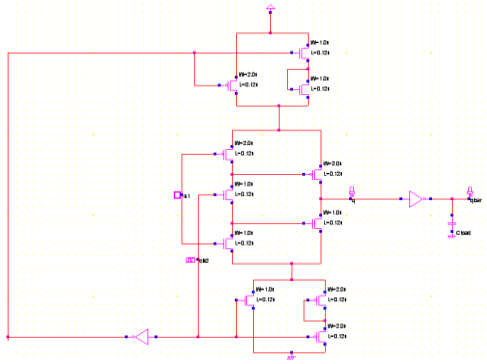


Fig 3: Schematic of SVL 5T TSPC FF

In order to avoid that we can incorporate the leakage reduction circuit called "Self-ControllableVoltage Level Circuit"[11] to this flip flop to reduce the power consumption. The block diagram of SVL-5TTSPC flip flop is shown in figure 3. The two circuits called upper SVL (U-SVL) and Lower SVL (L-SVL) is used to construct the above fourth proposed flip flop. Upper SVL consists of one PMOS (pSW) act as a switch and multiple NMOS (nRSm) act as resistors connected in series. Similarly, Lower SVL constructed by one NMOS (n SW) and multiple PMOS (p RSm) in series.

3.4 MODIFIED DFF:

By using the Pass Transistor Logic family idea this circuit has designed as well as by using only one clocking transistor so it will be consuming only less power in the clock network of the Flip flop when compared to all other circuits [19]. Here number of transistor is 6 excluding the not gates al. due to this less number of transistors the power consumption also less as compared to other designed flip flop.

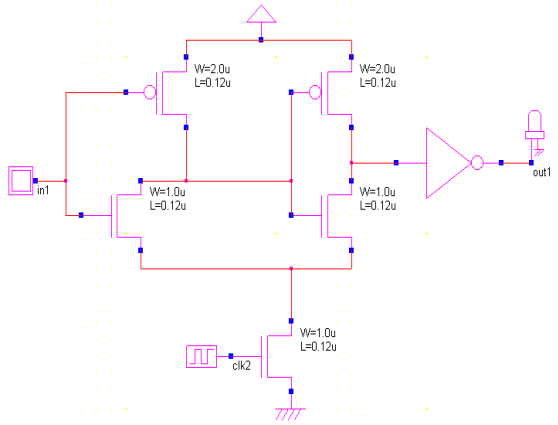


Fig 4: Schematic of low power D FF.

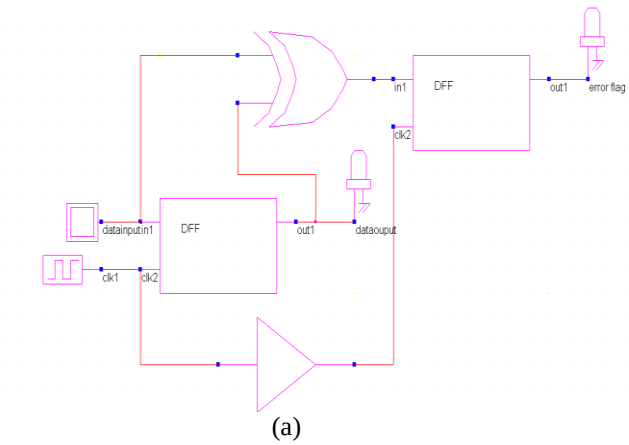
At the same time due to the reduced no of transistor count we can reduce the delay oriented things also. Thus we are reducing the overall switching delay and power, area consumption. So this circuit will be acting as good sequential elements when compared to other flip-flop design.

4. LOW POWER FLIP FLOP APPLICATIONS

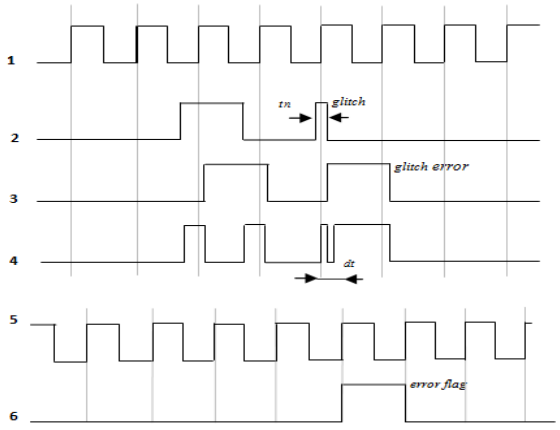
Portable multimedia and communication devices have experienced explosive growth recently. Longerbattery life is one of the crucial factors in the widespread success of these products. As such, low power circuit design for low power application has become very important [15]. The above low powerproposed flip flops are useful in the area of multimedia and wireless communication applications and also applicable in counters, shift register, Error detector and phase detector.

4.1 Error Detector [18]

Integrated circuit operating frequency and density increases due to deep submicron technology. Single chip containing many complex functional blocks with interconnects and buses. As complexity of circuit increases noise effect also increases like capacitive or inductive cross talk, transmission line effect etc. One of the common approaches to reduce the noise hazard is to bound the noise .Some deterministic method like BIST will generate the test pattern and detect the faults due to noise. Another approach is to detect the noise is on-line testing method. It will test the functional block during operation time. It has many advantages over deterministic methods. This method is highly reliable, increased system performance and high degree of noise tolerance. Double Sampling Data Checking Technique is the one of the on-line testing method [16].



(a)



(b)

Fig 5: (a) Schematic of existing Error Detector and (b) timing diagram

The principle behind this method is input data is sampled by two flip flops at a time interval *dt*andconsistency is checked from the two latched data's with each other. Consider the noise interval *tn* is less than *dt*. One of the flip flop will catches the error and sends the error signal, and then rest of theclock cycle will indicate error (i.e. difference) is occurred by comparing the two flip flops. The blockdiagram of error detector and its timing diagram is illustrated in figure 5. [16]. in wave form no.2 the first two transitions, from 0→1 and 1→0 there is no error flag is set in the wave no.6, due to validtransition. After some time the first flip flop acquire the glitch at interval *tn*. The output of first flop is glitch error output in the wave no.3. To detect the error properly, the buffer time of on-line errordetector should be set suitably. d*t*must be longer than the noise active region so that the second flipflop FF1 can catch the difference between outputs of FF1 and FF2 correctly. The *dt* must satisfy the following constraint [16].

$$Max\,(t_{DFF}\ , t_n)\ t_{ox} + t_{setup} < dt < t_{pd} + t_{xor} + t_{setup} - t_{ske}$$

Where, t_{DFF} and t_{xor} are the FF1 and the XOR propagation time respectively. t_n is the noise active duration. t_{setup} and t_{ske} is the FF2 set up time and worst case clock skew respectively. t_{pd} is the incoming signal minimal path delay.

4.2. PROPOSED LOW POWER ERROR DETECTOR:

In this proposed error detector, the conventional D-flip flop is replaced by low power modified low power flip flop and SVL5TTSPC flip flop discuss in section 3.3 and 3.4.

4.2.1. ErrorDetector by using modified DFF:

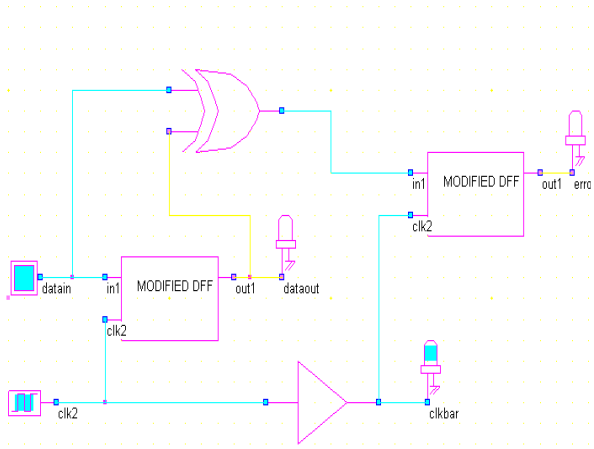


Fig 6: Schematic of proposed Error Detector by using modified DFF.

In this proposed error detector, the conventional D-flip flop is replaced by low power dff as discussed in section 3.4. Working principle of detector is same as the existing one. The difference between existing and proposed error detector is it will consume less power than existing one. The simulation results of proposed error detector are given in next section.

4.3.2 Error Detector by using SVL TSPCFF:

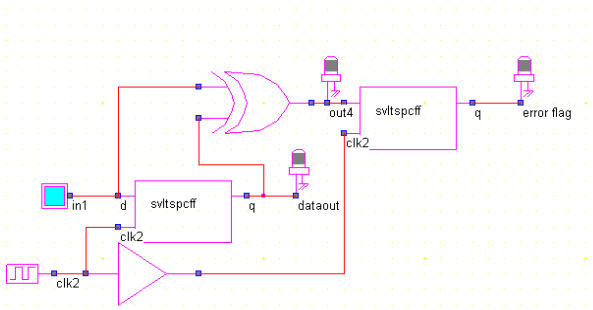


Fig 7: Schematic of proposed Error Detector by using SVL5TTSPCFF.

In this proposed error detector, the conventional D-flip flop is replaced by low power SVLTSPCFF discuss in section 3.3. Working principle of detector is same as the existing one. The difference between existing and proposed error detector is later will consume less power than existing one. The simulation results of proposed error detector will discussed in next section.

5. SIMULATION RESULTS

5.1Modified error detector outputs

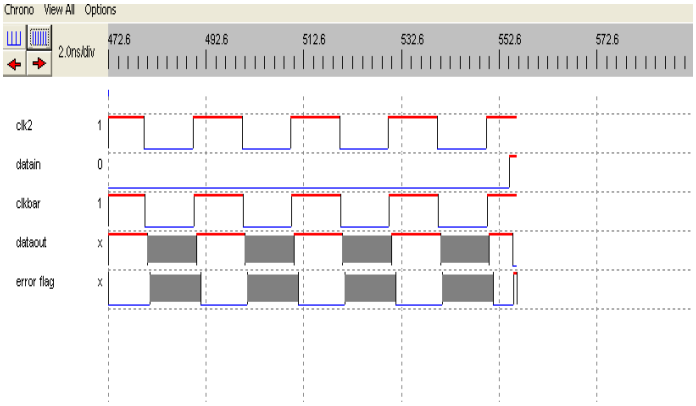
The simulation results were obtained from MICROWIND3.1 in 0.12µm CMOS process at roomtemperature VDD is 1V. All existing and proposed flip flops were simulated with output load capacitance *Cloadb* and layout level. The clock frequency for single triggering and double edgetriggering flip flop is 1GHz and 0.5GHz respectively. Following flipflops metrics are carried out tocompare the performance of the existing and simulated error detectors.

***Total no of Transistors*:** The total number of transistors is measured which contribute more area and power consumption in the integrated circuit design.

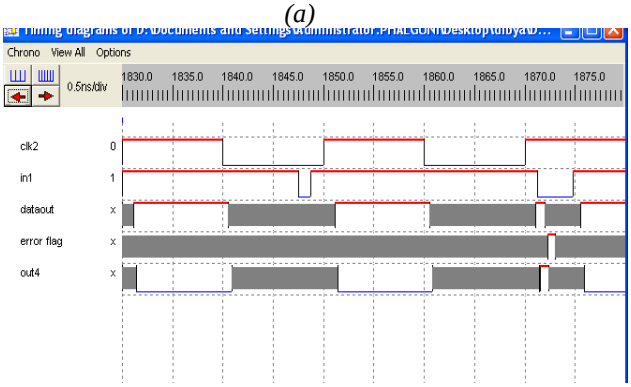
Number of clocked Transistor: Clocked transistors will contribute more power consumption due to high switching activity.

Delay: Delay is data to output delay (D-to-Q delay) which is sum of the *Set up time* and *clock tooutput (Q) delay*. Set up time is minimum time needed between the D input signal change and the triggering lock signal edge on the clock input. This metric guarantees that the output will follow the input in worst case conditions of process, voltage and temperature (PVT). The D-to-Q delay is obtained by sweeping 0_1 and 1_0 data transition times with respect to the clock edge and the minimum data-to-output delay corresponding to optimum set up time is recorded. The output is considered as Qb. Since, the load capacitor is connected to Qb output. The unit is *ps (Pico second).*

Power: It is the total power consumption of flip flop in terms of *µW (micro watt) and mW.*



(a)



(b)

Fig 8:Output of proposed low power error detector (a) by using modified dff, (b) by using SVL5TTSPCFF).

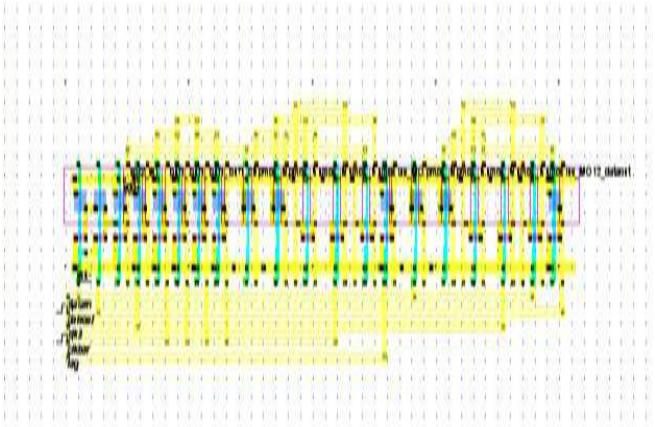


Fig 9: Error detector layout (by using modified dff)

6. CONCLUSIONS:

In this Paper Error Detector has designed based on Low Power DFF and SVLTSPCFF technique**.** The 1ST Proposed error detector design based on low power dff shows 55% power improvement than the existing error detector and it shows a reduction in area by 50%. Thus our proposed system is having very less power and area constraints as well as it is having a very low power clocking system which will lead to improvement in the case of implementation in future technology. The 2nd proposed system shows 67% power improvement as compared to the existing error detector but area is almost same as the existing technique. Error detector design using SVLTSPCFF gives low leakage power by providing a regulated dc voltage to the load circuit on request . In future This Detector can be very suitable for System On Chip (SOC) applications. This can be much suitable for application of battery oriented operation for less power and area.Refer table 1.

7. FUTURE WORK

Furthermore the work can reduce the power consumption by using low swing voltage approach. If supply voltage is halved, the switching activity of the transistor will be reduced which leads to power reduction. Then transistor scaling or layout optimization is another way to reduce power consumption.

TABLE 1:Comparison table for error detector:

DESIGN	*POWER*	*AREA*
Existing error detector	*131.48µw*	*427µmm^2*
Proposed error detector by using MODIFIED DFF	*58.83 µw*	*210µmm^2*
Proposed error detector by using SVLTSPCFF	*43.048µw*	*437.048µmm^2*
Improvement as compare to modified DFF	*55%*	*50%*
Improvement as compare to SVLTSPCFF	*67.4%*	----

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