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Performance Improvement of Turbo Product Code using Closed Chain Error Pattern Decoding in OFDM System

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Abstract-

The evaluation of bit error rate (BER) performance for various two dimensional turbo product codes (TPCs) is discussed. The turbo product code decoder is implemented using hard input hard output data, which is impaired by additive white Gaussian noise (AWGN).The effectiveness of the iterative TPC BER is evaluated using non sequential decoding. OFDM is a suitable candidate for high performance of wireless communication systems. OFDM transceiver will be implemented. The use of turbo product coding and power allocation in OFDM is useful to the desired performance at higher data rates. Simulation coding is done over additive white Gaussian noise (AWGN) and impulsive noise (which is produced in broadband transmission) channels. Simulation results demonstrated that, for particular codes, noticeable coding gain improvement of about 2 dB is achieved when compared to the standard sequential HIHO decoding and about 0.8 dB when compared to the non sequential HIHO decoding. The computational complexity of the CCEP decoder is substantially reduced at moderate and high signal to noise ratios by stopping the iterative process when it is not more beneficial to perform further iterations.

General Terms

Design and performance of turbo product code and closed chain error corrections decoding technique.

Keywords

CCEP, BER, eBCH, TPC, OFDM, HIHO, SISO, HDD, LBC, ISI, CSI, DPI.

1. Introduction

Turbo error correction coding is a powerful channel coding scheme used for power limited systems such as deep space wireless communications systems. Turbo codes offer a performance closer to the Shannon limit than any other class of error correcting codes [1]. Turbo product codes (TPCs) are also known as a block turbo codes, that has an excellent performance at high code rates and can provide a wide range of block sizes [2]-[3]. TPCs can be constructed using two or more simple linear codes either serially or in parallel; in order to achieve acceptable error performance with manageable encoding and decoding complexity.

To achieve the ultimate gain of TPCs, the decoder has to take soft input and produce soft output, and hence it is called soft input soft output (SISO) decoder. The soft decoding is based on the Chase II algorithm that requires a large number of hard decision decoding (HDD) operations for each row/column in the received matrix. Moreover, the Chase II algorithm produces hard data which has to be converted to soft information before it can be utilized by the soft input decoder in the subsequent iterations. The large number of HDD performed by the Chase II algorithm and the hard to soft data conversion considerably increases the decoder computational complexity and delay. Furthermore, the computation of the log-likelihood ratios (LLRs) of the received bits, requires accurate knowledge of the channel state information (CSI). In the absence of LLR knowledge, the coding gain promised by SISO TPCs will not be attained. Consequently, hard input hard output (HIHO) decoders have been proposed for applications where low complexity and short delay are required[4]-[5].which reduces the number of required SISO iterations by replacing part of the SISO iterations with a number of hard input hard-output (HIHO) iterations. This method has reduced the overall number of HDD operations by 20% and the number of arithmetic operations by 35%.

In particular applications that require precise soft information are not available viz. as data storage systems, Pyndiah and Adde [6] demonstrated that SISO decoders still can be used with a coding gain penalty of 2 to 3 dB. However the penalty is reduced to about 1 dB for high code rates TPCs. The main limitation of this approach, it is more suitable for high code rates and has the same complexity as the standard SISO decoders. A similar scenario is observed in optical channels where the computation of the log-likelihood ratio based on the Gaussian approximation leads to significant loss. Consequently, simpler decoding techniques for TPCs based on HIHO decoders have been proposed [4], [7]. HIHO decoding requires only one HDD operation for each row/column every half iteration and does not require any arithmetic operation. Hence it is substantially simple in design compared to SISO decoders. However, SISO decoders offer more than 3 dB coding gain as advantage over HIHO decoders [4], [8]. Thus, HIHO decoders have low complexity than SISO decoders and the difference in coding gain is tolerable in practical environments [4], [9].

A major drawback of HIHO decoders is their vulnerability to closed-chains error patterns (CCEP) [9]. Although such patterns consist of a small number of bit errors, the HIHO decoders fail to correct them because the number of bit errors in any direction is greater than the component code correction capability. The problem of CCEP is more apparent in [8] because a non-converging decoding process usually ends with a CCEP. In this, a new technique is proposed to correct CCEP by first locating the bit errors that form the CCEP, then using erasure decoding to correct them. This approach simply doubles the component codes correction capability. This is due to the fact that number of erasures that a linear block code (LBC) can correct might be as much as twice the number of errors. Extensive simulation results have confirmed that a noticeable coding gain improvement is achieved using the new decoding algorithm whereas the additional complexity is negligible at low channel error probability.

This paper is organized as follows. In Section 2, the basic principles of iterative TPCs are briefly introduced. Section 3 used OFDM system. Section 4 describes the decoding algorithm in details. Section 5 demonstrates the numerical results of a non sequential decoding algorithm and its performance compared to standard HIHO TPC over AWGN channels. Section 6 provides the conclusion.

2. TURBO PRODUCT CODES

TPCs are multidimensional arrays constructed from two or more linear block codes denoted as the component codes. Two dimensional TPCs are the most common among other TPCs where the product code is obtained using two systematic linear block codes min are the codeword size, number of information bits and minimum Hamming distance, respectively. As depicted in Figure 1, the TPC is constructed as follows: a two-dimensional product code is built from two component codes with parameters C 1 (n 1, k1, d1) and C2 (n2, k2, d2), where ni, ki, di indicate code word length, number of information bits, and minimum hamming distance respectively [3].The product code P = C1 x C2 is obtained by placing (K1 x K2) information bits in an array of K1 rows and K2 columns. The parameters of product code P are n =n1 X n2, K=K1 x K2, d=d1 x d2 and code rate is R = R1x R2, where Ri is the code rate of Ci, Thus long block codes are built with large minimum Hamming distance. Figure 1 shows the procedure for construction of a 2D product code using two block codes C1 and C2. The rows of matrix P are the code words of C1. The columns of matrix P are code words of C2 [3].

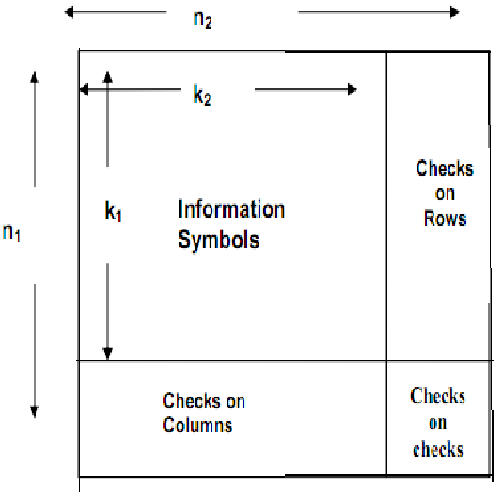

Figure 1: An example of a 2D product code constructed using two component codes

3. Block turbo coded OFDM system using channel

The transmitter configuration for the block turbo coded OFDM system is shown in Figure 2

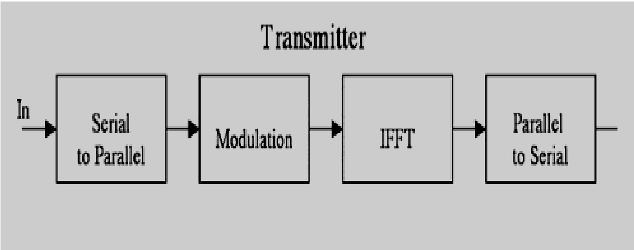

Figure 2: Transmitter configuration for the block turbo coded OFDM system

The block turbo code encoding, comprises of total K x K information bits that are placed into a k x k array. The a single parity check code is applied to every row of the array to result in a k x n matrix and subsequently the same code is applied to each column of the resultant matrix to yield an n x n matrix. The block turbo coded bits are mapped into complex numbers representing QPSK, 16-QAM and 64-QAM constellation points. The stream of complex valued sub-carrier modulation symbols at the output of the mapper is divided into groups of 48 complex numbers. Each group is transmitted in an OFDM symbol with 4 pilot carriers added. Thus, each symbol is constituted by a set of 52 carriers. 12 pilot carriers that are padded with zeros to make the number of subcarriers per symbol a power of 2 and applied to a 64- point IFFT which performs the OFDM modulation. The guard interval is inserted at the transition between successive symbols to absorb the intersymbol interference (ISI) created by multipath in the channel.

Figure 3 depicts the receiver configuration for block turbo coded OFDM system. The assumption is that the OFDM symbol synchronization is accomplished, the symbol cyclic prefix or guard interval are then removed and the useful portions of the OFDM data symbols are fed into a 64-point FFT which performs the OFDM demodulation.

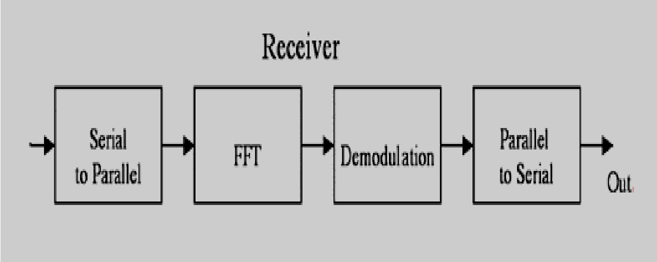

Figure 3: Receiver configurations for the Block turbo code OFDM system

The symbols at the output of FFT are used in channel estimation block. The channel estimation block estimates the channel impulse response by comparing the received training symbols with the known training symbols. The equalization block corrects the channel distortion by dividing the data carriers using estimated channel response determined in the channel estimation block. The equalized symbols are fed into a soft decision calculation block, which pass the soft input values to the iterative decoding block for turbo product code.

The conventional receiver operations, when the received soft input [R] enters into soft-in-soft-out (SISO) decoder for block turbo codes, the first thing that the decoder has to do is to search p least reliable position which is distorted severely by the channel. Based upon how accurately we find the p least reliable position, the error correction capability of the block turbo code will be varied. For conventional receiver operation the received symbols went through the equalization block where compensates for the distortion created by multipath in the channel. Due to such compensation being done by equalizer, it might cause the decoder not to find weak points, which can lead to lower the error correction capability of the block turbo code. Since it is considering coherent demodulation and not the system without having channel estimation equalization blocks. As a method of finding the parts distorted by the channel as weak points, it is come up with the scheme applying channel state information (CSI) to the soft input value so that the modified soft input at the input of the iterative decoder can be defined as

$$\mathbf{R'=CSI\,.\,R} \qquad (1)$$

Replace R in R', all equations are held in themselves. particularly, equation is written like this

$$r_j' = \frac{|CSI.R - c^{c}|{}^\wedge 2 - |CSI.R - c^{d}|{}^\wedge 2}{4}\, c_j^{d} \qquad (2)$$

4. The Decoding Algorithm

The proposed technique is based on estimating error locations before correcting them. The main advantage of this approach is to identify the error locations by doubling the number of errors that can be corrected by the component codes. It is noted from the example in Figure 4 that using standard iterative row/column decoding for an **H** with 4 errors makes things worse by introducing additional 12 errors [9].

0	0	2	0	2	0	0	0		
S	*S*	*F*	*S*	*F*	*S*	*S*	*S*		
								S	0
								S	0
		x		x				*F*	2
								S	0
		x		x				*F*	2
								S	0
								S	0
								S	0

Figure 4: closed chain error pattern identification example

Applying the technique of to decode **H** with any threshold value less than *t+1* will not suffice as in the standard decoding approach. However, it will not provide any improvement. The new procedure is summarized as follows [8]:

1) Apply the non-sequential decoding algorithm for i iterations.
2) Apply j iterations as follows:

a) Set the iterations counter $v = 1$.

b) Decoder all row in h and record $\hat{\imath}$ and I for each row. If $\hat{\imath} > t$, set I = F and $\hat{C}(v) = \hat{C}(v-1)$. The value of $\hat{\imath}$ can be computed as $\hat{\imath} = d(\hat{C}(v),\hat{C}(v-1))$.

c) Decode all columns in H and record $\hat{\imath}$ and I for each column. If $\hat{\imath} > t$ set I= F and $\hat{C}(v) = \hat{C}(v-1)$.

d) If $\sum_{i=1}^{n1+n2} \hat{\imath} = 0$ and I = S for all rows/columns, stop decoding, else go to (e).

e) Erase all the bits at the intersections of the all rows and columns where I = F.

f) Use Erasure decoding to decode any row with an erased bit.

g) If v = j, stop decoding, else go to (b).

An example of applying these techniques is shown in Figure 4 where the error pattern consists of a closed-chain of four bits, the erroneous bits are shaded. The results of applying the procedure given above is shown in Figure 4 as well where the erased bits are labeled with an X. Obviously, the erasure decoding will provide the correct results since $\alpha = 3$ for the BCH code.
This technique is based on assigning a reliability factor for each row or column that will be decoded. The threshold is related to the estimated number of errors in the received sequence. If any row or column has a reliability factor less than the threshold, the decoder does not decode that row/column. The main limitation of this system is that the decoder cannot correct CCEP if the number of errors in any row or column is larger than $t^{(i)}$ as depicted in Figure 4.

Another important feature of the proposed system that is used to stop the iterative decoding. Once all $\hat{\imath}$ values are equal to zero and there are no rows or columns with a decoding process indicator (DPI) value of F, then **Ĉ** is a valid codeword of C, thus performing more iterations is pointless.

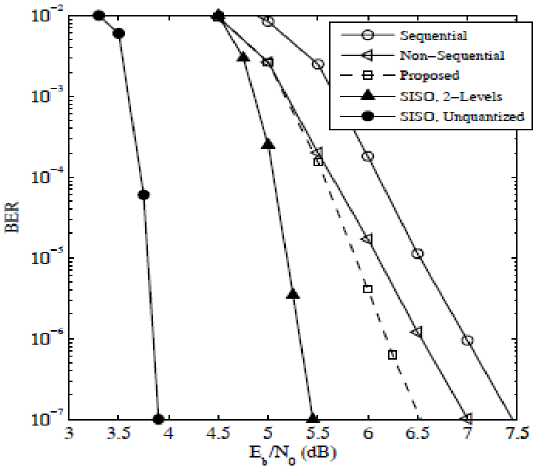

Figure 5: BER of the eBCH(128, 120, 4)2 over AWGN channels using different iterative decoding techniques.

TPC code (Hamming code as constituent code) with number of iteration has been tested in an AWGN channel.

The iterative decoding of product codes is also known as block turbo code(BTC)because the concept is quite similar to turbo codes based on iterative decoding of concatenated recursive convolutional code.

TPC (eBCH) (127,120,1) with code rate of 0.87 and 3rd iteration in a AWGN channel provides a BER of 10^{-7} at an Eb/No.

5. BER performance of Turbo Product Code under AWGN channel

The BER performance of turbo product code under AWGN channel for different iterations. From the result obtained it is observed that, with increase in the number of iteration, increases BER performance improving using chase algorithm. In closed chain error pattern algorithm using single iteration it will decodes all rows/columns, giving better BER performance.

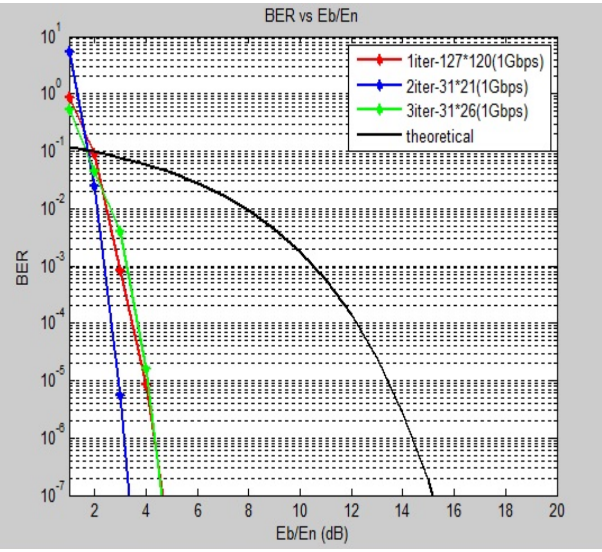

Figure 6: BER performance of block turbo coded 16 QAM-OFDM modulations

The Figure.6 shows that BER versus Eb/No over AWGN channels for the TPCs $(127, 120, 1)^2$, $(31, 26, 1)^2$ and $(31, 21, 1)^2$. Obviously, these codes have similar code sizes (4 to 1800 bytes) and different code rates that are equal to 0.87, 0.65 and 0.51, respectively. It can be noted from this Figure. 6 that the coding gain advantage of the non sequential HIHO decoder is proportional to the code rate.

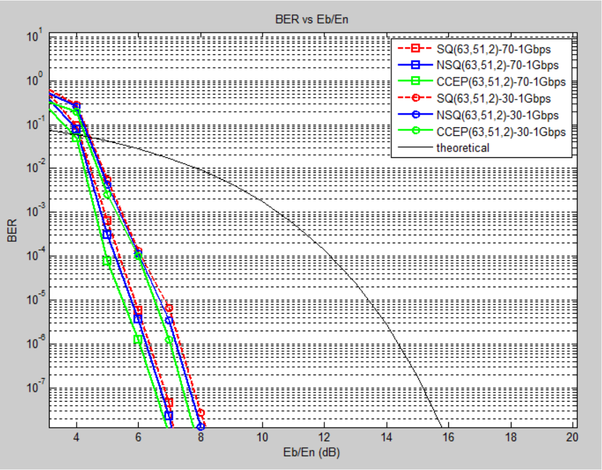

Figure 7 The BER vs Eb/No for TPCs with different code size but with the same code rates over AWGN channels.

Analysis of TPC (eBCH) is done considering parameters like BER versus E_b/N_0 ratio, characteristics of channel under consideration, noise variance of channel etc.

6. Results and Conclusion

The BER performance of various TPCs with different code sizes and code rates ~ 0.5 & 0.35 over AWGN channel is represented in Figure 7[10].The BER performance measured upto 10^{-7} for TPC under an AWGN channel is observed that data rates transmission is up to 1 Gbps for 3rd iterations. It is noted from this Figure 6 that extra coding gain offered by the non sequential is inversely proportional to the code size. After comparisons result, it is concluded that the decoding method is more useful as compared to other decoding technique. Conclude it is more efficient as compare to other algorithm; get better result and BER versus Eb/No.The effect of TPC (eBCH) channel coding method is evaluated using AWGN channel in OFDM mode. Implementing IEEE 802.16 system along with method to reduce the number of TPCs decoded in the closed chain error pattern algorithm for TPCs constructed with multi-error-correcting extended eBCH codes is expected to provide a better performance with respect to data rate, bandwidth and power gain, as compared to other available decoding techniques.

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