Improved Quality-Factor of 0.18-um Active Inductor by a Current Reuse Design

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ABSTRACT
A novel active inductor approach, which can improve the quality-factor, was presented in this report. A current reuse active inductor circuit topology was proposed, which can substantially improve its equivalent inductance. This active inductor was implemented by using a 0.18- CMOS technology,which gives a maximum quality-factor of 15 with a 6.7 nH at 6GHz.The dc power consumption of this active inductor is less than 186 mW.

General Terms
Active Inductor

Keywords
Active Inductor, CMOS, Q factor

1. INTRODUCTION
Analog circuit design is a challenging field. At the same time designing an analog circuit with reduced area or smaller size is further challenging. The technology is also racing towards nm range. For the reasons maintaining cost to market ratio is a bigger challenge.

Integrated embedded passive components can save the circuit real estate and are critical for the circuit performance of RF circuit. Integrated passive components improve package and Multi-chip Module (MCM) efficiency, enhance electrical and high frequency performance by reducing the parasitic, and eliminate surface mount assembly procedure which in turn improves the yield and reliability due to the reduced solder joint failures.

At high frequencies, particularly radio frequencies (RF), inductors have higher resistance and other losses. In addition to causing power loss, in resonant circuits this can reduce the Q factor of the circuit, broadening the bandwidth. In RF inductors, which are mostly air core types, specialized construction techniques are used to minimize these losses. To reduce parasitic capacitance and proximity effect, RF coils are constructed to avoid having many turns lying close together, parallel to one another. The windings of RF coils are often limited to a single layer, and the turns are spaced apart. To reduce resistance due to skin effect, in high-power inductors such as those used in transmitters the windings are sometimes made of a metal strip or tubing which has a larger surface area, and the surface is silver-plated. An on-chip passive inductor presents major disadvantages such as large silicon area, limited inductance value and quality factor. Most of the time, the inductor will be a major factor in determining the total chip area [4] where higher inductance values imply larger area consumption. Furthermore, their values are not precise even if the technology is well-characterized [3, 5].

The increasing popularity and growth of wireless communications has inevitably boosted research in the field of radio-frequency integrated circuit (RFIC) design, especially in CMOS technology due to the shrinking of sizes and low cost availability of the process. The inductor, an essential component in RF design, finds use in many blocks such as oscillators, filters, phase shifters, low noise amplifiers, impedance matching circuitry, biasing, etc. [1–4];however their implementation still remains to be a challenging task in CMOS.

A more area-efficient alternative to realize on-chip inductors is to use active inductors. Active inductors are particularly suitable for implementing shunt peaking in current-mode logic (CML) circuits due to both the low-Q requirement and low-swing nature of such circuits. One of the most attractive features of active inductors is that, unlike their passive counterparts, both their area and resonant frequency scale with technology. Also, they can be implemented in a standard digital process, since they can be designed using only active devices. In addition, the tunable nature of active inductors allows for gain tuning over the frequency range of interest. This property can be taken advantage of in channel loss compensation and equalization. Furthermore, active inductors can be tuned to compensate for the effects of process, voltage, and temperature (PVT) variations in the circuit.

The active inductors offer much less area consumption independent of the desired inductance value, high quality factors and tunability. Although the noise
performance and dynamic range will be degraded, it can be maintained at low enough levels for many applications[6, 7].

2. THEORY
A gyrator consists of two back-to-back connected transconductors. [8] When one port of the gyrator is connected to a capacitor, as shown in Fig.1, the network is called the gyrator-C network.

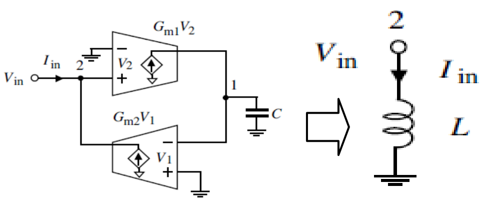

Figure 1. Lossless singel-ended gyrator-C active inductors.

A gyrator-C network is said to belossless when both the input and output impedances of the transconductors of the network are infinite and the transconductances of the transconductors are
constant. Consider the lossless gyrator-C network shown in Fig.1 The admittance looking into port 2 of the gyrator-C network is given by

$$Y = \frac{Iin}{V2} = \frac{1}{s\left(\frac{Cgs}{Gm1*Gm2}\right)} \qquad \text{-----1}$$

Eq.1 indicates that port 2 of the gyrator-C network behaves as a single-ended lossless inductor with its inductance given by,

$$L = \frac{Cgs1}{(Gm1*Gm2)} \qquad \text{------2}$$

Gyrator-C networks can therefore be used to synthesize inductors. These synthesized inductors are called gyrator-C active inductors. The inductance of gyrator-C active inductor is directly proportional to the load capacitance *C* and inversely proportional to the product of the transconductances of the transconductors of the gyrator. Also, the gyrator-C network is inductive over the entire frequency spectrum.

Although the transconductors of gyrator-C networks can be configured in various ways, the constraint that the synthesized inductors should have a large frequency range, a low level of power consumption, and a small silicon area requires that these transconductors be configured as simple as possible. Fig.2 shows the simplified schematic of the basic transconductors that are widely used in the configuration of gyrator-C active inductors.

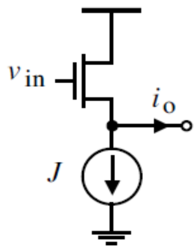

Figure 2 Simplified schematic of basic transconductors.

When either the input or the output impedances of the transconductors of gyrator-C networks are finite, the synthesized inductors are no longer lossless[9]. Also, the gyrator-C networks are inductive only in a specific frequency range.Consider the gyrator-C network shown in Fig.3 where *Go*1 and *Go*2 denote the total conductances at nodes 1 and 2, respectively. Note *Go*1 is due to the finite output impedance of transconductor 1 and the finite input impedance of transconductor 2. To simplify analysis, we continue to assume that the transconductances of the transconductors are constant.

The admittance looking into port 2 of the gyrator-C network is obtained from,

$$Y = \frac{Iin}{2}$$

$$= (s*Cgs2) + G02 + \frac{1}{s\left(\frac{Cgs1}{Gm1*Gm2}\right)} + \frac{Go1}{(Gm1*Gm2)} \qquad \text{------3}$$

Eq3 can be represented by the RLC networks shown in Fig.3.

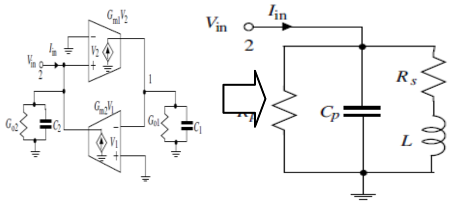

figure 3 lossy single-ended gyrator-C active inductor.

We comments on the preceding results :

- When the input and output conductances of the transconductors are considered,

the gyrator-C network behaves as a lossy inductor. *Rp* should be maximized while *Rs* should be minimized to low the ohmic loss. The finite input and output impedances of the transconductors of the gyrator-C network, however, have no effect on the inductance of the active inductor.

- The resonant frequency of the RLC network of the active inductor is given by,

$$\omega_0 = \frac{1}{\sqrt{L*cp}} = \sqrt{\frac{(Gm1*Gm2)}{(Cgs1*cgs2)}} = \sqrt{\omega t1*\omega t2} \qquad \text{----4}$$

Where ,

$$\omega t_{1,2} = \frac{Gm_{1,2}}{Cgs_{1,2}}$$

is the cut-off frequency of the transconductors. *ωo* is the self-resonant
frequency of the gyrator-C active inductor. This self-resonant frequency is typically the maximum frequency at which the active inductor operates.

- The finite input and output impedances of the transconductors constituting

active inductors result in a finite quality factor. *Q*-enhancement techniques that can offset the detrimental effect of *Rp* and *Rs* should be employed to boost the quality factor of the active inductors.

In 1988,89 a broad-band microwave active inductor has been proposed by Hara[9]. Inductances of 3.0 to 0.4nH and 7.7 to 0.9 nH are obtained at frequencies ranging up to 7.6 GHz and 5.5 GHz, respectively. This active inductor consists of a cascode FET with a feedback resistor. the two FETs are obtained with 150 um &75 um gate width. Their areas are less than 0.15 mm^2 even at high inductance value.

In 2000, a new circuit configuration of VHF CMOS transistor-only active inductor which allows very high frequency operation under low power supply voltages (<2 V) is proposed[11]. Gain enhancement techniques are applied to reduce the inductor losses achieving high-Q and wide operating bandwidth. HSPICE simulations using process parameters from a 0.35-µm CMOS technology show that the proposed floating active inductor operates under a single 1.5-V power supply voltage, exhibiting a self-resonant frequency of 2.5 GHz and a quality factor greater than 120 (phase errors <0.50) over the operating frequencies extending from 500 MHz to 1 GHz.

In 2002, a cascode-grounded active inductor circuit topology with a feedback resistance was proposed, which can substantially improve its equivalent inductance and quality-factor[12]. This feedback resistance active inductor was implemented by using a 0.18um 1P6M CMOS technology, which demonstrates a maximum quality-factor of 70 with a 5.7-nH inductance at 1.55 GHz..

3. PROPOSED ACTIVE INDUCTOR

A current reuse high-Q [12,13,14] active inductor is introduced by Wu which avoids the use of expensive external or on-chip inductors. In this work we propose an active inductor based on Wu's current reuse active inductor . The schematic of Wu's active inductor is shown below in figure 4.

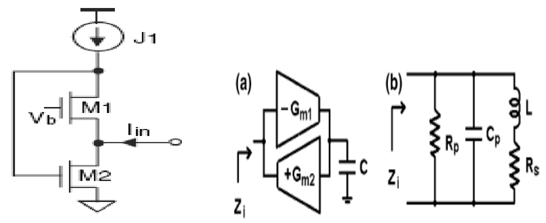

Figure 4: Wu's active inductor

It can be shown that the parameters of the RLC equivalent circuit of active inductor are given by ,

$$Rp = \frac{1}{G_{01}}$$

Cp = Cgs2

$$Rs = \frac{G_{01}}{(Gm1 * Gm2)}$$

$$L = \frac{Cgs_1}{(Gm1 * Gm2)}$$

----5

The inductance L, the parasitic series resistance Rs, and parasitic parallel resistance Rp are all functions of g_{m1} and g_{m2}, which are determined by the channel current of M1and M2. The quality factor of Wu's active inductors can be estimated by neglecting the effect of *Rs* and only focusing on *Rp* as *Rp* is small.

$$Q \approx \frac{Rp}{(\omega 0 * L)}$$

-----6

4. SIMULATION RESULTS

The active inductor circuit has been simulated in Pspice using CMOS 0.18um technology, with supply voltage of 1.8V.All NMOS have minimum channel length of 0.18 um. The width of the transistors and value of J1 the values of is chosen to ptimize the quality factor of the inductor as W1 = 50um & W2 = 40 um, Ji=400uA. The input bias voltage is varied from 0.1V to 1.8V. We get an inductive range of 6.676nH to 0.45nH at 3-9 GHz.The frequency response is as shown in fig.6.At self resonant frequency of 6GHz we get L of 6.676nH with Q factor of 15 as shown in fig.7

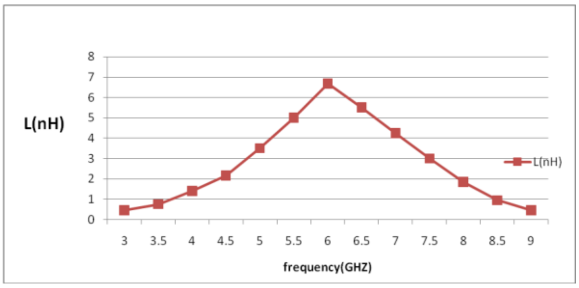

Figure 6 Inductor Vs frequency response of the active inductor

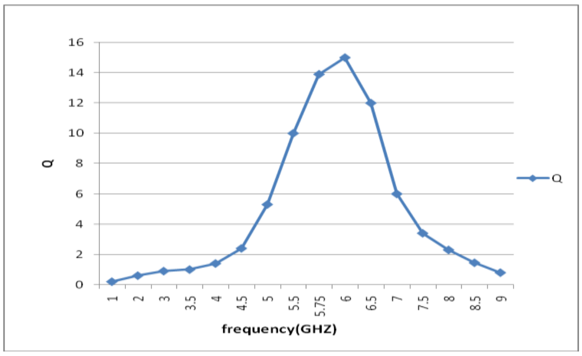

Figure 7 Q factor Vs frequency response of the active inductor

5. CONCLUSION

In order to emphasize the performance of the proposed inductor, Table 1 compares this work to previously published active inductors. Comparison of performances proves that the low voltage active inductor circuit presented has wide inductance band& reduced area.

Table 1. Comparitive analysis of previous work & proposed work

Parameter	**Ref. [9]**	**Ref. [10]**	**Ref. [11]**	**Ref. [13]**	**This work.**
Technology	0.3um	0.35-µm CMOS	0.18um 1P6M CMOS	0.35 um CMOS	0.18um CMOS
Inductive bandwidth	5.5GHz - 7.5GHz	500 MHz - 1 GHz	1.55GHz	400 MHz – 1.1 GHz.	3-9 GHz
L(nH)	3-0.4	n.a.	5.7	n.a.	6.7-0.45
Supply Voltage	5V	1.5V	2V	2.7V	1.8V
Area	0.15 mm^2	115 um^2	7.92 mm^2	150 um^2	64.8 um^2

6. ACKNOWLEDGMENTS

Our thanks to the experts who have contributed towards development of the template.

7. REFERENCES

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