

Dynamic and Static Analysis of Different Full Adder Topology at 180nm Technology Node

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Abstract

Adders are the most important components in digital design which not only perform addition operations, but also useful in calculating many other functions such as subtraction, multiplication and division. Different types of adders are frequently required in VLSI technology according to the requirement in processors to ASICs. In recent research we have found that Complementary Pass transistor Logic (CPL) is much more power-efficient than complementary CMOS. This paper describes the comparative performance of 1-bit CMOS (Complementary MOSFET) full adder, Transmission gate full adder, CPL (Complementary Pass Transistor Logic) full adder and Domino logic full adder, designed using TANNER EDA, using 180nm technology with different CMOS logic design styles. For a particular aspect ratio it is reported that different parameters like Dynamic and Static Power consumption and total propagation delay is less for Transmission gate Full adder.

Keywords

1-Bit CMOS full Adder, CPL full adder, Transmission Gate Full adder, Domino Logic Full adder, CMOS logic design styles

I. Introduction

Today the demand of low-power Very Large Scale Integration (VLSI) as well as minimum area design is increasing at very high rate. Reduction of power consumption makes a device more reliable. The need for devices that consume a minimum amount of power was a major driving force behind the development of CMOS technologies. At the circuit design level, there are many choices for power savings exists for implementing combinational circuits. This is because all the important parameters governing power dissipation—switching capacitance, transition activity, and short-circuit currents—are strongly influenced by the chosen logic style.

Depending on the application, the kind of circuit to be implemented, and the design technique used, different performance aspects become important. In the past, the parameters like high speed, small area and low cost were the major issues of concern, but due to great demand of low power devices power considerations are now gaining the attention of the community associated with VLSI design. In

recent years, the growth of fast computing devices and wireless communications systems has made power dissipation a most critical design parameter [6]. In the absence of low-power design techniques circuits generally suffer from very short battery life, while packaging and cooling them would lead to an unavoidable increase in the cost of the product. In addition, reliability is strongly affected by power consumption. High power dissipation is associated with high temperature operation, which, in turn, may tend to the failure mechanisms in the system. Two components determine the power consumption in a CMOS circuit:

1. Dynamic power consumption
2. Static power consumption

CMOS devices have very low static power consumption, which is the result of leakage current. This power consumption occurs when all inputs are held at some valid logic level and the circuit is not in charging states. But, when switching at a high frequency, dynamic power consumption can contribute significantly to overall power consumption. Charging and discharging a capacitive output load further increases this dynamic power consumption. Dynamic power dissipation occurs when the circuit is operational, while static power dissipation becomes an issue when the circuit is inactive or is in a power-down mode. There are three major sources of power dissipation in digital CMOS circuits, which are summarized in following equation:

$$P_{tot} = P_{(dynamic)} + P_{(static)} \quad (1)$$

The first term represents the switching component of power, where C_L is the load capacitance, f_{clk} is the clock frequency.

$$P_d = C_L * V_{DD}^2 * f_{clk} \quad (2)$$

Where:

P_d = transient power consumption

V_{DD} = supply voltage

The second term is due to the direct-path short circuit current, I_{sc} , which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current $I_{leakage}$ which can arise from substrate injection and sub-threshold effect is primarily determined by fabrication technology considerations. The switching power dissipation in CMOS digital integrated circuits is a strong function of the power supply voltage.

$$I_{leakage} = I_s * e^{(qV/kT-1)} \quad (3)$$

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I_s = reverse saturation current

v = diode voltage

k = Boltzmann's constant ($1.38 * 10^{-23}$ J/K)

q = electronic charge ($1.602 * 10^{-19}$ C)

T = temperature

$$P_s = V_{DD} * I_{sc}(4)$$

V_{DD} = supply voltage

I_{sc} = current into a device (sum of leakage currents)

Therefore, reduction of V_{DD} emerges as a very effective means of limiting the power consumption. However, the saving in power dissipation comes at a significant cost in terms of increased circuit delay. Since the exact analysis of propagation delay is quite complex, a simple first order derivation [7] can be used to show the relation between power supply and delay time.

$$T_d \propto C_L * V_{DD} / (K * V_{DD} - V_{TH})^\alpha \quad (5)$$

K = Transistor's aspect ratio (W/L)

V_{TH} = Transistor threshold voltage

α = Velocity saturation index which varies between 1 and 2.

Unfortunately, reducing the supply voltage reduces power, but when the supply voltage is near to threshold voltage, from equation (5), the delay increases drastically [8]. Section II, gives the four important adder architectures, designed in this paper for W/L ratio of 1.5 for NMOS and 3 for PMOS and supply voltage is 1.8V in all cases. Results of quantitative comparisons based on simulations of different adder architectures by using different logic design styles are given in section III. Some conclusions and references are finally drawn in Section IV and V, respectively.

II. Logic Design Styles

A) CMOS Full Adder

The conventional CMOS full adder has 28 transistors and is based on the regular CMOS structure. The CMOS full adder circuit is shown in Fig. 1. A 1-bit full adder has three 1-bit inputs (a , b , and c) and two 1-bit outputs (sum and $carry$). The relations between the inputs and the outputs are expressed as:

$$sum = a \oplus b \oplus c$$

$$carry = a * b + b * c + c * a$$

The CMOS structure combines PMOS pull-up and NMOS pull-down networks to produce considered outputs. In this style all transistors (either PMOS or NMOS) are arranged in completely separate branches, each may consist of several sub-branches [1]. Mutually exclusiveness of pull-up and pull-down networks is of a great concern. Advantages of the CMOS logic style are its robustness against voltage scaling and transistor sizing (high noise margins) and thus reliable operation at low voltages and arbitrary (even minimal) transistor sizes (ratio less logic) [2]. Disadvantage of complementary CMOS is the substantial number of large PMOS transistors, resulting in high input loads.

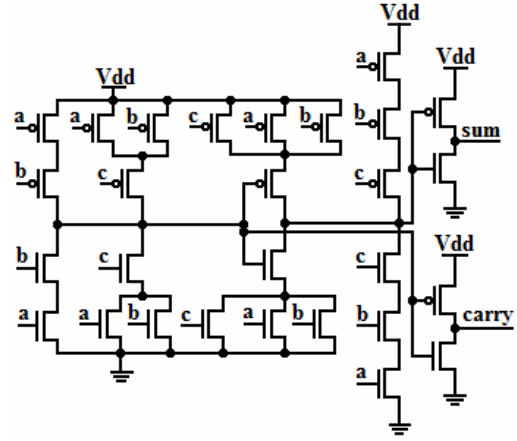


Fig. 1 CMOS Full Adder [9]

B) Complementary Pass Transistor Logic -CPL Full Adder

The complementary pass-transistor logic (CPL) full adder has 32 transistors and is based on the CPL logic. A CPL logic full adder circuit is shown in Fig. 2. In the circuit, there are two small pull-up PMOS transistors for swing restoration in the Sum output signal and the complementary Sum output signal, and another two small pull-up PMOS transistors for swing restoration in the Carry output signal and the complementary Carry output signal [2]. CPL full adder provides high-speed, full-swing operation and good driving capabilities due to the output static inverters and fast differential stage of cross coupled PMOS transistors. Due to the presence of lot of internal nodes and static inverters, there is large power dissipation [4]. The differential stage, on the other hand, leads to considerably larger short-circuit currents. Because the high voltage level of the pass-transistor outputs is lower than the supply voltage level by the threshold voltage of the pass transistors, the signals have to be amplified by using CMOS inverters at the outputs. The advantages [3], of pass logic transistors include smaller number of transistors and smaller input loads, along with MUX and especially XOR circuits being implemented efficiently. The disadvantage, of pass transistor logic is that threshold voltage drops through the NMOS transistors makes it necessary to maintain output voltage level, hence inverter is used at output which increases the number of transistors.

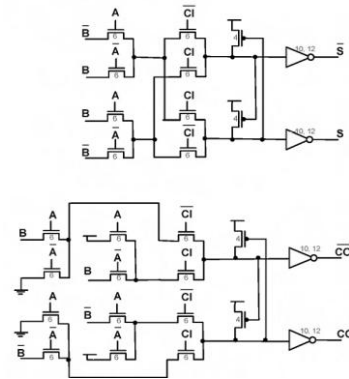


Fig. 2 CPL Full Adder [3]

C) Transmission Gate Full Adder (TGA)

The transmission-gates CMOS (TGCMOS) full adder has 20 transistors and is based on transmission gates. The transmission gate full adder circuit is shown in Fig 3. These adders are inherently low power consuming and are good for designing XOR or XNOR gates. The main disadvantage of this logic style is that they lack driving capability [4]. When TGA are cascaded, their performance degrades significantly. TG full adder produces buffered outputs of proper polarity for both sum and carry. The circuit is simpler than the conventional full adder. It uses complementary properties of NMOS and PMOS transistor. It is built by connecting a PMOS transistor and an NMOS transistor in parallel, which are controlled by complementary control signals. Both the PMOS and NMOS transistors will provide the path to the input logic “1” or “0”, respectively, when they are turned on simultaneously. Thus, there is no voltage drop problem whether the 1 or the 0 is passed through it.

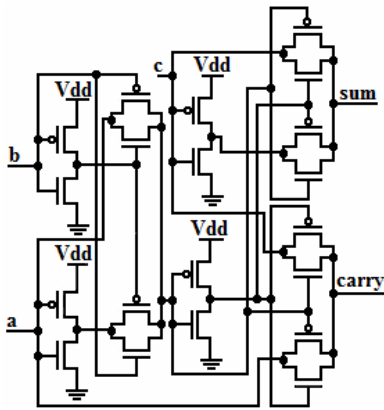


Fig. 3 Transmission Gate Full Adder [9]

D) Domino Logic Full Adder (DLA)

Domino logic is a CMOS-based evolution of the dynamic logic techniques based on either PMOS or NMOS transistors. It allows a rail-to-rail logic swing. The Dynamic Domino, circuits operate

using a sequence of pre-charge and evaluation phases orchestrated by the system clock signal as in Fig. 4. Domino gates are faster than their complementary CMOS counterparts but, on the other hand, they are more susceptible to input noise. This is due to the leakage currents flowing through the Pull down network, which can cause an unwanted discharging of the dynamic node. Dynamic domino gates have the severe limitation of not being able to implement inverting logic functions (such as NOR, NAND, XOR) and high power consumption due to clock [5]. Advantages of this type of adder are that they have smaller areas than conventional CMOS logic. This type of adders may have charge distribution problem. Operation is free of glitches as each gate can make only one transition. Only non-inverting structures are possible because of the presence of inverting buffer.

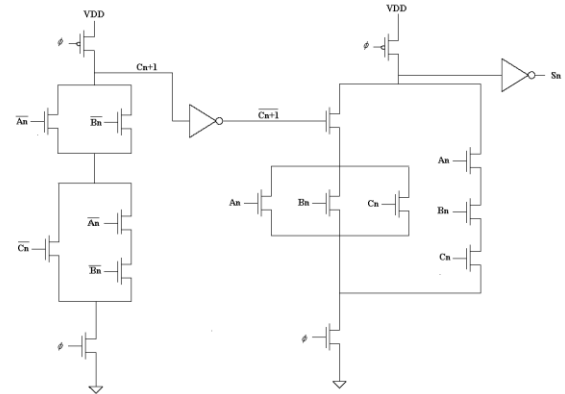


Fig. 4 Domino Logic Full Adder

III. Comparison of Various Parameters

| FULL ADDER TYPE | DYNAMIC PD (in watts) | STATIC PD (in watts) | PD SUM (in sec) | PD CARRY (in sec) |
|-----------------|-----------------------|----------------------|-----------------|-------------------|
| CMOS | 8.12E-6 | 2.00E-10 | 1.77E-10 | 1.01E-8 |
| TGA | 2.12E-6 | 1.84E-10 | 5.92E-11 | 1.01E-8 |
| CPL | 4.01E-6 | 2.54E-10 | 1.70E-10 | 1.01E-8 |
| DLA | 5.13E-6 | NA | 8.00E-11 | 3.01E-8 |

Graphical Representation of Results

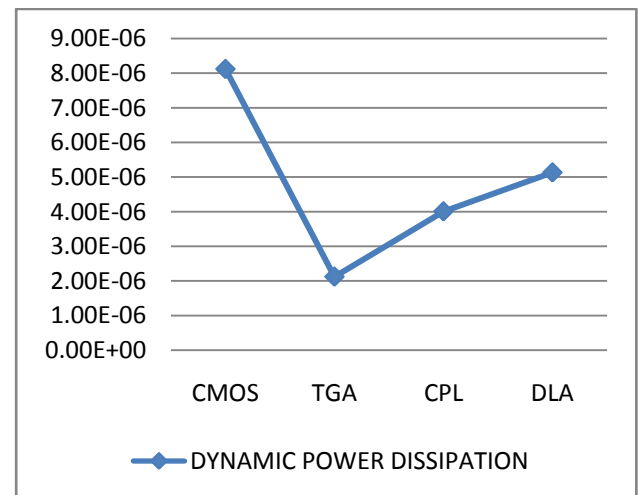


Fig. (a) Dynamic Power Dissipation

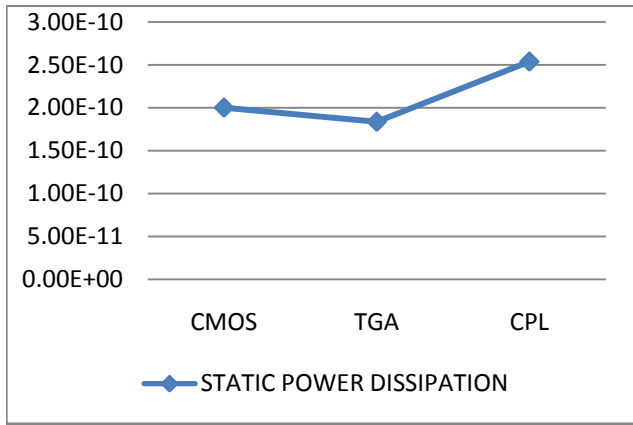


Fig. (b) Static Power Dissipation

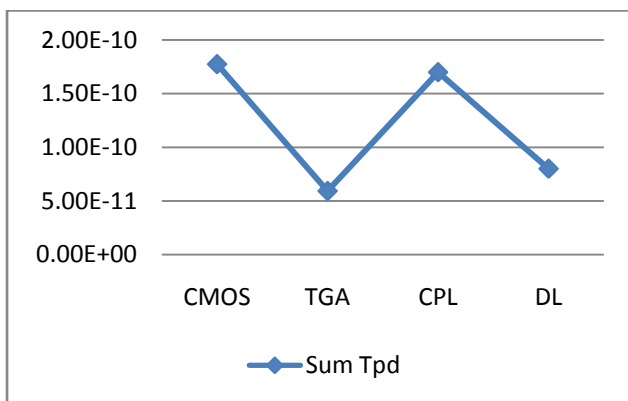


Fig. (c) Sum Propagation Delay

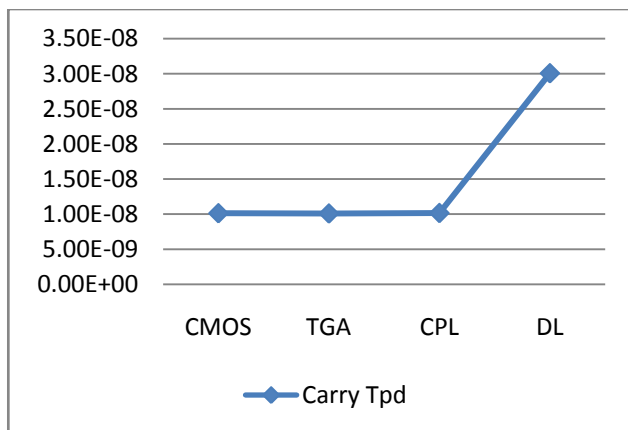


Fig. (d) Carry Propagation Delay

IV. Conclusion

From the simulation results it is observed that Transmission Gate Full Adder is the most efficient adder since it has the minimum delay and power dissipation. As a result it is the fastest adder among CMOS, CPL, DLA and TGA. Dynamic power consumption can be limited by reducing supply voltage, switched capacitance, and frequency at which the logic is clocked. Power consumption is a function of load capacitance, frequency of operation, and supply voltage. A

reduction of any one of these is beneficial. A reduction in power consumption provides several benefits. Less heat is generated, which reduces problems associated with high temperature, such as the need for heat sinks. This provides the consumer with a product that costs less. Furthermore, the reliability of the system is increased due to lower-temperature stress gradients on the device. An additional benefit of the reduced power consumption is the extended life of the battery in battery-powered systems.

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