Implementation of Binary Multiplication using Booth and Systolic Algorithm on FPGA using VHDL

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ABSTRACT

In mathematics, multiplication is the most commonly used operation. Though integer multiplication is used commonly in the real world, binary multiplication is the basic multiplication used for the integer multiplication. Systolic and Booth algorithms are the efficient algorithms to perform the binary multiplication. In this paper, an attempt is made to implement the prototype of binary multiplier using Booth algorithm (for signed number) and the systolic array multiplication algorithm (for unsigned number). This is implemented using Xilinx ISE6 software, simulated using Modelsim XE 5.5a Simulator by Mentor graphics. The synthesis is done on Field Programmable Gate Array (FPGA) Spartan2S15 kit using Very High Sp eed Integrated Circuit(VHSIC) Hardware Description Language (VHDL). The results are compared with the standard results of the paper presented at Peneng, Malaysia with the publication number ICSE2002 Proc.

General Terms

VHDL, FPGA, Xilinx.

Keywords

Booth algorithm,
Systolic algorithm.

1. INTRODUCTION

Multiplication is the form of repeated addition, which is the basic operation used in all branches of science and mathematics.Booth's multiplication algorithm is the multiplication algorithm that multiplies two signed binary numbers in two's complement form. The algorithm was invented by Andrew Donald Booth in 1951 while doing research on crystallography at Birkbeck Collegein Bloomsbury, London. Booth used desk calculators that were faster at shifting than adding and created the algorithm to increase their speed. Booth's algorithm is of interest in the study of computer architecture. Booth's algorithm is a technique to multiply two binary numbers of either sign may be multiplied together by a uniform process which is independent of any fore knowledge of the signs of these numbers. Booths algorithm takes on account two bits starting from the least significant digit in the multiplier at a time to decide on the partial products.Except for the last partial product for a particular multiplier, the partial products are shifted and added to the existing sum of partial products [1][2].

Systolic algorithm is the form of pipelining, sometimes in more than one dimension. In this algorithm data flows from a memory in a rhythmic fashion, passing through many processing elements before it returns to memory. A "systolic array" is an arrangement of processors in an array where data flows synchronously across the array between neighbors, usually with different data flowing in different directions. Each processor at each step takes in data from one or more neighbors (e.g. North and West), processes it and, in the next step, outputs results in the opposite direction (South and East) H. T. Kung and Charles Leiserson were the first to published a paper on systolic arrays in 1978, which refers to the 'pumping action' of the heart.

VHDL finds many applications because of its very high speed integrated circuit. It is a hardware description language and program can be loaded into the chip and can be used by tool user[5]. As the language supports flexible design methodology, it can be used to define complex electronic systems. Common language can be used to describe the library components [6]. Because of its unique feature, VHDL is used to design N-bit binary multiplier. The program in VHDL provids the scope for multiplication of two N-bit binary numbers by including the user defined package.

2. PROBLEM FORMULATION

In VLSI design system, "power", "speed" and "area" are the most important parameters to achieve cost effective and reliable systems. Logic present in FPGA provides the same. VHDL is the verification tool for implementing the design on FPGA. But VHDL directly doesn't support the binary multiplication. Binary multiplication is the most commonly used algorithm in mathematics. If progra mmer wants to use the binary multiplication, then programmer has to write the code for the same, which is not the main aim of the programmer. This method is time consuming for the programmer. The solution to this problem needs the binary multiplication algorithm is written in the VHD L and included in the library so that programmer can directly use this in his program and do the main program efficiently.

3. IMPLEMENTATION

According to Booth's multiplication algorithm among the two input binary numbers the one with minimum number of bit changes is considered as multiplier and the other as a multiplicand in order to reduce the time taken for calculating the multiplication product. For getting a multiplication res ults with mini mum delay following steps should be followed-

1.According to the number of changes in the operands, multiplier and multiplicand are assigned with two numbers.

2.Based on the last two bits of the multiplier following actions are carried out as follows:

a) 00-Shift multiplicand right by one position.

b) 01-Add multiplicand to regist er U and shift.

c) 10-Subtract multiplicand from register U and shift. d) 11-Shift multiplicand right by one position.

3.This process should be continued till N iterations are carried out.

The block diagram of Booth multiplier is as shown in figure 1. In systolic multiplicationalgorithm,to carryouthe multiplication and get the final product following steps should be followed

1.The multiplicand and multiplier are arranged in the form of array as shown in the figure 2.

2.Each bit of multiplicand is multiplied with each bit of multiplier to get the partial products.

3.The partial products of the same column are added along with carry generated.

4.So the resulted output by adding partial products and the carry is the final product of the two binary numbers.

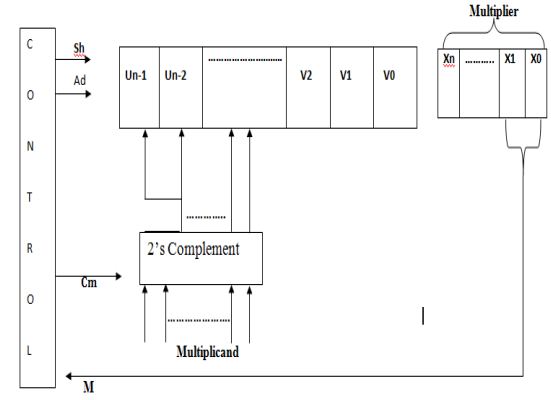

Figure 1. Block diagram of Booth's multiplier [3].

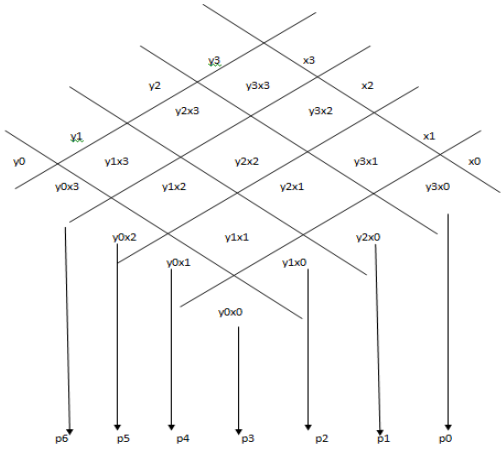

Figure 2. Block diagram of Systolic multiplier [3].

3.1 FPGA is best suited for the design

The above mentioned results are accurate and error free. But, if it is time consuming then the efficiency of multiplier decreases because, in recent days the efficiency is measured n ot only with the accuracy but also with the speed. As FPGA is purely hardware circuit, the time taken by it to execute the algorithm is much less than the time consumed by the softwares. Thus, the binary multiplication algorithm implemented on FPGA works faster than any other multiplication technology.

4. RESULTS:

4.1 Simulation results

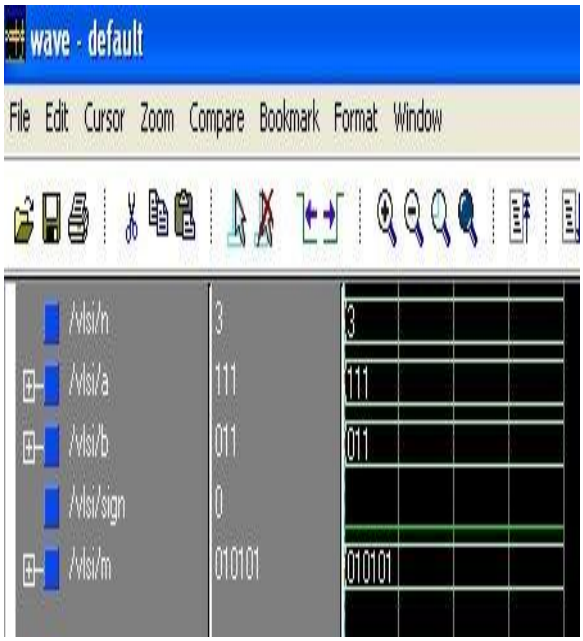

Figure 3. Simulation result of unsigned multiplication.

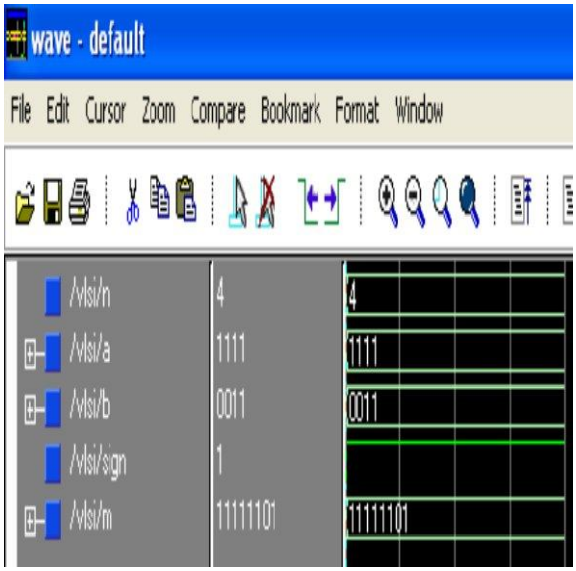

Figure 4. Simulation result of signed multiplication.

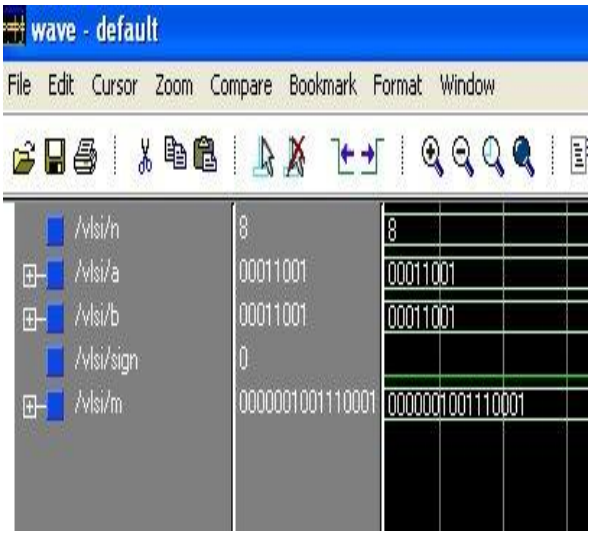

Figure 5.Simulation result for 8 bit unsigned multiplication

Simulation results are as shown in the figure 3. and figure 4. Figure 3. shows the simulation result for unsigned numbers. The inputs given are 111(7) and 011(3) and the output obtained is 10101(21). Figure 4. shows the multiplication of signed numbers. Here one bit (MSB) represents the sign of the number and others represent the magnitude of the number. One indicates that the number is negative and zero indicates that the number is positive. The inputs provided are 1111(-1) and
0011(3). The output obtained is 11111101(-3) is in 2's complement form. The sign bit should be made one for signed
multiplication and it should be zero for unsigned multiplication.
Here 'n' represents the number of bits in multiplicand and multiplier. The number of bits in the output is twice the number of bits in multiplicand or number of bits in multiplier.

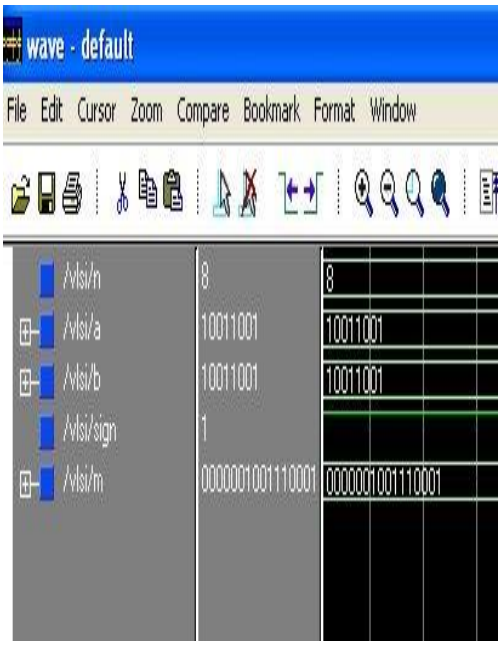

Figure 6. Simulation result of 8 bit signed multiplication with two negative numbers.

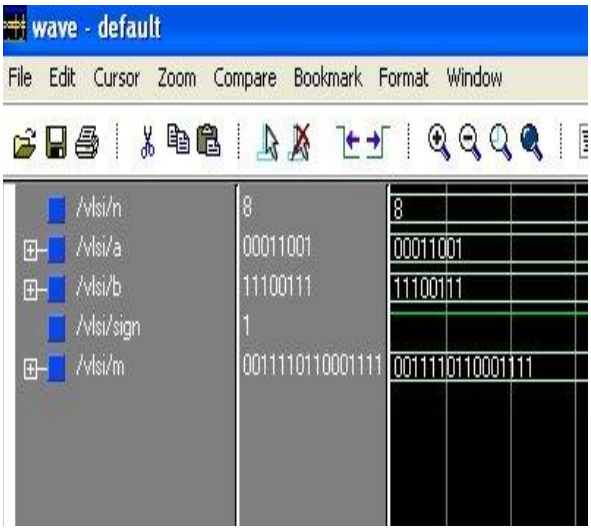

Figure 7. Simulation result for 8 bit signed multiplication with one positive and one negative number.

4.2 Synthesis Results

The synthesis is done on Spartan 2 i.e. XC2s15.The synthesis report for N-bit multiplier is as shown in the figure 7 and 8 respectively. Figure 7. shows the timing constraint for default path. The total delay obtained is 20.249ns. This delay includes the logic gate delay and the routing delay. Here the logic delay is 8.738ns and routing delay is 11.511ns.This routing delay can be minimized by placing the logic gates in an optimal fashion. This can be achieved using structural style of modeling. Figure 8. shows the design statistics. It provides the information about the number of multiplexers, xor gates, LUTs etc… used to implement the code.
The implemented multiplier is compared with Lakshmanan, Masuri Othman and Mohamad Alauddin Mohd. Ali paper published by ICSE Proc, 2002, Peneng, Malaysia, multiplier method takes 50ns where as proposed design by us takes 20ns hence faster , efficient , and consumes low power.

```
293  ------------------------------------------------------------------------
294  Timing constraint: Default path analysis
295  Delay:              20.249ns (Levels of Logic = 8)
296    Source:           a<2> (PAD)
297    Destination:      m<6> (PAD)
298
299    Data Path: a<2> to m<6>
300                                 Gate     Net
301      Cell:in->out      fanout   Delay    Delay  Logical Name (Net Name)
302      ----------------------------------------  ------------
303       IBUF:I->O           62   0.776    4.770  a_2_IBUF (a_2_IBUF)
304       LUT3:I2->O           5   0.549    1.566  SF25451 (SF2545)
305       LUT4:I2->O           1   0.549    1.035  Mmux_m_Result<6>57 (CHOICE1468)
306       LUT4:I2->O           1   0.549    1.035  Mmux_m_Result<6>71 (CHOICE1470)
307       LUT4:I2->O           1   0.549    1.035  Mmux_m_Result<6>358_SW0 (N17228)
308       LUT4:I1->O           1   0.549    1.035  Mmux_m_Result<6>358 (CHOICE1523)
309       LUT4:I3->O           1   0.549    1.035  Mmux_m_Result<6>370 (m_6_OBUF)
310       OBUF:I->O                4.668          m_6_OBUF (m<6>)
311      ----------------------------------------
312      Total                    20.249ns (8.738ns logic, 11.511ns route)
313                                       (43.2% logic, 56.8% route)
314
315  ========================================================================
```

Figure 8. Synthesis result of timing constraint

for default path.

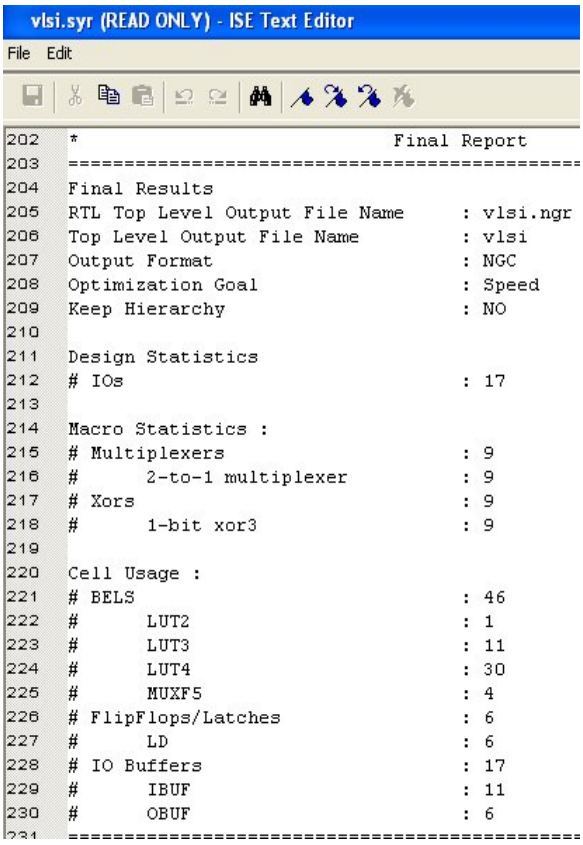

Figure 9.Final report of multiplication algorithm.

5. CONCLUSION

The binary N-bit multiplier is efficiently implemented on hardware. Though there are many binary multipliers used at present, they can be replaced by FPGA binary multiplier which consumes less area, takes less time to multiply and consumes less power, which are the main criterions of the present system. Since VHDL does not support binary multiplication,the system designed helps us perform multiplication in VHDL programming by including the library containing the user defined package for multiplication. The time taken to multiply two N-bit numbers is 20.249ns

6. ACKNOWLEDGMENT

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l=1&fp=bdd9097c9b58ade7.

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