An Approach for Minimizing CMOS Layout by Applying Euler's Path Rule

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ABSTRACT

An attempt has been made to reduce area requirement while improving electrical characteristics during very large scale integration (VLSI) design. The area can be reduced by designing a layout without diffusion breaks. In this paper, a method is proposed that provides more compact layout without breaks in diffusion with minimal metal pattern, less contacts and low parasitic capacitance. A novel approach towards constructing Euler's path on complementary metal oxide semiconductor (CMOS) circuit is also discussed.

General Terms

VLSI design , CMOS

Keywords

Euler's path, Optimal layout, Metal pattern, Diffusion breaks

1. INTRODUCTION

Minimization of area and improving electrical characteristics is the main aim in VLSI. The area can be minimized by designing a layout without diffusion breaks. The goal of this work is to find an ordering of the MOSFETs such that a minimum number of diffusion brakes are required [2], [3]. It is possible to reorder the signals to eliminate the brakes in some cases [4]. By minimizing the number of diffusion breaks it is possible to fabricate the complex circuit which needs lesser chip area [7]. This study discusses how to get a optimal layout area without breaks in the diffusion.

The paper is organized as follows. Section 2 introduces the basic concepts with the help of complex circuit. The comparison of area requirement, diffusion brakes and metal pattern is discussed in section 3. Finally in section 4 the major findings are written.

2. METHODOLOGY

In Euler path approach, the dual network graph is drawn. Each N-channel MOSFET in pull down network is expressed by an edge and each node by a vertex. The vertices in the graph are source/drain of the device. Each edge is named with the gate signal name for that particular MOSFET [1], [5], [6], [7]. Then a dual pull up graph is constructed from the pull down graph using the dual graph concept. A new vertex is created within each confined area in the pull down graph and neighboring vertices are connected by edges which cross each edge in the pull down graph only once [6],[7]. This new graph represents the pull up network of PMOS devices. The name of the device in pull up graph will be the name of edge of pull down graph which is cut. The methodology is discussed with the help of following example;

The circuit diagram of the complex equation

$$Z = \overline{A (D + E) + B C}$$

is drawn as shown in fig (1).

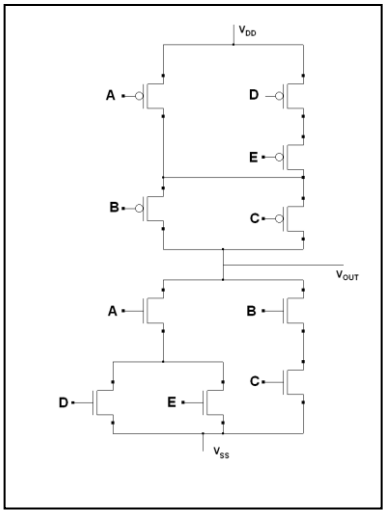


Fig. 1: Circuit diagram of COMS complex equation

$$\mathbf{Z = \overline{A (D + E) + B C}}$$

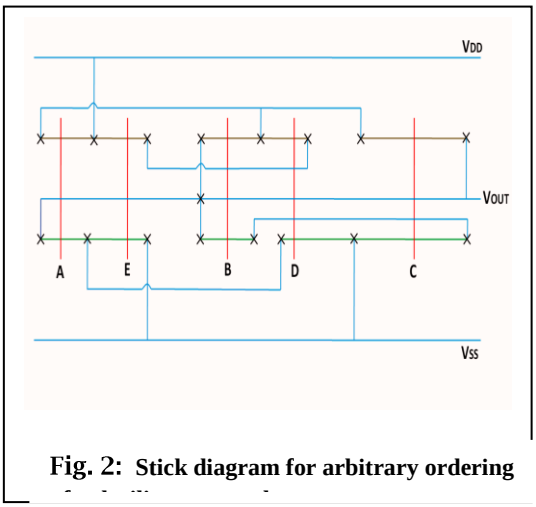


Fig. 2: Stick diagram for arbitrary ordering

The Euler graph of fig (1) network is as shown in fig.(3)

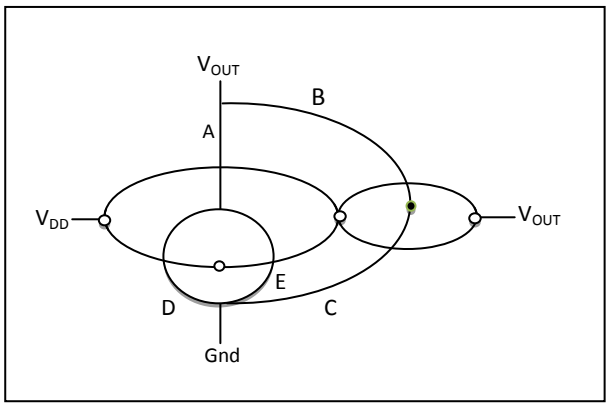


Fig. 3: Euler graph

The separated pull down and pull up graphs are shown in fig.(4) and fig.(5)

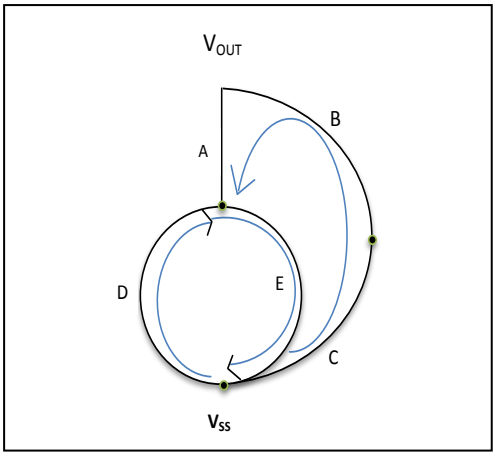


Fig. 4: NMOS Graph

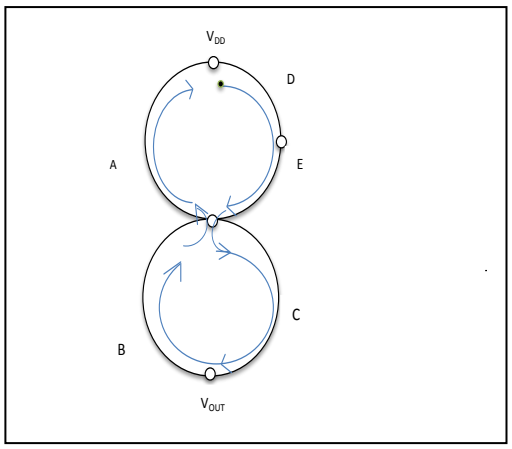
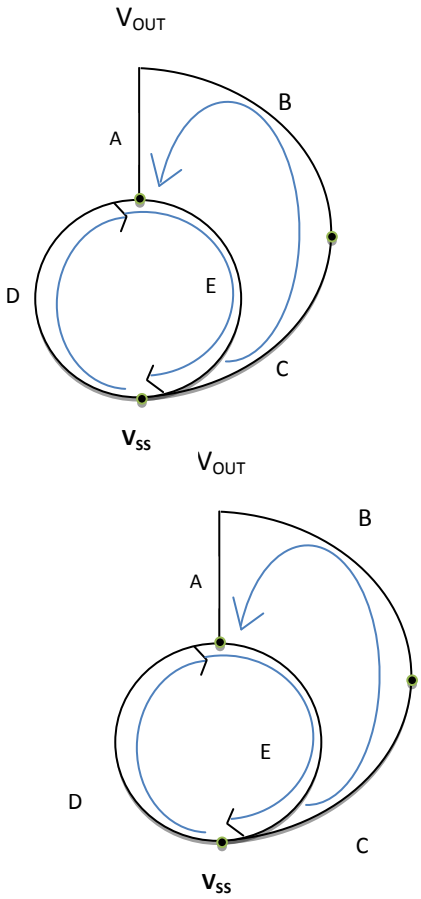


Fig. 5: PMOS Graph



The Euler path in the pull down graph and pull up graph with identical ordering of input labels are drawn as shown in fig (4) and (5). The Euler path is defined as an uninterrupted path that traverses each edge (branch) of the graph exactly once. To simplify the metal connections following rules are used:

For pull down

i) For pull down start from Vss/Vout.

ii) If only one source is connected to Vss then start from extreme left.

iii) If two sources are connected to Vss then start the metal pattern of Vss connection in between two polysilicon strips or two metal strips at two ends of diffusion.

iv) If three sources are connected to Vss then one Vss connection from extreme left which will connect the source to ground and other two sources are connected by drawing metal strip from Vss and between two polysilicon strips of the two devices whose sources are to be connected to Vss.

For pull down

i) For pull up start from V_{DD}/Vout.

ii) If only one source of PMOS device is connected to V_{DD} then draw metal strip from extreme left.

iii) If two sources are connected to V_{DD} then start the metal pattern of V_{DD} connection between two polysilicon strips or two metal strips at two ends of diffusion..

iv) If three sources are connected to V_{DD} then one V_{DD} connection from extreme left which will connect source of one device to V_{DD} and other two sources are connected by drawing metal strip from V_{DD} and between two polysilicon strip of the two devices whose sources are to be connected to V_{DD}.

If odd number (N) of sources are connected to ground / V_{DD} then total vertical metal strips from V_{SS}/V_{DD} to diffusion (if there are no breaks in diffusion) will be

$$1 + (N-1)/2$$

One metal strip from extreme end and (N-1)/2 will be between polysilicon strips. The number of vertical metal strips from V_{SS}/V_{DD} to diffusion will be minimum if there are no breaks in diffusion. If breaks in diffusion are present then some extra metal strips from V_{SS}/V_{DD} to diffusion are required, which will increase area and parasitic capacitance

If even number of sources (N) are connected to V_{SS}/V_{DD} then total vertical metal strips from V_{SS}/V_{DD} to diffusion will be,

$$2 + (N-2)/2$$

(if two metal strips are at extreme ends of diffusion.) or

$$N/2$$

(if no metal strips at extreme ends of diffusion.)

While drawing metal strips from V_{SS}/V_{DD}, follow the path and name the terminals of the device. The stick diagram of fig (1) using Euler's rule is shown in fig.(6)

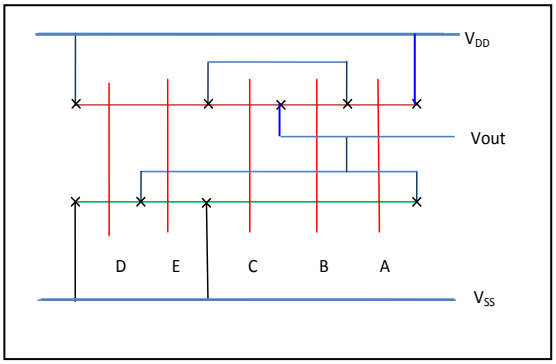


Fig. 6: Stick Diagram for polysilicon ordering using Euler's rules.

The names of terminals of the devices are given according to the path travelled.

3. RESULT AND DISCUSSION

The mask layout for arbitrary ordering of polysilicon gates is shown in fig (7). Fig(8) shows proposed layout when Euler's rules are used.

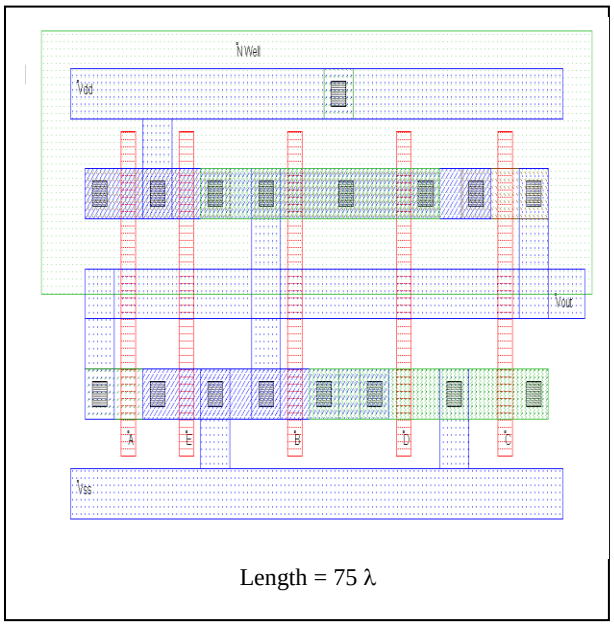


Fig. 7: Mask layout for arbitrary ordering of polysilicon gate columns.

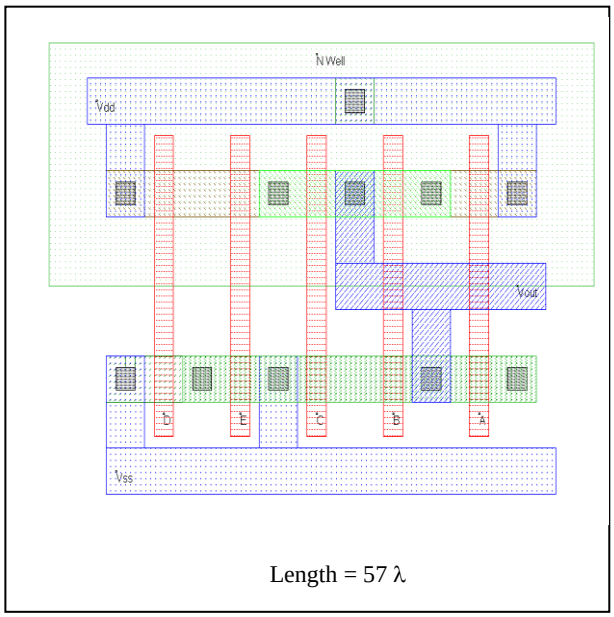


Fig. 8: Mask layout for polysilicon gate column ordering using Euler's rules.

From the two layouts drawn using Microwind software following observations regarding area of the layouts, diffusion breaks and number of metal contacts are made.

Parameter	**Layout for arbitrary ordering of polysilicon gate columns.**	**Proposed layout using Euler's rule.**
Length	75λ	57λ
Diffusion breaks	4	Nil
Metal contacts at diffusion	16	10

Table 1

The layout comparisons are shown in Table (1), it is clear that the length required using proposed method is less as compared to the length required using arbitrary ordering of polysilicon gate column method. Due to reduction in length less area is required. For the example discussed above, there is 24% saving in the area. The diffusion breaks and metal contacts at diffusion are reduced in the proposed method. Due to this the parasitic capacitance decreases which helps in reduction of the propagation delay time.

4. CONCLUSION

This work changes the viewpoint of ordering of polysilicon gate columns and constructing the metal pattern on CMOS circuits and puts some basic layout ideas into systematic approach. The method makes more compact layout with less breaks in diffusion, metal contacts and parasitic capacitance. The proposed method provides another way of designing metal pattern using Euler's path on CMOS circuits.

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