# Design of Control Circuit for Torsion Bar Testing Machine

P.Maran
SSN Engineering college
Chennai, India

E.Madhankumar
St.Peter's University
Avadi, Chennai,India

P.Mathivanan
SriRam engineering college
Avadi, Chennai, India

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**ABSTRACT**In today's industrial and research laboratories more applications are calling for control and data acquisition (DAQ) devices. Personal computers have become a primary tool in data acquisition with the development of hardware and software interfaces. Our paper is aimed at developing a control circuit for the torsion bar testing machine. The torsion bar testing machine is used to increase the resilience of the torsion bar i.e. to increase the elasticity of the torsion bar and as well as to check the quality of the manufactured bar. The existing circuit for the torsion tester is designed to be compatible with the ISA bus of the main computer but in today's modern world ISA bus has become obsolete with the introduction of the more efficient PCI bus and our project is aimed at designing a control circuit that is compatible with the PCI bus of the main system and also to reduce the circuit complexity. The main advantages of the PCI bus over ISA are high bandwidth and speed and no address conflict problems which helps in efficient operation of the machine. One part of the project involves in making PCI I/O card that is concerned with passing the control signal to the rotor and as well passing angular position of the rotor to the main system and the second part of project involves in designing the circuit that controls the rotor of the machine.

## KEY WORDS

plug and play, position feedback, rotary encoder.

## 1. INTRODUCTION

A torsion bar suspension, also known as a torsion spring suspension ortorsion beam, is a general term for any vehicle suspension that uses a torsion bar for its suspension here we have several advantages over normal suspension, it takes less space than other suspension systems. It provides more spacious compartment for passenger. The height of torsion bars can also be adjusted more easily than other suspension systems. They are also extremely durable and traditionally have a long service life. Here one end of a long metal bar is attached firmly to the vehicle chassis; the opposite end terminates in a lever, mounted perpendicular to the bar that is attached to a suspension arm, spindleor the axle. Vertical motion of the wheel causes the bar to twist around its axis and is resisted by the bar's torsion resistance. The effective spring rate of the bar is determined by its length, cross section, shape and material. Torsion bar suspensions are currently used on armored fighting vehicles or tanks like the T-72, Trucks and SUVs from Ford, Dodge, GM, control circuit is based on the ISA bus and this ISA card is designed in such a way that it contains two 8255 programmable peripheral interface chips and the control signals form the card are transmitted to the machine and the feedback from the rotor is given back to the main system, but now these ISA bus loose their scope. Considering it importance this testing machine control circuit has been remodeled by using our designed control circuit for its efficient operation.



## 2.WORKING OFTORSION BAR TESTING MACHINE

The main aim of testing torsion bar is to check whether it can with stand the suspension of heavy duty vehicle. Here the suspension bar is tested with suitable arrange as per the setup in vehicle with one end is fixed where as other end is rotated to maximum degree to check its suspension level. During this process generated force at the fixed end is converted into voltage using load cell and then into current and finally digital value is obtained in the main system via serial communication. In the rotating end a counter counts the pulses produced by the encoder and the value is fed into the system the PCI card, Depending on the both inputs, the systemcalculates the residual angle, once the predetermined angle is reached it stops rotating and start rotating in reverse direction till the load cell shows 0Volts the angle measured at this point is the residual angle, here PCI card acts as the interface between the system and the machine and The program will execute all five cycles of the testing procedure and moves rotor according to it. A model explain how the torsion bar acts as suspension Fig1.2a and the block diagram of torsion bar testing machine is shown in the fig1.2b

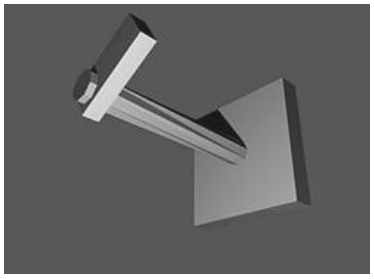

Fig1.2a Torsion Bar as Suspension

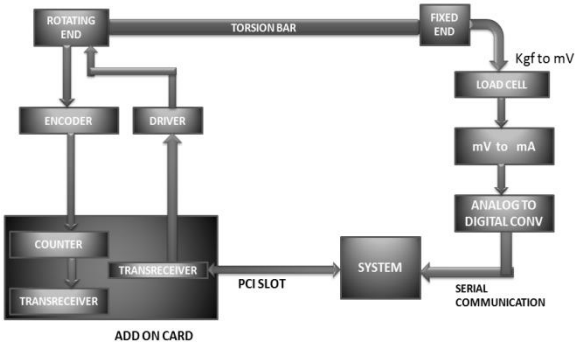


Fig1.2b Block diagram of Torsion bar testing machine

## 3. ENHANCING ISA BUS USING PCI CARD

Our aim is to enhancing the existing control circuit to PCI technology; usuallyPCI is a complete synchronous bus where all its operation is based on system clock cycle. It solves many of the problems with older architectures and also increases the speed of operation here PCI provides a new way of connecting peripherals to both the system memory and the CPU. [1,2,3]

After inserting PCI card into the PCI slot of the main system,set the base address of the card using dip switch to avoid the conflict with other address and then the main program in C, which controls the entire testing procedure is executed. GAL 22v10 acts as the mediator between the PC and the control circuit, handling all the control signals from the system and make the entire circuit to act as PCI target. When the execution of the program begins the rotor starts rotating and encoder sense pulse to drive counter, here the main program computes the angle of the rotor with the feed back value from the counter and it takes the decision according to it as explained later. Further, program executes all the five cycles of testing procedure and their results are analyzed. From the obtained results the residual angle of torsion bar is studied, which determine whether it suit for the requirement, here Operation of control circuit in testing machine is studied and shown in the fig 1.4 a.

*The Operation of the PCI I/O Board*

Initially the bus is in STATE 4 that is Bus is in idol state; the beginning of the new bus operation is detected in this state based on the C/BE [3:0] #signal from PCI. It transits to STATE 2(write) or STATE 5(read) when an I/O cycle is initiated to this target device. It transits to STATE 0 when a bus cycle with no relations with this target device begins. When the C/BE[3:0]# is 0011 the bus transits from STATE 4 to STATE 2 by this I/O write cycle to this device is being executed. In STATE 2 this device asserts DEVSEL# and responds bus cycle.At the same time, target device asserts TRDY# and shows that it is ready to accept data from initiator.

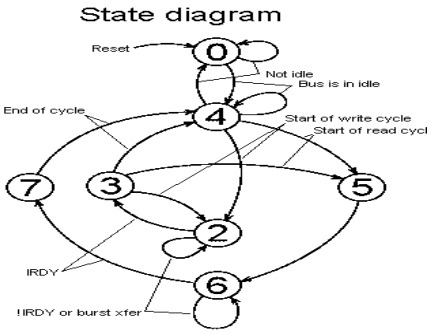


Fig 1.3 State diagram [1]

At this time, it latches data and transits to STATE 3 when IRDY# is being asserted (initiator ready to send data) and FRAME# is being deasserted. In STATE 3 DEVSEL# and TRDY# is deasserted normally, DEVSEL# and TRDY# are released at the next clock, and transits to IDOL STATE (STATE 0).It can transits directly to STATE 2 or STATE 5 from STATE 3 without passing through the IDOL STATE when it faces the device under this state and I/O read/write command was issued again. (fast back to back transaction) if the state transits from STATE 3 to STATE 2 write cycle is executed in the same manner and this process continues till all the bytes are transferred from initiator to target, and then it goes to STATE 4 waiting for next control signal , on the other hand if the state transits from STATE 3 to STATE 5 the read cycle begins without passing through the IDOL STATE, the STATE 5 can also be reached from STATE 4 if the C/BE[3:0]# is 0010 once the bus reaches the STATE 5 the read operation begins then it transits to STATE 6 where the Read cycle is in progress. Target device asserts DEVSEL# and respond to the read cycle. At the same time, output read data to the AD bus and asserts TRDY#. At this time, it transits to STATE 7 when IRDY# is being asserted (initiator can accept read data) and FRAME# is being deasserted (last data).during which the Read cycle is finished. Target device deasserts DEVSEL# and TRDY#. Then, release DEVSEL# and TRDY# at the next clock and it transits to the IDOL STATE. For any other condition in the C/BE[3:0]# then it is considered as STATE 1 which is undefined so it will transit to STATE 0 and then the same cycle continues[1,2,3]

## 4. DESIGNING ROTARY CIRCUIT USING H-BRIDGE

PORTS of 8255 are configured to work as simple I/O by writing a control word in its control register by using the main program, and then the values are transferred to ports which command the rotor to rotate in either forward or reverse direction by using H-Bridge.OPTOCOUPLER is used to prevent back off and to provide isolation between PCI card and H-Bridge in the in rotor control circuit .while executing the main program the rotor starts rotating and now the pulses are generated from rotary encoder which are given to the squaring circuit to get perfect clock pulses. Now the counter starts counting. The counting data is simultaneously communicated to the system via 8255 and PCI, Now the main program will compute the degree of rotation of the rotor using counter values and decides further process as stated in section2. [3]

## 5. COMPARISON RESULT OF PCI BUS

PCI bus with 32 bit (read/write ) cycle is compared with the ISA(read write ) cycle of the bus here PCI bus perform 2000 times faster than ISA and other bus with the maximum operation frequency range of 25 MHZ are analyzed and tabulated in the Table 1 below.

| Types of bus | Fast PCI(32 bits) bus | Slow PCI(32 bits) bus | ISA(16 bits) bus | C-bus |
|---|---|---|---|---|
| Speed(cycle/sec) | 5525 | 3737 | 1422 | 1060 |
| Operating frequency($MH_Z$) | 33.3 | 33.3 | 8.33 | 10 |

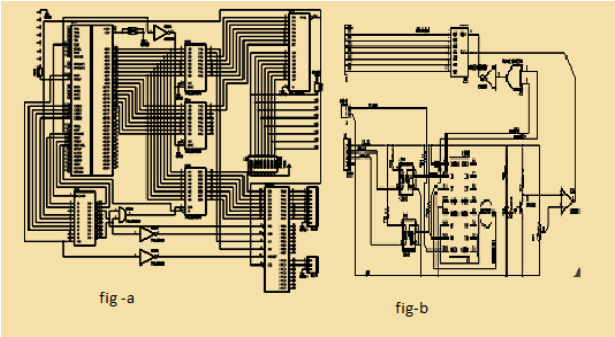


Fig 1.4 a.PCI add-on card, b.Rotor control circuit

## 6. CONCLUSION

The ultimate objective of the project is to design a control circuit for the torsion bar machine. Our aim was to enhance the existing old circuit of the machine to the current technology. We successfully designed and implemented the PCI I/O card and the rotor control circuit. From our detailed study of the project we conclude that PCI bus has higher speed and wide bandwidth over the ISA bus. The future enhancement in this project would be replacing GAL with complex FPGA, which would even more enhance the speed of PCI I/O card

## 7. ACKNOWLEDGMENT

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