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Result Verification Of CMOS Full Adder Used For Wallace Tree Multiplier

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ABSTRACT
Wallace Tree Multiplier (WTM) is the fastest multiplier used in number of data-processing processors to perform fastest arithmetic function. From the structure of the RCWM Reduced Complexity Wallace Tree Multiplier, it is clear that there is scope of reducing the power consumption and area. This work uses an efficient and simple gate-level modification to significantly reduce the power and area of RWTM. Conventional WTM is still area-consuming due to the CMOS switching structure. The logic operations involved in conventional RCWM and WTM are analyzed to study the data dependence and to identify redundant logic operations. RCWM reduced number of half adders used in Standard Wallace Multiplier (SWM) with slight increases in full adders to reduce the multiple numbers of gates. Adiabatic Logic eliminated all the redundant logic operations present in conventional RCWM. Experimental analysis shows that this architecture achieves the three folded advantages in terms of power and area.

Keywords
adiabatic logic, Wallace tree multiplier, tanner tool, 16×16 multiplier.

1. INTRODUCTION
Multiplier is one the most important component of many systems. In high speed digital signal processing - DSP and image processing multiplier play a vital role. In image processing fast Fourier transform (FFT) is the most important transform often used. Computational process of fast Fourier transform required large number of addition and multiplication operation. The execution of these algorithms required dedicated MAC, Arithmetic and Logic Unit (ALU) architecture. Adders and multipliers are the key element of these arithmetic units as they are in the critical path. With the recent advancement in technology, many researchers are tried to implement increasing efficiency of multiplier. They aim at offering high speed, low power consumption and reduction in delay.

One such multiplier is Standard Wallace Multiplier (SWM). SWM is totally parallel version of the multiplier, the carry save adders used in SWM are conventional full adders whose carries not connected, due to that three inputs are taken and two words are out. SWM also uses half adders that reduction in phase. A Wallace Multiplier is easily a hardware implementable and efficient methodology that multiplies two integers, proposed by Chris Wallace; he is an Australian Computer Scientist. For unsigned multiplications, up to n number of shifted copies of the multiplicands are added to form the result. The entire procedure is carried out in to three steps; partial product generation, partial product grouping and reduction, and final addition. The principle of Wallace tree multiplication. For the n x n multiplication there are partial products that have to be summed. The 1st steps in the algorithm involved in grouping the partial products into set of 3. For example, if there are *n'* rows of partial products - 3*[n/3] rows are grouped and the remaining n mod 3 rows are passed to the next stage. Therefore 3 rows of partial products are grouped with each other in stage 1; These 3 rows are then sum using full adders and if there is 2 dots in particular a column the half adder is used. The resulting carries and sum signals from the half and full adders are passed to the next stage. The processes are repeated till the entire partial products are summed. The resulting carries and sum out of the last stages is added using carry propagation adder at the final stage.

Reduced complexity Wallace multiplier RCWM [1] reduced multiple number of half adders use in SWM with slight increases in full adders to reduces the multiple number of gates. Reduced complexity Wallace Multiplier RCWM is the modified version of Standard Wallace Multiplier - SWM. In SWM they used full adder and half adder their reduction in phase, but half adder do not reduces the number of partial bit , therefore RCWM reduces the number of half adders used in the SWM with slightly increase in the full adder . The partial products are formed by AND gates. The partial products are arranged in the Tree structure format. The modified Wallace reduction methods divide the matrix into three groups. Full adder is use for each group of three bits in a column like Standard Wallace reduction. A two bits group in a column isn't processed, so it is passed on to the next stage in contrast to the Standard Wallace method. Single bits are passes on to the next stage in the Standard Wallace reduction. The only time half adder is used to ensure that the number of stages doesn't exceed that of a Standard Wallace multiplier. For the some cases, half adder is used in the final stage of reduction. In RCWM they use carry propagating adder CPA. One possible carry propagating adder for RCWM is the hybrid adder consist of S+1 ripple carry half adder.

Both the multipliers SWM and RCWM have same numbers of stages and delay is also same between them. In Energy Efficient CMOS full adder in reduced complexity Wallace Multiplier (RCWTM) at the place of Full adder of (SWM) Standard Wallace Multiplier in order to improvement in speed and reduce Area, Power. An Energy Efficient CMOS Full adder design using alternative logic scheme gives low power delay product (PDP), in terms of power consumption, speed and reduced area. This paper proposes use of new Energy Efficient switching method that is the adiabatic switching for CMOS full adder in (RCWTM) reduced complexity Wallace multiplier in order to reduce power even further.

Adiabatic Logic is the term shows that low-power electronic circuit's operations. The problem of energy dissipation in faster and smaller circuit is solved by Adiabatic logic. The main causes of energy dissipation in CMOS circuits are due to the discharging and charging of the node capacitor. In adiabatic switching, the process of charging and discharging the node capacitance is carried out in the way so that a small amount of energy is wasted and a recovery of the energy stored on the capacitor is achieved. Adiabatic switching can be achieved by ensuring that the potential across the switching devices is kept small. This can be achieved by charging the capacitor from constant curent source or a time varying voltage source.

2. LITRATURE REVIEW

Authors Shahebaj Khan, Yogesh Suryawanshi , Sandeep Kakde suggest the technology entitled "VLSI Implementation of Reduced Complexity Wallace Multiplier Using Energy Efficient CMOS Full Adder" in to which modified reduced complexity Wallace Multiplier with reduced power consumption and area by using Energy Efficient CMOS Full Adder. 2**.** Author C. S. WALLACE suggested a technology for multiplier entitled "A Suggestion for a Fastest Multiplier" suggest A Multiplier is an easily hardware implementable and efficient methodological, that multiplies two integers. 3. Authors Kazunari Kato, Yasuhiro Takahashi, and Toshikazu Sekine suggested in paper entitled "Two Phase Clocking Sub-threshold Adiabatic Logic". They proposes a novel sub-threshold adiabatic logic. Our previously proposed ultra low-power sub-threshold adiabatic logic has been a problem that the noise margin is reduced, so that it is impossible to implement a cascade connection. 4. Author Yasuhiro Takahashi, Nazrul Anuar and Toshikazu Sekine in paper entitled "4-bit Ripple Carry Adder using (TPCL) Two Phase Clocked Adiabatic CMOS Logic" presented the low energy operation of 4-bit ripple carry adder (RCA) employed two phase clocked adiabatic static CMOS logic (2PASCL) circuits techniques. 5. Authors Toshikazu Sekine H. Rahamanin, M. Chanda, A. Dandapat paper entitled "Ultra Low-Power Sequential Circuit Implementation by a Quasi Static Single Phase Adiabatic Dynamic Logic - SPADL" presented the Implementation of sequential logic circuits by using a novel Quasi-Static Single-phase Adiabatic Dynamic Logic (SPADL) has been presented.

3. ENERGY EFFICIENT CMOS FULL ADDER

Alternative logic Structure For a Full Adder an Energy Efficient CMOS Full adder design using alternative logic scheme gives low power delay product - PDP, in terms of power consumption, reduced Area and speed. Examining the truth table of EECFA, it can be seen that the S0 output gives A B when C=0, and it also gives A B when C= 1. Thus, the Multiplexer can use to obtain the respective value taking C input as a selection signal. Following the same criteria taking C0 as a output equals to A×B when input C=0, and A+B when input C=1. Again C can be used as a respective value for the required result, using Multiplexer. An alternative logic schemes to design a full adder cell can be formed by a logic block to obtain the A B & A B signals , another block can be obtain the A × B and A + B signals, and two Multiplexers driven by the C input to generate S0 and Cs0 outputs as shown in fig 1. Full adder design using swing restore complementary Pass-Transistor logic (SR-CPL) style build the AND/OR gates And XOR/XNOR gates, and multiplexer based on pass transistor to obtain S0 and C0 output. The AND/OR gates build using a powerless and groundless pass-transistor logic.

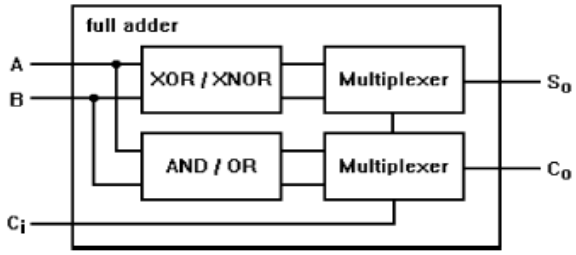

Fig1. Alternative Logic scheme for CMOS Full Adder – from ref. [2]

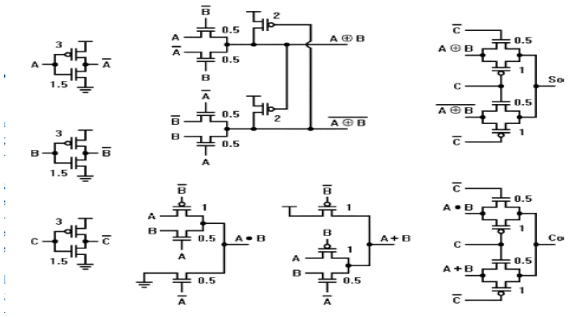

Fig. 4. Full-adder designed with the proposed logic structure- from ref.[2]

Double-pass transistor logic eliminated some of the inverter stages required for the complementary pass transistor logic by using both N and P transistors, with dual logic paths for every function. While due to low input capacitance it has high speed , it has very limited capacity to drive a load.

1. Proposed Architecture

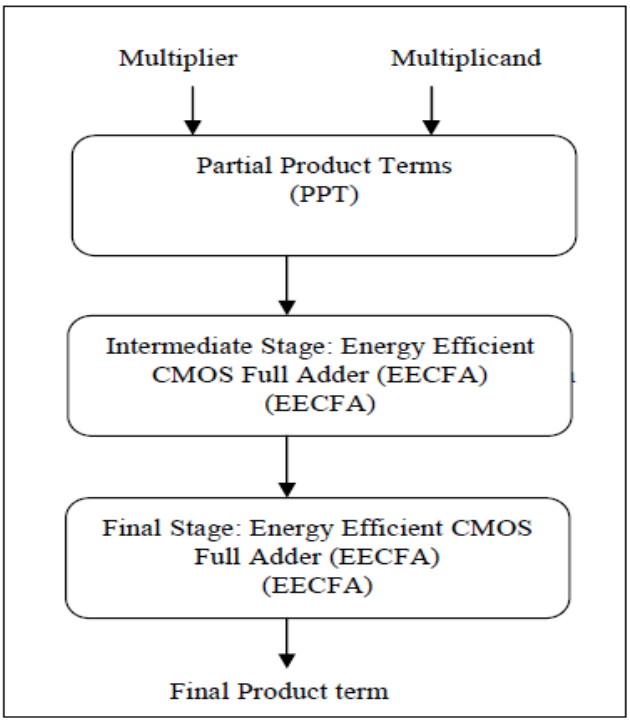

Fig 2. Proposed Wallace Multiplier using energy efficient CMOS Full adder -from ref.[1]

Proposed architecture has same stages as RCWT Multiplier. At the stage of conventional full adder is present. Energy Efficient Full Adder is used as shown in Fig 2. Our proposed architecture aims to leads to increase speed and reduced overall power consumption. The design makes use of Energy Efficient CMOS Full Adder in the Place of conventional full adder. Let two numbers multiply using RCWT Multiplier as shown below. The RCWTM Multiplier has three steps. Multiply (that is - AND) each bit has one of the arguments, by each bit of the other, giving *n*2 results. Depending on position of the multiplied bits, the wires carrying different weights, for e.g. wire of bit carrying result of a2 b3 is 32. Fig 3 shows the multiplication of two 4-bit numbers. The numbers are denoted by A & B where a0 , a1, a2, a3 represents the bits of multiplicands A with as its least significant bit and significant bit b0, b1, b2, b3 represents the bits of multiplier B with as its least significant bit and its most significant bit. The Multiplication of two 4-bit numbers giving partial products, which arrange these partial products bit in tree format and reduced the group of two bit using Half adder shown in first stage, reduced group of three bit using full adder shown in second stage of Fig 4. Then final adder adds all the result of second stage give final product, which is of 8-bit.

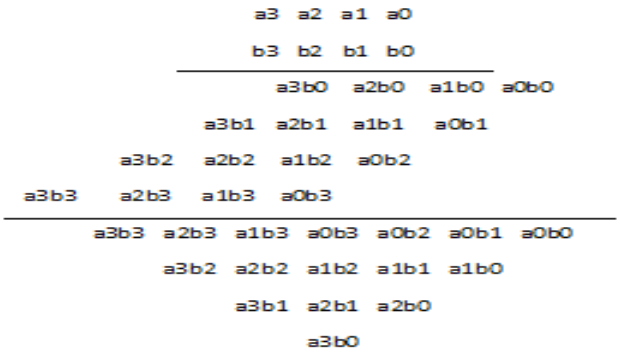

Fig 3. Multiplication of two 4 bit numbers-from ref.[1]

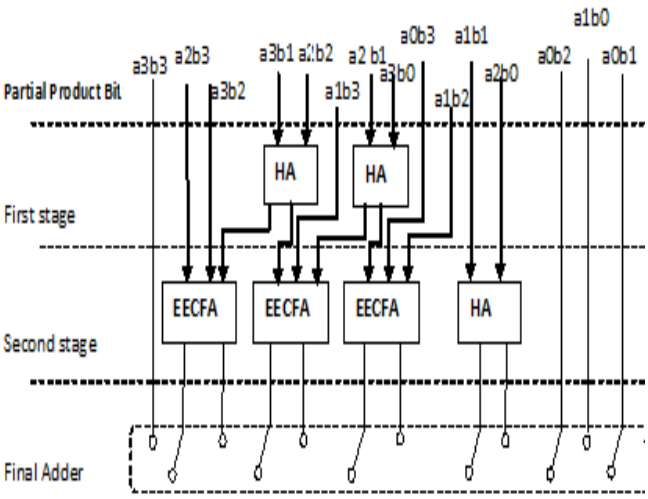

Fig 4.Proposed Architecture of 4×4 Wallace Multiplier-from ref.[1]

4. AREA OPTIMIZED WALLACE TREE MULTIPLIER

Table IComplexity Of Reduction

Proposed Wallace Tree Multiplier Using EECFA					
Number of bits	8	16	24	32	64
Number Of stages	4	6	7	8	10
Full Adders	39	201	490	907	3853
Half Adders	3	9	16	23	53
Total Gates	324	1644	3984	7348	31036

Table I shows the complexity reduction. As seen from the table the total gate count for proposed multiplier is reduced as compare to other multiplier. Total number of gate count for full adder is 8 and for half adder is 6. Table II below shows the comparison between conventional full adders i.e. carry propagate adder and proposed full adder [4]. From the below table it is seen that total fate count in carry propagating adder is 32 and in conventional full adder it reduced to 26 because of this total gate count for multiplier is reduced.

Table 2Comparison Table For Full Adder

ADDER	GATE COUNT
Carry Propagate Adder	32
Proposed Full Adder	26

5. SIMULATION RESULTS AND ANALYSIS

A. Schematic of Energy Efficient CMOS full adder Fig5 Below shows a schematic for Energy Efficient CMOS [4] full adder using and/or, XOR/XNOR and 2:1 MUX by using transmission gate.

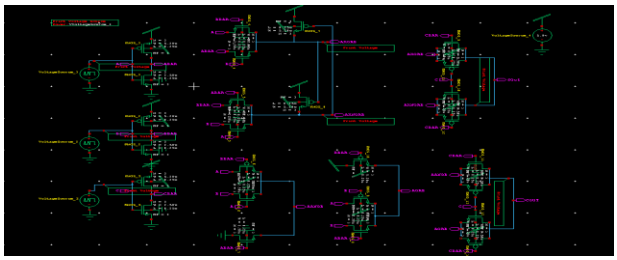

Fig 5. Tanner implementation for EECFA

B. Result for Energy Efficient CMOS Full adderThis section analyzes the Result of energy efficient CMOS full adder shown in Fig6.

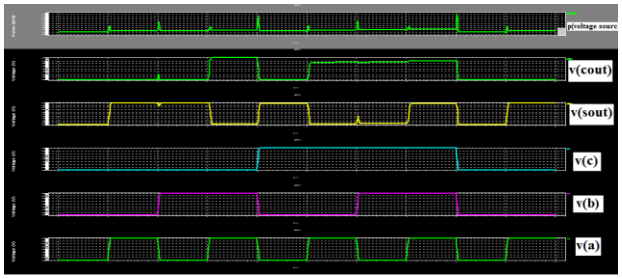

Fig 6. Result for EECFA

6. CONCLUSION

The description of the multiplier circuits turned out well, all multipliers and helper circuits were easily made generic with respect to the number of bits in the inputs. This paper proposed modified reduced complexity Wallace Multiplier with reduced power consumption and area by using Energy Efficient CMOS Full Adder at the place of conventional Full adder. From the literature view it can be notify that proposed multiplier reduced power and total number of gate count i.e. reduced area.

7. REFERENCES

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