

Design and Simulation of DAC on the basis of Capacitor Array

Pranit G. Konde
M.Tech IVth sem. (VLSI),
B.D.C.E, Sevagram
Nagpur University

R. N. Mandavgane
Associate professor & HOD.
E&TC Dept.B.D.C.E,
Sevagram
Nagpur University

A. P. Bagade
Assistance professor
E&TC Dept.B.D.C.E,
Sevagram
Nagpur University

ABSTRACT

DAC can be basically design on the basis of capacitor array by applying a specific amount of voltage and some circuitries are also included for the proper functioning of the system. The designing of DAC is performed on the basis of capacitor array and the circuits will gives better results. When a DAC is used to decode the binary digital signals, meaningful output appears. The 10 bit digital signals and inverters are used for the specific design and for the efficient and necessary results the capacitors are used which are connected with inverters which are further interconnected with each other to form the final DAC output properly in order to give the better result for the double-tail comparator. And similarly on the basis of this result we can easily design the substitute module which is necessary.

Keywords

DAC, digital-to-analog conversion, Inverter, Capacitors Array.

1. INTRODUCTION

Circuits that interface both analog and digital signals, which is often determined by its Input-referred offset voltage, which is essential for the resolution of high-performance DACs [3].

Digital-to-analog conversion is a process in which signals having a few defined levels or states i.e. digital in nature which are converted into the signals which having a theoretically infinite number of states i.e. analog in nature. A digital to analog conversion process is a function that converts digital signal data into an analog signal either current or voltage. Unlike analog signals, digital data can be transmitted, Manipulated, and stored without degradation.

Basically, digital-to-analog conversion process is the opposite of analog-to-digital conversion process. Comparator is commonly used in flash as well as SAR-ADC and DAC because of their decision making speed regarding to equipments [1]. In most of the cases, if an *analog-to-digital converter (ADC)* is placed in a communications circuit after a DAC, the digital output signal is identical to the digital input signal. Also, in most applications when a DAC is placed after an ADC, the analog output signal is identical to the analog input signal. Both the DAC and the ADC are of significance in some applications of digital signal processing. Many high speed DAC needs high-speed with small chip area [2]. The intelligibility or fidelity of an analog signal can be mostly improved by converting the analog input signal to digital form using an ADC, then clarifying the obtained digital signal, and finally converting the "cleaned-up" digital impulses back to analog from using a DAC.

2. LITERATURE SURVEY

Brian P. Ginsburg developed a capacitive digital- to-analog converter (DAC), a comparator, and control logic which is called the SAR. To minimize the error between the digital output signal and the analog input signal the control logic switches the DAC using a binary search algorithm. The split capacitor array and comparator, the two analog blocks are design under 65nm CMOS technology. The conventional DAC choice is a binary-weighted capacitor array which is insensitive to stray capacitance. However, the conventional capacitor array uses charge inefficiently during a conversion process. In order to express this, a conversion of a 2-bit capacitor array is presented [4].

Chih-Wen Lu obtained novel resistor-floating-resistor- string digital-to-analog converter (RFR-DAC) architecture with a 10-bit resolution for liquid crystal display (LCD) driver applications. It contains shift registers, input registers, data latches, level shifters, DACs and output buffers, within the column driver. Among these components, DACs and output buffers find out the speed, resolution, voltage swing, and power dissipation of a column driver. Resistor-resistor-string DACs (RRDACs) utilizing two cascaded resistor strings. The first resistor string provides a little equal voltage segments between two reference voltages. A voltage selector chooses two coherent voltages and, then, sends them to the second resistor string for extra fine voltage division. RFR-DAC architecture capable of acquire high linearity and high uniformity [5].

3. PURPOSE OF DAC

1. To convert digital values to analog voltages
2. Performs inverse operation of the Analog-to-Digital Converter (ADC)
3. $V_{out} \propto$ Digital value.

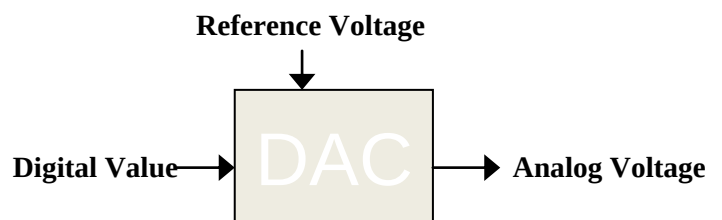


Fig1:- Symbol of DAC

4. DESIGN TOOLS

DAC is fabricated in 90nm CMOS technology in the tanner tool EDA software. Tanner Tools Pro is a software suite for the design, layout and verification of analog, mixed-signal,

RF and MEMS ICs. Tanner Tools Pro consists of fully-integrated front end and back end tools, from schematic capture, circuit simulation, and waveform probing to physical layout and verification.

L-Edit Pro is a comprehensive physical layout and verification system that accelerates design cycles with high performance and an extremely short learning curve. T-Spice Pro, Tanner EDA's design entry and simulation system includes S-Edit for schematic capture, T-Spice for circuit simulation and W-Edit for waveform probing.

In this software we design the module in S-EDIT with the help of given circuitry and the simulation waveform can be check in T-SPICE and after that we can easily check the output which showing different regions. After simulation in T-SPICE the waveform is shown with the specific output with respect to input and it gives the necessary result asrequired and the conversion of digital signal to analog signal takes place.

5. BLOCK DIAGRAM OF DAC

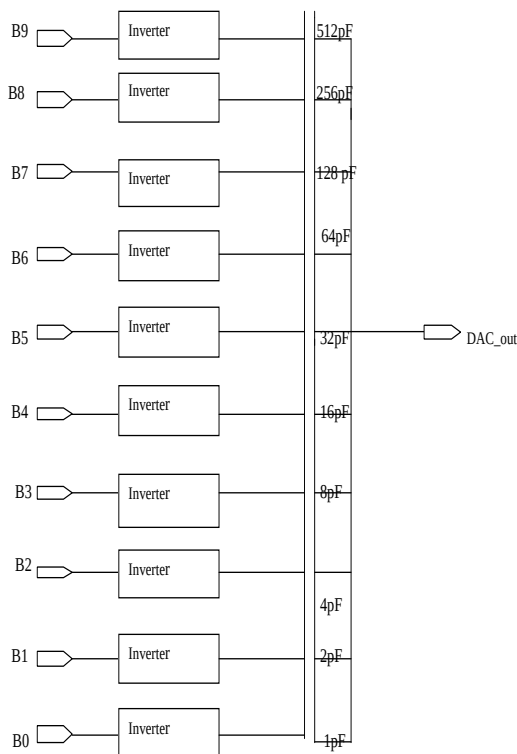


Fig2:- Block diagram of DAC

6. DESIGNING OF DAC

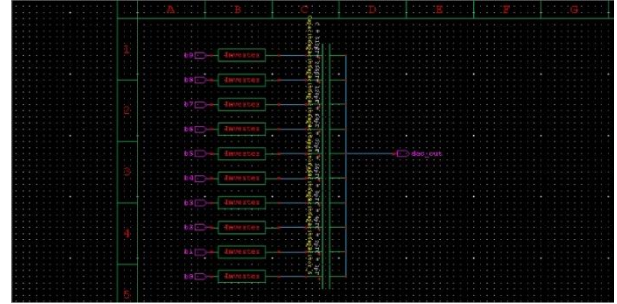


Fig3:- Design of DAC in Tanner Tool

7. WORKING OF DAC

10 bit digital input signals from B0-B9 are used for the designing of DAC and inverter gets connected to every input bit. It brings into inversion process and gives analog output which varies inversely. It means that if the input is low then the output becomes high and on the other hand if the input is high then the output becomes low which means that output is inversely proportional with the input shows the conditions given below.

$$I/P \text{ LOW} = O/P \text{ HIGH}$$

$$I/P \text{ HIGH} = O/P \text{ LOW}$$

Capacitor is used to balance the final output of the circuit and output becomes varies with respect to input. The capacitors are used according to the 10 digital input signals and the ranging of capacitor is from 1pF-512pF. With every input bit from descending order the value of capacitor increases with each input signals. This condition shows that output is directly proportional with the input.

The design of DAC using the capacitor array is important for the double-tail comparator in order to provide the proper supply voltage and also to achieve and optimized the performance of the resulting parameters. Capacitor circuits are used to provide accurate voltage gain. A switched capacitor is an electronic circuit element used for discrete time signal processing. It works by moving charges into and out of capacitors when switches are opened and closed. The use of capacitor array in current design gives the stable output.

8. TABLE 1:

Digital Input Code				Analog Output Voltage
Bit 3	Bit 2	Bit 1	Bit 0	(V)
0	0	0	0	0.000
0	0	0	1	-0.625
0	0	1	0	-1.250
0	0	1	1	-1.875
0	1	0	0	-2.500
0	1	0	1	-3.125
0	1	1	0	-3.750
0	1	1	1	-4.375
1	0	0	0	-5.000
1	0	0	1	-5.625
1	0	1	0	-6.250
1	0	1	1	-6.875
1	1	0	0	-7.500
1	1	0	1	-8.125
1	1	1	0	-8.750
1	1	1	1	-9.375

9. OUTPUT WAVEFORM

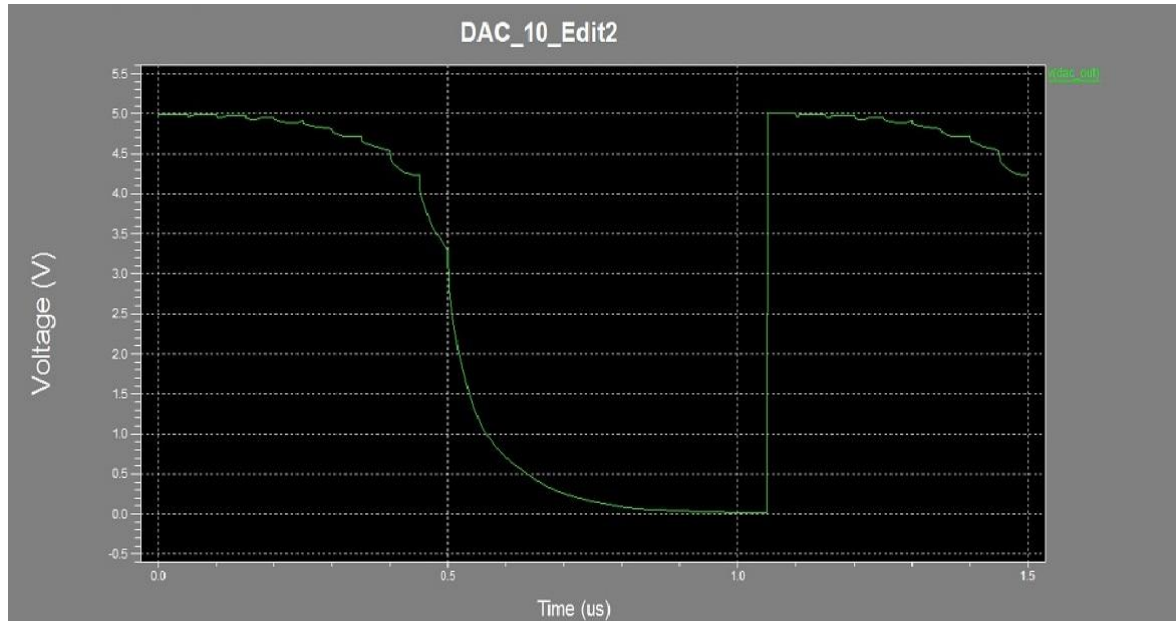
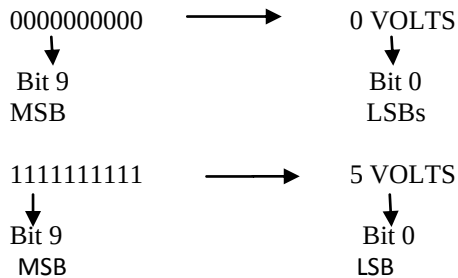


Fig 4:Output Waveform

10. CONVERSION CALCULATIONS

Digital to Analog conversion involves transforming the computer's binary output in the form of 0's and 1's (1's Typically = 5.0 volts) into an analog representation of the binary data. If we are using a 10-bit converter, the binary representation is 10-bit binary number which can take on 2^9 or 512 different values. If our voltage range is suppose to be 0 - 5 volts, then



11. RESULT

From the above output waveform of DAC, it is clear that the digital signals are discrete in nature and the analog signals are continuous in nature and the result is shown in the waveform. The digital signals decreases from high to low value and at the same time by using a capacitor array design the analog input increases from low to high value which affect on the analog output. This indicates that the output is stable with respect to input.

12. CONCLUSION

We conclude that, the designing of DAC on the basis of capacitor array is often easy and more efficient. This work uses the capacitor array because it has both the lowest switching energy and does not require an extra clock phase that would limit high speed operation. It gives better result while using capacitor array for the stable output which is necessary for the circuit. This strategy gives high speed and with increasing value of capacitor the output becomes more stable.

13. REFERENCES

- [1] Samaneh Babayan-Mashhadi, and Reza Lotfi, "Analysis And Design of a Low-Voltage Low-Power Double-Tail Comparator" in. *proc. IEEE. Int. Midwest Symp. Circuits syst. papers*, vol.22, pp.1063-8210, Feb.2014.
- [2] P. M. Figueiredo and J. C. Vital, "Kickback noise reduction technique For CMOS latched comaparators," *IEEE Trans. Circuits Syst. II, Exp.Briefs*, vol. 53, no. 7, pp. 541-545, Jul. 2006.
- [3] J. Li and U. Moon, "High-speed pipelined ADC using Time-shifted CDS technique," in *Proc. IEEE Int. Symp. Circuits Syst*, vol. I May 2002, pp. 909-912.
- [4] Masaya Miyahara, Akira Matsuzava, "A Low-Offset Latched Comparator Using Zero-Static Power Dynamic Offset Cancellation Technique," *IEEE A Solid-state Circuits*, Vol. 56, no. 5, pp. 911-919, May 2009.
- [5] Brian P. Ginsburg, and Anantha P. Chandrakasan, "500-MS/s 5-bit ADC In 65-nm CMOS with Split Capacitor Array DAC," *IEEE A Solid-state Circuits*, vol. 42, no. 4, pp. 0018-9200, April 2007.
- [6] Chih-Wen Lu, Ping-Yeh Yin, and Ching-Min Hsiao, "A10-bit Resistor-Floating-Resistor-String DAC (RFR-DAC) for High Color-Depth LCD Driver ICs," *IEEE A Solid-states Circuits*, vol. 47, no. 10, October 2012.
- [7] A. Ali and K. Nagaraj, "Correction of operational amplifier gain error in Pipelined A/D converters," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. I, May 2001, pp. 568-571.
- [8] B. P. Ginsburg and A. P. Chandrakasan, "An energy-efficient charge recycling approach for a SAR converter Withcapacitive DAC," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2005, vol. 1, pp. 184-187.
- [9] C.-H. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6mm," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1948-1958, Dec. 1998.

- [10] G. Promitzer, "12-bit low-power fully differential switched capacitor Noncalibrating successive approximation ADC with 1 MS/s," *IEEE J. Solid-State Circuits*, vol. 36, no.7, pp. 1138–1143, Jul. 2001.
- [11] J.-K. Woo, D.-Y. Shin, D.-K. Jeong, and S. Kim, "High-speed 10-bit LCD column driver with a split DAC and a Class-AB output buffer," *IEEE Trans. Consum. Electron*, vol. 55, no. 3, pp. 1431–1438, Aug. 2009.
- [12] M. J. Bell, "An LCD column driver using a switch Capacitor DAC," *IEEE J. Solid-State Circuits*, vol. 40, no.12, pp. 2756–2765, Dec. 2005.
- [13] C.-W. Lu, C.-C. Shen and W.-C. Chen, "An area-efficient fully R-DAC-based TFT-LCD column driver," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 10, pp. 2588–2601, Aug. 2010.
- [14] Y.-C. Sung, S.-M. So, J.-K. Kim and O.-K. Kwon, "10 bit source Driver with resistor-resistor-string digital to analog converter," in *SID Int. Symp., Seminar & Exhibition Dig. Tech. Papers*, May 2005, vol. 36, no.1, pp. 1099–1101.