Design and Verification of Carry Select Adder in 180nm CMOS Technology

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ABSTRACT
Adders are the basic unit of arithmetic operations. Due to the rapidly growing mobile industry not only the faster arithmetic unit but also reduced area and low power arithmetic units are needed. The CMOS carry select adder (CSLA) consists of two sets of ripple carry adder (RCA) and the modified CSLA replaces one set of RCA with a binary to Excess One (BEC) converter. The modified carry select adder architecture has developed using Binary to Excess-1 converter (BEC). In this paper design of 16 bit modified carry select adder has been designed.

Keywords
Area efficient, CSLA, low power and BEC.

1. INTRODUCTION
In recent years, the increasing demand for high-speed arithmetic units in micro-controllers, image processing units and DSP chips has paved the path for development of high-speed adders as addition is an most important operation in almost arithmetic unit, also it acts as the basic block for synthesis of all other arithmetic computations .To increase robustness of systems and battery life, area and power are the important parameter of concern. Even in servers and computers (PC), power dissipation is an important design parameter. In today's scenario, Design of area-efficient and power-efficient high-speed logic systems are the one of the crucial areas of research in VLSI design. Addition is one of the fundamental arithmetic operations and nearly 8.72 % of all the instruction in a typical processor is addition.. Low power area-efficient, and high-performance VLSI systems are increasingly used in portable and wireless devices, multi-standard wireless receivers, and biomedical instrumentation An adder is the main component of an arithmetic unit. A complex digital signal procesor (DSP) system involves multiple adders. An power efficient adder design essentially improves the performance of a complex DSP system Amongst the different building blocks of a DSP system, a adder is an most essential component that has a significant role in both speed and power performance of the entire system. Therefore, to improve the performance of DSP SoCs, designing of high performance and power efficient as well as delay efficient adder is crucial. So Carry Select Adder (CSA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions.

Since, addition dominates the execution time of most DSP algorithms therefore fast adder is much desired .With an ever-increasing quest for greater computing power on battery-operated cell phone devices, design emphasis has shifted from optimizing delay time, area size to minimizing power dissipation while still maintaining the high performance. The low power and high speed adder

can be implemented with different logic style. As we know billions of instructions per second are performed in microprocessors & microcontrollers. So, speed of operation is the most crucial constraint to be considered while designing adder. The demand of reduce power high speed circuits are in demand with the increasing growth in electronic system and the loss of information is not acceptable as with single loss of a bit information the energy loss is kTlog2 joules/bit. Reversible logic can be of major interest to design low power arithmetic and data path units for digital signal processing applications, such as the designs of low power adders, multipliers etc.

Reversible logic has received great attention in recent years due to its ability to reduce the power dissipation Reversible logic circuits find wide application in low power digital design Reversible logic is very essential for the construction of low power, low loss computational structures which are very essential for the construction of arithmetic circuits used in quantum computation, nano technology and other low power digital circuits.

2. LITERATURE REVIEW
Bedriji 1962 proposes a new carry select adder [3] that the problem of carry propagation delay is overcome by independently generating multiple radix carries and using these carries to select between simultaneously generated sums. Akhilash Tyagi 1993 introduce a design of carry select adder to generate carry bits with block carryin 1 from the carries of a block with block carryin 0 [8]. Chang and Hsiao 1998 [4] propose that instead of using dual carry ripple adder a carry select adder scheme using an add one circuit to replace one carry ripple adder. Youngioon Kim and Lee Sup Kim 2001 [6] introduces a multiplexer based add one circuit is proposed to reduce the area with negligible speed penalty. Yajuan He et al 2005 planned an area efficient square root carry select adder scheme based on a new first zero detection logic [5]. Ramkumar et al 2010 proposed a BEC method to reduce the maximum delay of carry propagation in final stage of carry save adder [2]. Ramkumar.et.al in 2011 proposed [11] BEC technique which is a simple and efficient gate level modification to significantly reduce the area and power of existing CSLA. Padma Devi et al 2010 proposed [7] a modified carry select adder designed with different stages which has reduces the area and power consumption.

2.1 Carry Select Adder

CMOS carry select adder consists of two sets of ripple carry adders. CMOS Ripple-carry select adders are the simplest and most compact full adders, but their concert is limited by a carry that must propagate from the least - significant bit to the most- significant bit. The various 4bit, 8bit, 16bit, 32bit, 64bit and 128-bit CSLA can also be developed by using ripple carry adders. The quickness of a carry select adder can be improved upto 40% to 90%, by performing the additions in equivalent, and reducing the maximum carry delay. Fig 3 shows the Regular structure of 16-bit SQRT CSLA. It includes many ripple carry adders of variable sizes which are divided into groups. set 0 contains 2-bit Ripple Carry Adder which contains only one ripple carry adder which adds the input bits and carry and result in the form of sum [1:0] and the carry out. The carry out of the set 0 which acts as the selection input to mux which is in set 1, selects the product from the corresponding RCA (Cin=0) or RCA (Cin=1). Similarly the remaining groups will be selected depending on the Carry from the previous groups. In CMOS CSA, there is only one RCA to perform the addition of the LSB. The remaining bits (other than LSBs), the sum is calculated by two RCAs corresponding to the one assuming a carry -in of 0, the other a carry-in of 1 within a group. In a set, there are two RCAs that takes the same data inputs but different Cin. The uppermost adder has a carry-in of 0, the lower adder a carry-in of 1. The actual Cin from the earlier sector selects one of the two RCAs. That is, as revealed in the Fig.3, if the carry is 0, the sum and carry-out of the upper RCA is selected, and if the carry-in is 1, the sum and carry-out of the lower RCA is selected. For this standard CSLA architecture, the functioning code, for the Full Adders and as per our requirement the Multiplexers of different size were designed.

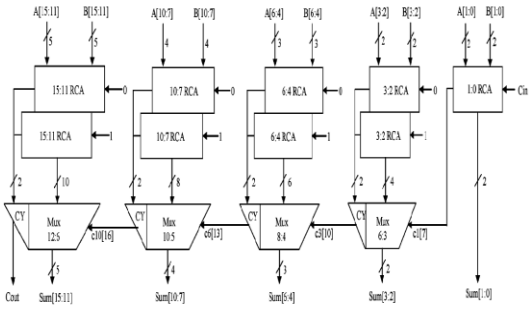

Fig 1:-Regular 16- bit CSLA (Ref-1)

- The problem in CSLA design is that if the quantity of full adders is increased then the circuit complexity also increases.
- The quantity of full adder cells are more thereby power consumption of the design also increases
- Number of full adder cells doubles the area of the design also increased.

3. RESULTS

Figure1 shows the mux design using pass transistor logic. It will be used in auxiliary stage of CSA. Design require 6 Mosfet having width 2.5um and length 250nm.

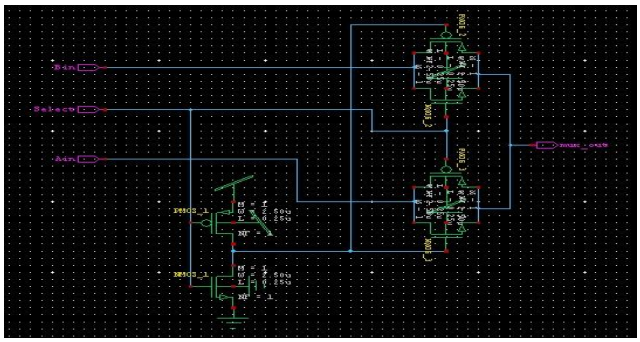

Fig.1 Schematic of MUX for 4bit CSLA

Figure 2 shows 16bit CSA with A[15:0] and B[15: 0] with corresponding output of 16 bit i.e Out[16:0].

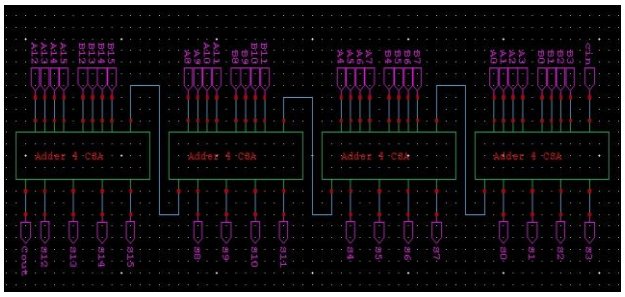

Fig.2 Schematic of 16 bit CSLA schematic

Figure 3 is a single bit carry sum generator with 28 mosfet designed with pass transistor logic. Device is having width 2.5um and length 250nm. Design is showing two inputs A and B and respective output is Sum and carry.

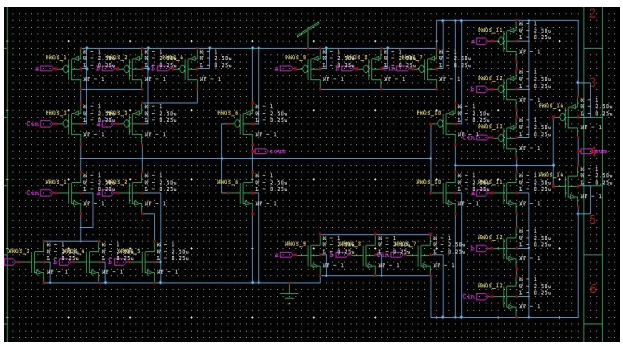

Fig.3 Schematic of Carry sum generator for 1 bit csla

Figure 4 is the output waveform for 4 bit CSLA structure. Input is varied from 0000 to 1111 and corresponding output is observed at each instant of time. Waveform is seen in W-edit window of tanner.

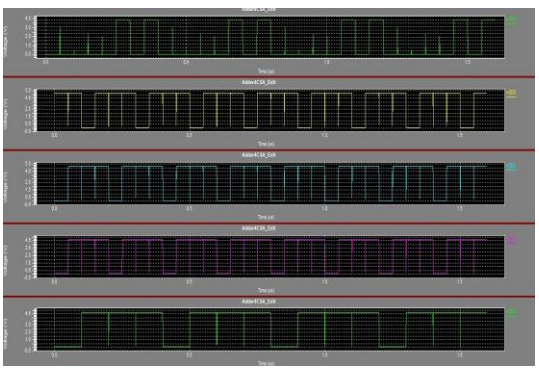

Fig.4 Waveform of Output waveform of 4bit csla

Figure 5 is the output waveform for 16 bit CSLA structure. Input is varied from "0h0000" to "0h1111" and corresponding output is observed at each instant of time. Waveform is seen in W-edit window of tanner.

Table:1Power and technology comparison table

Adder	Power	Delay	Total Nb Of Gate Count
1 Bit CSA	2.131×10^-4W	0.957ns	28
4 Bit CSA	8.130×10^-4W	0.80ns	112
16 Bit CSA	3.42×10^-3W	0.998ns	448

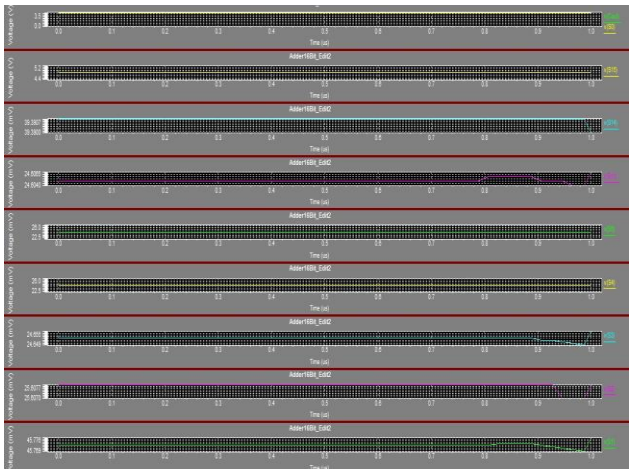

Fig.5 Waveform of Output waveform of 16bit CSA.

4. CONCLUSION

Digital Signal Processing IC require less delay and low power dissipation without compromising the speed. Reducing the delay of the adder is a key to satisfy overall power budget. One of the primary functions of most computer systems is to perform a great number of mathematical operations such as addition at a much faster speed. Since a computer devote a considerable full amount of its processing time to performing mathematical operations specially addition, an improvement in the speed of a processor of the computer for performing a particular type of operation will increase the overall speed of operation. The various types of adder are verified, tested and implemented on Field Programmable Gate Array, but for ASIC it may be implemented in VLSI. Using Reversible logic in carry select adder, delay will get reduce and the speed of execution can be increased. The proposed carry select adder using reversible logic is not implemented yet at CMOS process technology

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