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A Review on Design a Low Power Flip-Flop based on a Signal Feed-through Scheme

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ABSTRACT
Flip-flops and latches are the most important elements of a design for both a delay and energy point of view. In many electronics design low power consumption is basic need in most of the applications. The energy performance requirements enhance the most designers of next generation system towards the least possible power consumption. The power consumption is basically reduced by scaling of a power supply voltage.Flip flops typically consumes more than 50% of random logic power in the SoC chip, because of redundant transition of internal node. A low power flip flop design featuring pulse triggered structure based on signal feed-through scheme is presented which successfully solves the long discharging path problem in a various pulse triggered flip flop design and achieve a better power performance and better speed. In this paper we have studied all the major techniques to achieve a low power flip flop and presented their comparison.

Keywords
Flip-Flops, low power, pulse triggered, leakage power, pipelining.

1. INTRODUCTION
Flip-flops (FFs) are the basic data storage elements used extensively in all kinds of digital designs. Particularly, digital designs nowadays often use intensive pipelining techniques and built many FF-rich modules such as register file, shift register, and first in first out. Traditionally, the demand for high performance was accessed by increasing clock frequencies with the help of technology scaling. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is nearly 50% of the total system power. FFs, thus, consumes a significant portion of the chip area and power consumption to the overall system design [9], [10].Pulse-triggered FF (P-FF), having a single-latch structure, is more popular than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. Along with its speed advantage and simple circuitry P-FF helps tominimize the power consumption of the clock tree system. A P-FF consists of a pulse generator for strobe signals and a latch for data storage. The latch acts like an edge-triggered FF, if the triggering pulses are sufficiently narrow. Since because of single latch structure, design of P-FF is simpler in respect to circuit complexity. This leads to a higher toggle rate for high-speed operations [11]–[12].

Pulse generation circuitry requires delicate pulse width control to deal with possible variations in process technology and signal distribution network.. To obtain balanced performance among power, delay, area and speed, design space exploration is also a widely used technique [8]–[14].

Depending on the method used for pulse generation, P-FF designs can be classified as implicit or explicit [2]. In an implicit-type P-FF, the pulse is generated inside the flip flop;the pulse generator is a part of the latch design while it suffers a long discharging path with delayed timing operation. In an explicit-type P-FF, the pulse are generated externally, the designs of pulse generator and latch are separate. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. This is because the former merely controls the discharging path while the latter needs to physically generate a pulse train and consumes more power. In pulse flip flop the delay discrepancy in latching data '1' and '0' is observed which shortenthe delay by introducing input signal directly to the internal node of latch design which result in increasing data transition speed and power delay product(PDP) performance. As the feature size of CMOS technology process decreases the more transistors, the more switching and the more power dissipated in the form of heat or radiations. Most of the researchers have worked on low power flip-flop design, but they are mostly focused on one or a few types of flip-flops architecture or applications. The need for comparing different designs and approaches is the main motivation for this paper.

2. ARCHITECTURES OF LOW POWERFLIP FLOPS DESIGN

2.1 Conditional discharge flip-flop
In [1] the author classified this flip-flop architecture into two categories i.e. conditional pre-charge and conditional capture technologies. This classification is based on how to prevent or reduces the redundant internal switching activities.

Fig. 1 shows the conditional discharge technique, is proposed in [1] for both implicit type and explicit type pulse-triggered flip-flops without the problems associated

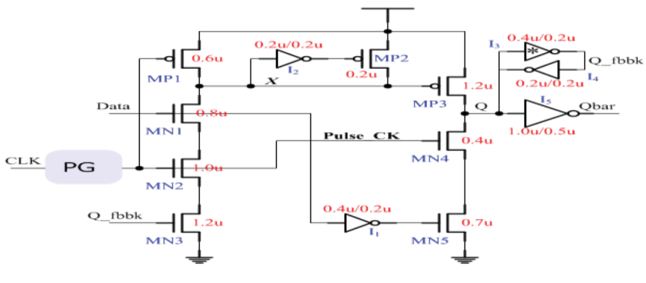

Figure1. Conditional Discharge-Flip-Flop ref [5]

with the conditional capture technique. In this technique, the extra switching activity is reduced by controlling the discharging path when the input is stable HIGH and, therefore, the name given Conditional Discharge Technique.Therefore the conditional discharge is introduced to eliminate the switching activity at the internal nodes of flip flop. The conditional discharge technique used in implicit type of flip flops design. Parameters and the reference values are illustrated in table 1.

Table1. Parameters for CD-FF

Sr. No.	Parameters	Reference Value
1.	Technology	180nm CMOS
2.	Simulation	HSPICE
3.	Supply Voltage	1.8V
4.	No. of Transistors	28
5.	Delay (D-Q)	185ps
6.	Power	20.2µw

2.2 Static dual edge triggered flip-flop (scdff)

In [2] the author proposed a new static dual edge triggered flip flop which gives minimum switching activity at the internal node of flip flop.

The main architecture of the SCDFF shown in Fig. 2 consists of two static stages. SCDFF basically reduces the internal switching activity by removing the pre-charging at node X and makes use of the inverted output QB as a discharge control signal. This helps in minimizing the power dissipation, regardless of any input data activity. Also, with the aim to reduce the capacitive load at node X, node X drives only the output pull-up transistor M5 in the second stage. In [2] the author tried to eliminate the dynamic pre-charging (i.e. static mode) of the pull-up transistor, M1.

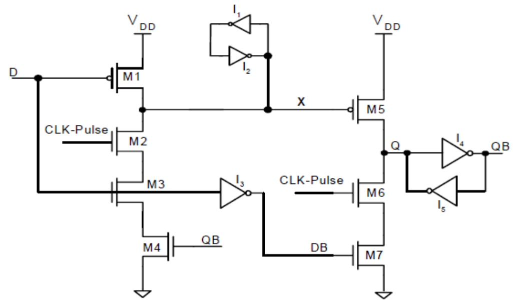

Figure2. Static-Controlled Discharge Flip-Flop (SCDFF) ref [2]

Following CDFF [1], the output signal, QB acts as a discharge control path of stage one for discharging node X, to minimize extra switching activity when input D is at a stable high. As a result, morepower saving can be saved since the circuit is now statically controlled rather than dynamically controlled.The parameters and the reference values are illustrated in table 2.

Table2. Parameters for SCDFF

Sr. No.	Parameters	Reference Value
1.	Technology	180nm CMOS
2.	Simulation	SPECTRE
3.	Supply Voltage	1.8V
4.	Clock frequency	250 Mhz
5.	Delay (T_{l-h})	148ps
6.	Power	290µw

2.3 Pulse triggered (p-ff) flip-flop

In [5] the author proposed the method of low power design pulse triggered flip flop based on signal feed through scheme for improving the delay.Here the signal feed through scheme uses the pulsed generator circuitry which generates the pulse of sufficient width which is useful in driving the signal from input node directly to the output node. The [5]flip flop is distinct from the previous flip flop architecture design. The changes made in [5]used p-Mos transistor in the first stage of flip flop latch structure. The charge keeper circuit is eliminated in [5] design which makes circuit simple. The MNx pass transistor employed for a discharging path, the role of MNx pass transistor is for providing extra driving to node during 0 to 1 data transition and for discharging node Q during "1" to "0" transition of data. The extra element introduced is an n-MOS pass transistor for supporting signal feed through scheme. Technology used is TSMC 90-nm CMOS process. The pulsed width is most important factor in latching of data in

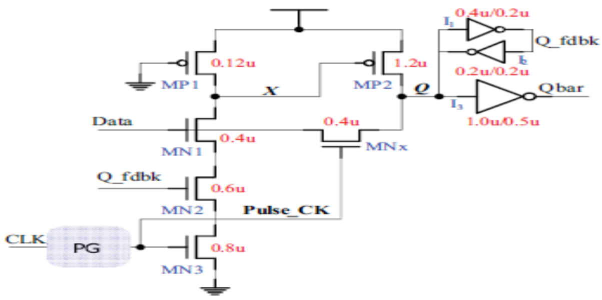

Figure 3 Schematic of P-FF design ref [5]

to the pulsed flip flop for low power consumption. The pulsed flip flop makes signal feed through technique to improve this delay. The architecture of a pulsed (P-FF) flip flop design is illustrated in fig.3

Table3. Parameters for SCDFF

Sr.No.	Parameters	Reference Value
1.	Technology	TSMC 90-nmCMOS
2.	Simulation	HSPICE
3.	Supply Voltage	1.8V
4.	No. of transistors	24
5.	Delay (D-Q)	109.1ps
6.	Power	30.09 µw

The parameters and the reference value are illustrated in table 2.

2.4 Explicit pulse data close output (ep-dcoff) flip-flop

For the high-performance applications, such as the critical paths of a circuit design, for obtaining a smaller flip-flop delay is important while power consumption isa secondary concern [18]. The fast data-to-Q delay ofthe pulsed semi dynamic flip-flops, however, comes at the expense of significant power consumption. The main important reason for this high power consumption is the dynamic nature of the flip-flop, the power may be consumed in the dynamic stage due to the precharging and evaluate cycle even when the input is maintained constant.

An explicit-pulsed, hybrid semi dynamic flop (ep-DCO)schematic in Figure 4.

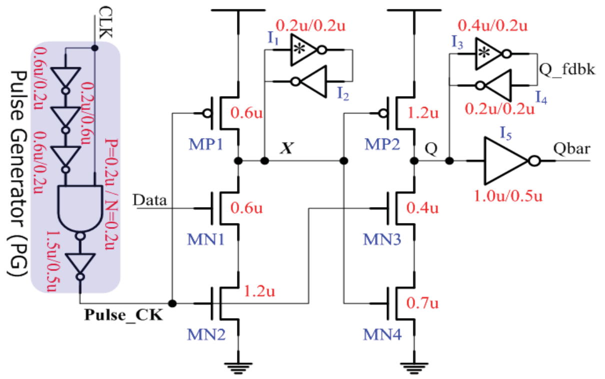

Figure 4 Schematic of EP-DCO FF design ref [5]

The explicit pulsed data close output does not offer any performanceadvantage over implicit-DCO, and consumes more energy due to theexternally generated pulse. However, the pulse generator power consumption can be significantly minimized by sharing a single pulse generator among a group of flip-flops.Thus performance of the bothip- DCO and ep-DCO with shared pulse generator gives the best among all semidynamic flip-flop as far as of speed and critical paths is concerned. PF-FFs, in terms of pulse generation, can be classified as an implicit type and explicit type. In an implicit type P-FF, the pulse is generated inside of flip flop and is a part of the latch design and no explicit pulse signals are generated.

In an explicit type P-FF, the pulse is generated outside the flip flop, the pulse generator circuit and the latch are separate [5]. The implicit type P-FFs are generally more power-economical without generating pulse signals externally However, they suffer from a longer discharging path, which leads to inferior timing characteristics.

While in Explicit pulse generation, in contrary, offers a more power consumption but the logic separation from the latch design gives the a unique speed advantage for flip flop design. The power consumption and the complexity of design can be effectively reduced if one pulse generator is shares a group of FFs.The explicit Pulse-Flip Flop design, named data close to-output (ep-DCO) [5]. It consist of a NAND logic based pulse generator and a semi dynamic true-single-phase-clock (TSPC) structured latch design. In this P-FF architecture, the inverters I3 and I4 are used for latching of data, and inverters I1 and I2 are used for holding the internal node *X*. The delay of three inverters determines the pulsed width; this design suffers from a serious drawback i.e., the internal node *X* is discharged on every rising edge of the clock in spite of the presence of a static input “1.” This gives rise to large switching power dissipation[5].

3. APPLICATIONS

- Low power flip flops are used in level Convertors.
- In Clocking System.
- In Counters.
- In Shift registers.

4. CONCLUSION

This paper presented different architectures of a low power flip flop structure. In this paper we have studies the basic architectures of a Flip flop design of SDFF, SCDFF, EP-DCO FF and Pulsed triggered flip flop for low power consumption with their comparative results. The performance of Pulsed triggered flip flop is more efficient than the CDFF,SCDFF, EP-DCO FF.Pulse triggered flip flop design and achieves a better power performance and better speed. In future we minimize power consumption of p-FF by using adiabatic logic design.

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