# Convolutional Encoder Design using 16 Bit Vedic Multiplier on High Speed Revolution

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## ABSTRACT
In mathematics, multiplication is the most commonly used operation. This paper explores the design approach of a convolution encoder using vedic multiplier which leads to improve delay and faster speed. Here, the efficiency of Urdhva Triyagbhyam Vedic method for multiplication which strikes a difference in the actual process of multiplication itself. It enables parallel generation of partial products and eliminates unwanted multiplication steps. This algorithm follows a fast multiplication process and achieves a significantly less computational complexity over its conventional counterparts. The coding is in VHDL and synthesis is in Xilinx ISE simulator.

## Keywords
Convolutional Encoder, Multiplier, Urdhava Tiryakbhyam, Vedic Mathematics.

## 1. INTRODUCTION
An encoder is a device that converts information from one format to another, for the purposes of faithful recovery of message bits. The terms encoding is used in reference to the process of analog-to-digital conversion. Convolutional encoding is error correction scheme. This coding scheme is often used in the field of deep space communications and more recently in digital wireless communications. It is very efficient and robust. In most of real time applications like audio and video applications, the Convolutional codes are used for error correction. The cost for the convolutional encoder is expensive for a specified design because of the patent issue. Therefore, to realize an adaptive Convolutional encoder on a field programmable gate array (FPGA) board is very demanding. we concern with designing and implementing a convolutional encoder which is the essential block in digital communication systems using FPGA technology. Convolutional codes offer an alternative to block codes for transmission over a noisy channel. Convolutional coding can be applied to a continuous input stream as well as blocks of data. A simple convolutional encoder is shown in Figure 1.

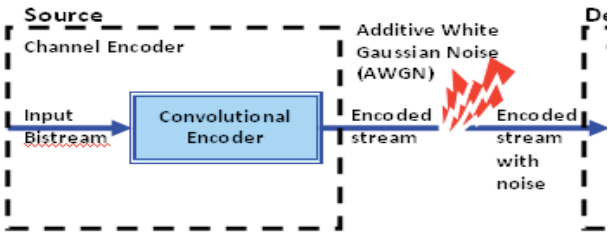


**Figure 1: Convolutional Encoder [15]**

Urdhva tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and Crosswise". To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (5498 × 2314). The conventional methods already know to us will require 16 multiplications and 15 additions. An alternative method of multiplication using Urdhva tiryakbhyam Sutra is shown in Fig. 2. The numbers to be multiplied are written on two consecutive sides of the square as shown in the figure. The square is divided into rows and columns where each row/column corresponds to one of the digit of either a multiplier or a multiplicand. Thus, each digit of the multiplier has a small box common to a digit of the multiplicand. These small boxes are partitioned into two halves by the crosswise lines. Each digit of the multiplier is then independently multiplied with every digit of the multiplicand and the two-digit product is written in the common box. All the digits lying on a crosswise dotted line are added to the previous carry. The least significant digit of the obtained number acts as the result digit and the rest as the carry for the next step. Carry for the first step (i.e., the dotted line on the extreme right side) is taken to be zero .

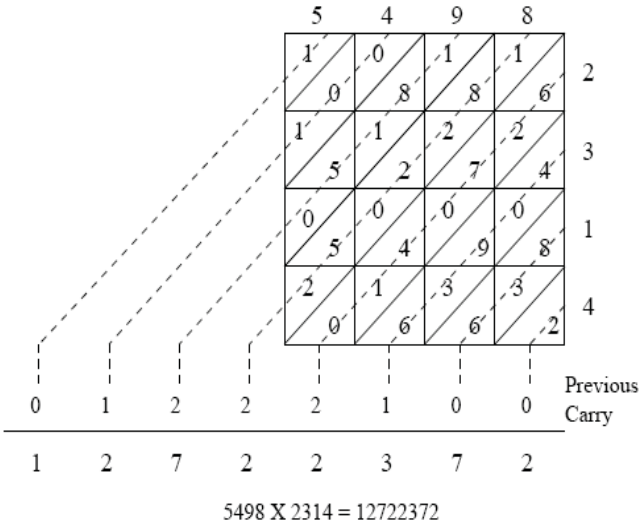


**Figure 2: Alternative Way Of Multiplication By Urdhva Tiryakbhyam Sutra [1]**

### 1.1 Convolution Encoder using Vedic Multiplier
Convolutional codes protect information by adding redundant bits to any binary data. The convolutional encoder computes each n-bit symbol (n >k) of the output sequence from linear operations on the current input k-bit symbol and the contents of the shift register(s). Thus, a rate k/n convolutional encoder processes a k-bit input symbol and computes an n-bit output symbol with every shift register update. Convolutional codes are commonly specified by three parameters; (n,k,m).

n = number of output bits

k = number of input bits

m = number of memory registers

The quantity k/n is called as code rate. it is a measure of the efficiency of the code. Commonly k and n parameters range from 1 to 8, m from 2 to 10 and the code rate from 1/8 to 7/8 except for deep space applications where coderates as low as 1/100 or even longer have been employed. The quantity L is called the constraint length of the code and is defined by

Constraint Length, L = k (m-1)

The constraint length L represents the number of bits in the encoder memory that affect the generation of the n output bits. The constraint length L is also referred to by the capital letter K, which can be confusing with the lower case k, which represents the number of input bits. In some books K is defined as equal to product the of k and m. Often in commercial specifications, the codes are specified by (r, K), where r = the code rate k/n and K is the constraint length. [12]

Convolutional coding has been used in communication systems including deep space communications and wireless communications. Convolutional codes are used as r an alternative to block codes of transmission. Convolutional coding can be applied to a continuous input stream (which cannot be done with block codes), as well as blocks of data. A convolutional encoder is a Mealy machine, where the output is a function of the current state and the current input. It consists of one or more shift registers (DFF) and multiple XOR gates. XOR gates are connected to some stage of the shift registers as well as to the current input to generate the output polynomials.

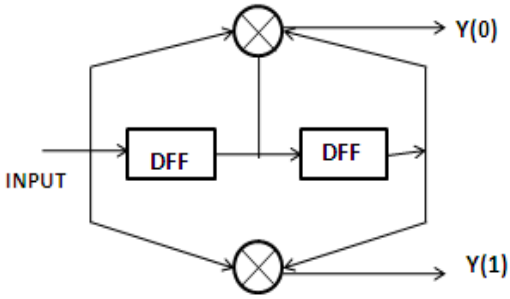


**Figure 3: Convolutional Encoder of Rate [4]**

The encoder in figure 3 produces two bits of encoded Information for single bit of input information, so it is called a rate 1/2 encoder. A Convolutional encoder is generally represented in (n, k, m) format with a rate of k/n, where n is number of outputs of the encoder, k is number of inputs of the encoder, m is number of flip-flops. In this paper, we discuss decoding of convolutional codes generated by a (n,1,m) encoder with the rate 1/n with the number of outputs n=2.

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The above figure 3 shows the Convolutional Encoder with rate =1/2. Convolutional encoder can be described in terms of state table, state diagram and trellis diagram. The figure 4 shows the block diagram of convolution encoder using vedic multiplier.

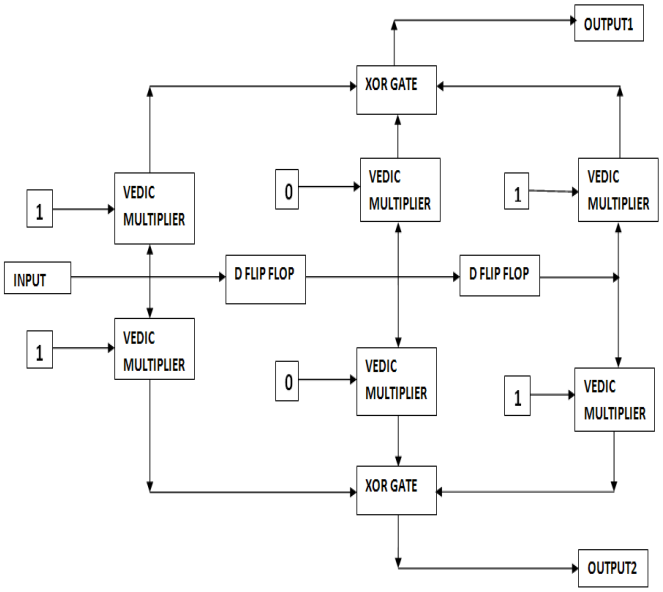


**Figure 4: Block Diagram of Convolution Encoder Using Vedic Multiplier**

## 2. DESIGN AND IMPLEMENTATION

The Vedic multiplier is implemented using VHDL. The synthesis is done using Xilinx Synthesis Tool (XST) available with Xilinx ISE 13.1i and simulation is with Xilinx ISE 9.1i.

### 2.1 Vedic Multiplier for 16x16 Bit

The architecture of 16X16 Vedic multiplier using Urdhva Tiryagbhyam Sutra is shown in Figure 5. The 16X16 Vedic multiplier architecture is implemented using four 8x8 Vedic multiplier modules and two16 bit binary adder stages. The resultant output is given as,

X×Y=(Z3 1-Z1 6)&(Z1 5-Z8)&(Z7-Z0)

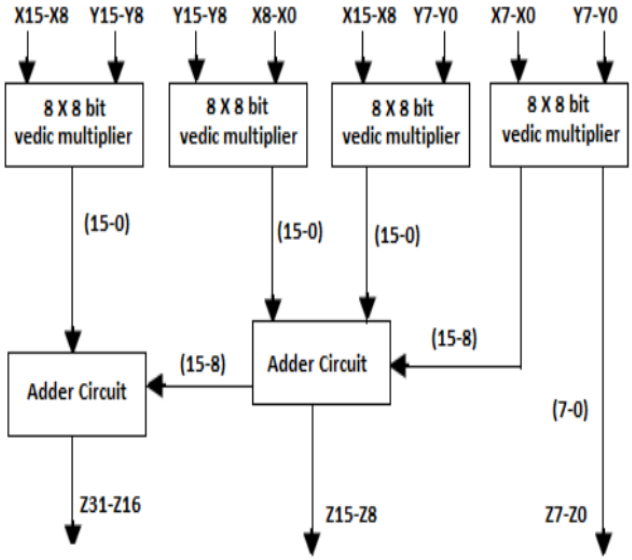


**Figure 5: Hardware Realization of 16x 16 Bit Multiplication Using Urdhava Tirya Kbhyam Sutra [14]**

# 3. SIMULATION RESULTS

## 3.1 Convolutional Encoder Using 16 Bit Vedic Multiplier

*3.1.1 RTL View*

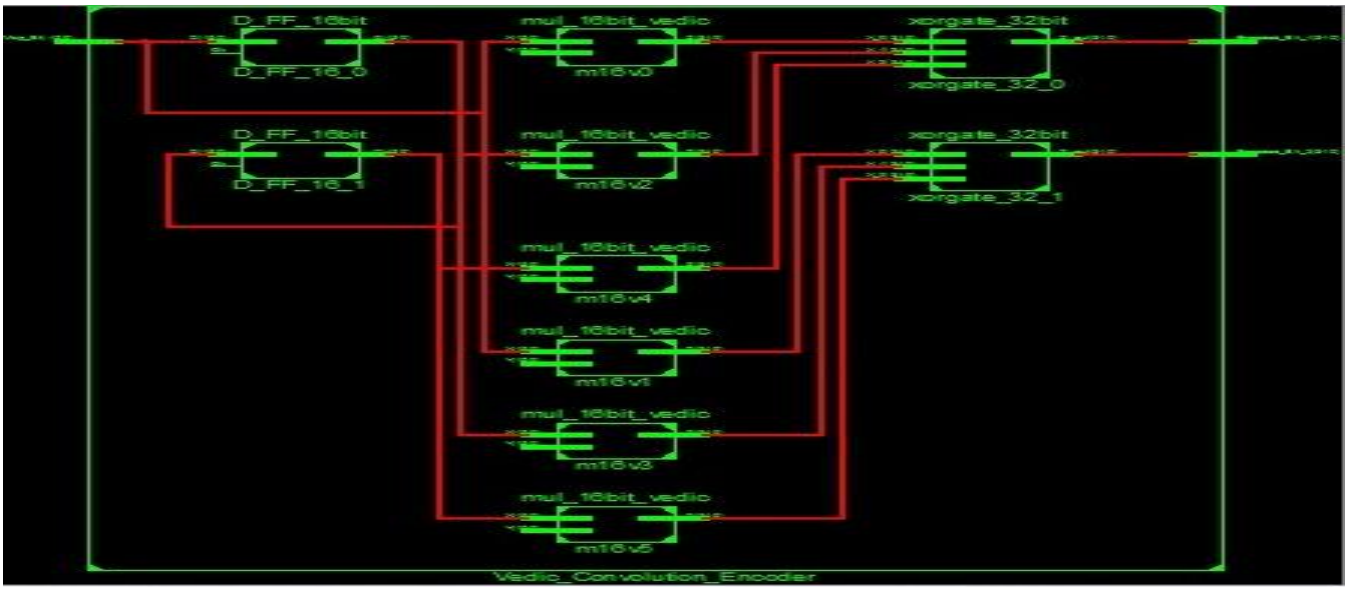


**Figure 6: RTL Schematic of Convolutional Encoder using 16 Bit Multiplier**

*3.1.2 Simulation Result*

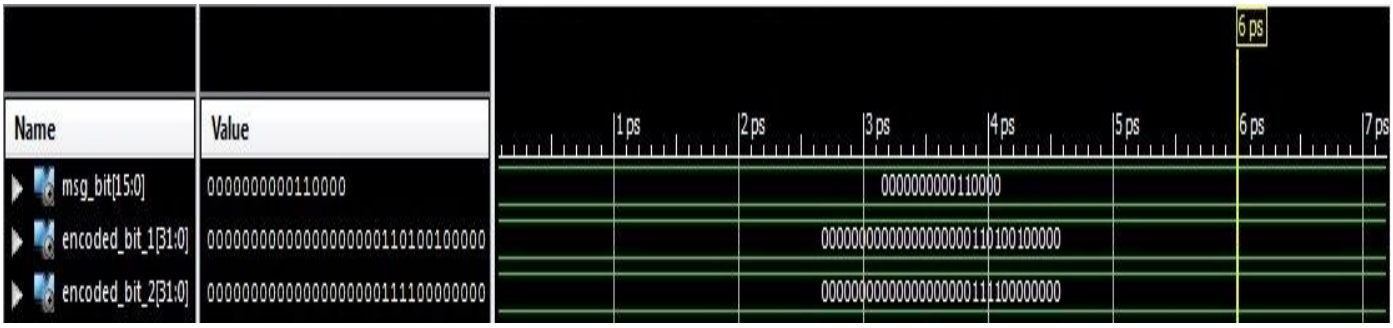


**Figure 7: Simulation Result of Convolutional Encoder Using 16 Bit Multiplier**

The Convolutional encoder for the constraint length of K=16 and code rate of r = 8/16 has been developed and the synthesis is carried out and the simulation results is shown in the figure 7.

**Table No. 1: Synthesis Results of the Codes**

| Vedic multipliers | 4 Bit | 8 Bit | 16 Bit |
|---|---|---|---|
| Constraint Length | 4 | 8 | 16 |
| Code rate | 2/4 | 4/8 | 8/16 |
| Delay | 7.045ns | 22.775ns | 31.491ns |

From the above table, it is clear that if the size of multiplier increases ultimately delay and size of encoder also increases.

# 4. CONCLUSION

In this paper, we have presented the design and simulation of the Convolutional encoder using vedic multiplier. The designs of Convolutional codes are basically encoders which are very important for extremely low error probabilities used at high data rates. For the basic design of the codes can be developed based on code rate and constraint length. This design has been simulated and synthesized using XILINX-ISE.

The advantages of this proposed architecture is efficient in speed and area (1ess resources used, such as less number of multipliers and adders) and is Flexible in design Example, the same architecture can be extended for 16 -bit, 64- bit etc multiplication.

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