Implementing an Application of Data Acquisition System using NIOS –II Soft Core Processor

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ABSTRACT
This paper represents an application of data acquisition system. Its design is based on NIOS II soft core processor. The design is proposed to create and manage the interconnected systems of analog signal to digital embedded platform. NIOS II is a versatile embedded processor that presents high performance and has been created on FPGA. Paper provides the creation of ADC managing block with small involvement of processor hence the complexity reduces and speed up the system performances. Also the proposed deign can added to the other system which requires analog signal.

Keywords
Altera CYCLONE II FPGA, NIOS II Soft Core Processor, SOPC builder.

1. INTRODUCTION
The communication system is performing the very important role in the digital world. In modern electronic systems, signal processing and storage are performed in the digital domain. However, for these systems to interface with the real world, conversion between analog signals and digital signals are mandatory [1].For converting the analog signals to digital signals, an analog to digital convertor (ADC) is required.

A soft-core processor is a microprocessor fully described in software, usually in an HDL, which can be synthesized in programmable hardware, such as Field Programmable Gate Arrays (FPGAs). Soft-core processors implemented in FPGAs can be easily customized to the needs of a specific target application thus demonstrating a potential advantage [2].

Nios II is a 32 bit RISC soft-core processor optimized for implementation in Altera FPGAs. Many architectural parameters of Nios II can be customized at design time, including the data width, register size, cache size, custom instructions and others.[3]

This paper provides development of NIOS-II soft core processor on the Altera Cyclone II FPGA with the external A/D conversion hardware.

The organization of paper in the following section: (2) Overview (2.1) Design architecture (2.2) Analog to Digital converter (2.3) Define ADC (2.4) Implementation (3) Result (4) Conclusion

2. OVERVIEW

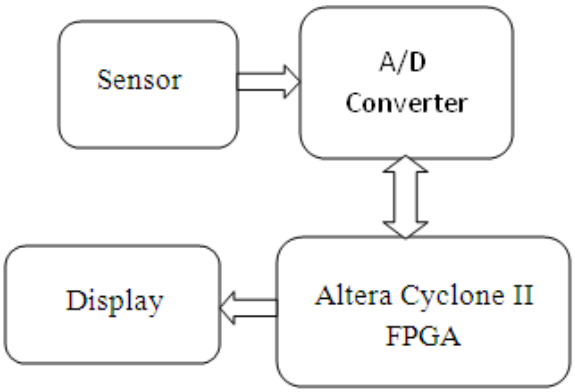


Fig. 1 Block diagram of system design

Our design approach to achieve the aim of the proposed work is based on Altera NIOS II embedded soft core processor that provides a highly reconfigurable devices and having better output response. Altera FPGA provides development platform for soft core processor with their interfaces peripheral component. The design gives interconnect with internal hardware of FPGA and external hardware like Analog to Digital convertor and sensor.

2.1 Design Architecture
The NIOS II embedded processor is 32 bit RISC general purpose configurable soft core processor [1]. The Avalon interconnection bus topology is used for connection of peripheral component [2]. The Altera Cyclone II does not provide on-chip ADC peripheral, therefore there is a need to manage the ADC to some extent. The analog signal under test is fed to an Analog to Digital Converter IC and then with the help of self-generated ADC block in HDL will deal with all the signal handshaking between the NIOS II soft core and the external ADC IC. This will reduce the programming of NIOS II core and externally converted analog signal will be fed to the NIOS II soft core in digital form. And this digital word can be detected by input-output port (GPIO) of the NIOS II core.

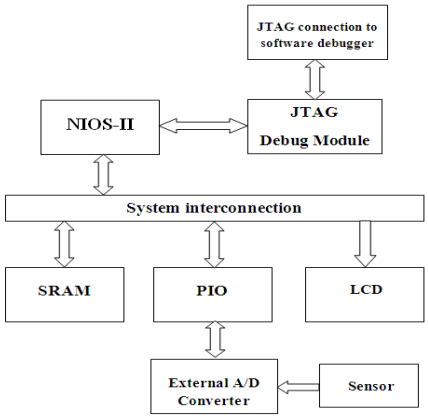


Fig. 2 NIOS II architecture

2.2 Analog to Digital Converter

The HDL code written for Analog to Digital converter is compatible with ADC 0808-8 bit and 8 channel ADC. The channel multiplexer can directly access any of 8 different analog signal, with the help of channel selection pins, that are to be converted. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals [1].

2.3 Define ADC block

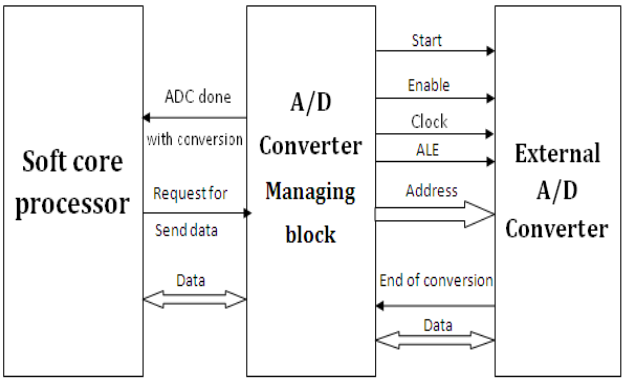


Fig. 3 Proposed ADC managing block

Many times analog signals must be converted into digital signals for storage purpose or input to other application. Embedded system application requires analog signal but due to the programming complexity the processor is isolated from ADC by our HDL block and thus, processor is free for the other application execution.

When the conversion gets over and data is given by ADC, the ADC managing block will simply interrupted the processor and then process takes the charge over ADC data from now on and performs the required task. Here the processor is not consuming a time managing the ADC data and also processor has no need to wait until the conversion gets over and then execute. It can simply perform some other tasks in the meantime. Thus we have achieved the advantage of parallel processing.

2.4 Implementation

For the transferring data through the ADC, we have designed NIOS II processor with necessary peripheral interface. The entire implementation processes are assigned into two stages:

2.4.1 Generation of Hardware System

The NIOS II soft core processor is generated in Quartus II software environment, the software tool provides the System on Programmable Chip (SOPC) builder. Now a day's many applications have requirement of various peripherals. And so they are embedded on single chip therefore the complexity increases.

The SOPC Builder is used for the hardware design of the system. The whole system integrated hardware and software can easily be customized in the user friendly graphical interface, which can greatly improve the efficiency of design [7]. Also it automatically generates optimized interconnect logic to your specifications, saving you from time-consuming [8].

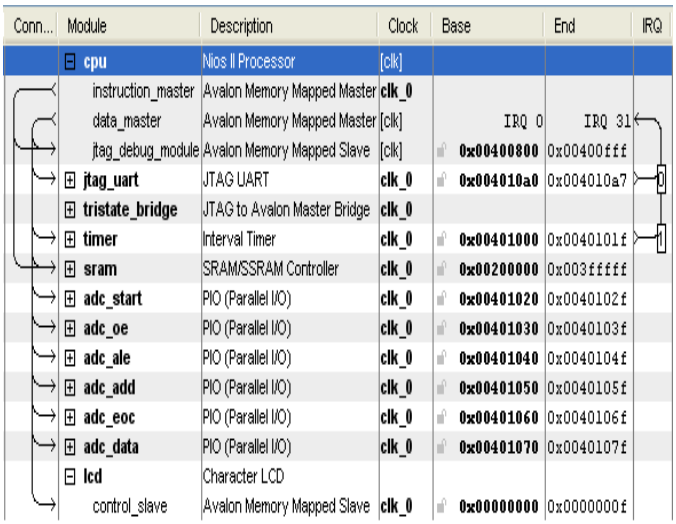


Fig 4. SOPC block generation

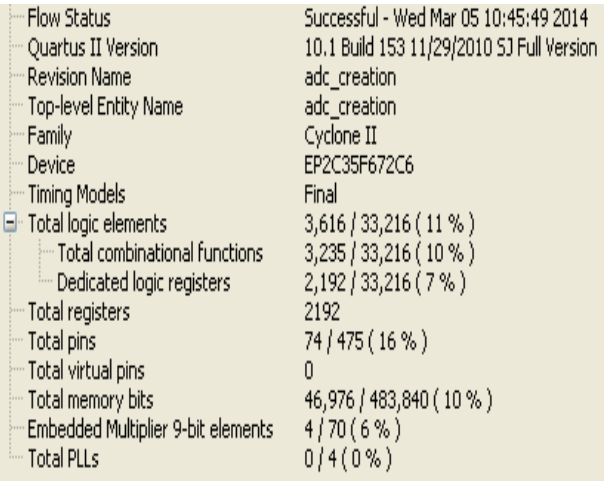
2.4.2 Software Implementation

The software development environment of NIOS II processor that called NIOS II Integrated Development Environment (IDE) consists of a C/C++ compiler [9]. Here the program is written in C language just like we do embedded C coding for any microcontroller when we get it bought from market.

The algorithm for design to accept and manage the converting data from the A/D Converter is done here. Basically we are now writing this C code for NIOS II and thus all the tasks that are required to be performed by NIOS II are defined here. When the NIOS II receives an interrupt from the ADC Managing block, the processor reads it and then uses it as per the requirement.

3. RESULT

We have designed a data acquisition system that manages through the ADC without NIOS II getting directly involved. The huge number of data can be processed by the processor and displayed on LCD.



Flow Status	Successful - Wed Mar 05 10:45:49 2014
Quartus II Version	10.1 Build 153 11/29/2010 SJ Full Version
Revision Name	adc_creation
Top-level Entity Name	adc_creation
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	3,616 / 33,216 (11 %)
Total combinational functions	3,235 / 33,216 (10 %)
Dedicated logic registers	2,192 / 33,216 (7 %)
Total registers	2192
Total pins	74 / 475 (16 %)
Total virtual pins	0
Total memory bits	46,976 / 483,840 (10 %)
Embedded Multiplier 9-bit elements	4 / 70 (6 %)
Total PLLs	0 / 4 (0 %)

Fig 5. Compilation report

The compilation report states that, the logic element is only 11%. Hence this ADC block can directly import to the other design. Therefore the design can improve the performances of that application.

4. CONCLUSION

This paper proposed that use of digital embedded system for the analog communication helps to manage the A/D Converter without any overhead to the processor. These proposed design blocks can be added to more complex design which requires analog signal. By adding these design blocks, speed of the system will increase but it requires certain amount of memory. Due to multi core feature proposed design of A/D managing block and LCD managing block, we are taking the field of Embedded Systems into a new direction.

5. REFERENCES

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