Performance Analysis of Multicarrier PWM Strategy for Seven Level Diode clamped Z-Source Inverter

T.Sengolrajan
AssistantProfessor
Department of EEE
Arunai Engineering College
Tiruvannamalai-606 603
Tamilnadu, India

B.Shanthi
Professor
CISL
Annamalai University
Annamalainagar-608 002
Tamilnadu, India

S.P.Natarajan
Professor
Department of EIE
Annamalai University
Annamalainagar-608 002
Tamilnadu, India

ABSTRACT
This paper investigates the performance analysis of various Multicarrier Pulse Width Modulation strategies with Sinusoidal reference for single phase seven level diode clamped Z-source inverter designed with two intermediate Z-source networks connected between the input source and inverter circuit. The diode clamped Z-source based MLI strategy enhances the fundamental output voltage and reduces the Total Harmonic Distortion (THD). Performance factors such as %THD, V_{rms} where measured and CF, DF of output voltage are calculated for different modulation indices 0.8-1. The results are compared. The simulation results indicate that the use of Z-Source in DCMLI boost 60% of the total output voltage. PODPWM strategy provides low THD and COPWM strategy is found to perform better since it provides relatively higher fundamental RMS output voltage.

Keywords
Diode Clamped Multilevel Inverter (DCMLI), Multicarrier Pulse width modulation, PD, POD, APOD, VF, COPWM, Z-source Inverters

1. INTRODUCTION
Multilevel inverter possesses the advantage of reduced harmonics, high-power and high-voltage cability. The Z-source DCMLI is a kind of single stage multilevel inverter which has the ability of voltage boost. It employs an impedance circuit which connects the power source to the inverter circuit thus providing a unique feature which cannot be obtained in the conventional Voltage Source Inverter (VSI) uses a capacitor and Current Source Inverter uses inductor. The Z-source inverter overcomes the limitations of the traditional VSI and CSI. Inverter (VSI) can only produce an output voltage which is equal to the supply voltage. The maximum output voltage obtainable is limited by the DC bus voltage. Hence Z-source inverter has the useful feature to either buck or boost the batteries voltage to a desired output voltage through shoot through state and non-shoot through state control. Baskar et al [1] described about the switching strategies for pulse-width modulation based Z-source inverter, having simple boost PWM, maximum boost PWM, maximum constant boost PWM, modified-reference PWM, modified space vector PWM, hysteresis current control and sine carrier PWM. Balamurugan et al [2], [3] presented three phase five level Diode Clamped Multilevel Inverter (DCMLI) simulated using various modulating strategies for induction motor load. Bindeshwar Singh et al [4] proposed the modulation methods such as sinusoidal pulse width modulation, multilevel selective harmonic elimination and space-vector modulation. Esfandiari et al [5] described a new configuration for DCMLI based on multi-winding transformer. Fang et al [6] presents a Z-source inverter system and its control for general-purpose motor drives. Gao et al [7] presented five-level Z-source DCMLI attempting to introduce special structures to reduce the number of elements of multilevel Z-source inverter. Kuppuswamy et al [8] presented impedance source Neutral Point Clamped (NPC) three level inverter with reduced number of impedance source networks and clamping diodes for non-linear loads. Comparative evaluation of pulse width modulation strategies for Z-source neutral-point-clamped inverter was proposed in [9]. Mohamed Yousuf et al [10] presented a comparative analysis of several multicarriers PWM techniques like phase-shifted multicarrier PWM and level-shifted multicarrier PWM used for harmonic mitigation in the NPC multilevel Z-Source inverter. Mohamed Yousuf et al [11] presented a comparative THD analysis of NPC multilevel Z-Source inverter using novel PWM control strategies, which is effectively used for harmonic mitigation. Nasiri et al [12] compares APODPWM strategies for a five-level Z-source diode-clamped inverter for on-grid renewable energies applications. Poh Chiang Loh [13] presented the development of two three level cascaded Z-source inverters, whose output voltage can be stepped down or up unlike a traditional buck three-level inverter. Rajaei et al [14] described a Z-source inverter (ZSI) has been used to drive a single-phase induction motor. Yifan Yu et al [15] described novel low-frequency harmonics elimination pulse width modulation strategy, which could greatly reduce low-frequency capacitor voltage ripple for given Z-Source network.

2. SEVEN LEVEL DIODE CLAMPED Z-SOURCE INVERTER
Fig.1 shows the topology of the proposed single phase Z-source based seven level diode clamped inverter, consisting of a split inductor (L1 and L2) and two capacitor (C1 and C2) is connected between the input DC source and switches. The proposed Z-source inverters are controlled with their AC outputs transiting between the seven distinct voltages. They are: $+3V_{dc}$, $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$ and $-3V_{dc}$.To obtain the seven levels, the required switching scheme is given in Table.1.
The presented Z-source inverter is expected to perform better, since performance limitations commonly associated with dead-time delay which was avoided.

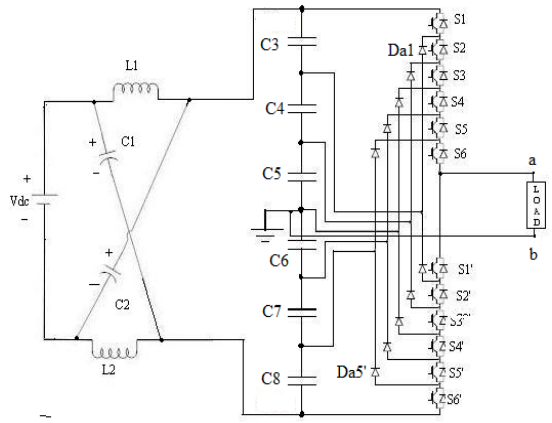

Fig 1: Seven level diode-clamped Z-Source Inverter

Inductors L_1 and L_2 have the same values and Capacitors C_1 and C_2 have the same values. Z-source network is a symmetrical network. The operating states of the Z-source inverter are shoot through zero state and non shoot through zero state. A DCMLI producing m-levels on the output voltage consists of (m-1) capacitors on the DC bus. In this proposed inverter the DC bus consists of six capacitors C_3 ,C_4, C_5, C_6, C_7 and C_8 acting as voltage divider.

Table 1. Switching scheme for Seven level DCMLI

S_1	S_2	S_3	S_4	S_5	S_6	S_1'	S_2'	S_3'	S_4'	S_5'	S_6'	V_{ab}
1	0	0	1	1	0	0	1	1	0	0	1	+3V
1	0	0	1	1	0	0	1	1	0	1	0	+2V
1	0	0	1	0	1	0	1	1	0	1	0	+1V
1	0	1	0	0	1	0	1	1	0	1	0	0V
0	1	1	0	0	1	1	0	1	0	0	1	-1V
0	1	1	0	0	1	1	0	0	1	0	1	-2V
0	1	1	0	0	1	1	0	0	1	1	0	-3V

3. PULSE WIDTH MODULATION STRATEGIES

To synthesize multilevel output AC voltage using different levels of DC inputs, semiconductor devices must be switched ON and OFF in such a way that desired fundamental is obtained with minimum harmonic distortion. There are different types of approaches for the selection of switching techniques for the multilevel inverters. In this paper, various multicarrier PWM techniques like Phase disposition (PD), Phase opposition disposition (POD), Alternative phase opposition disposition (APOD), Variable Frequency (VF) and Carrier Overlapping (COPWM) are proposed for single phase seven levels diode clamped Z-source inverter.

For an m-level inverter (m-1) carriers with same frequency f_c and same peak-to-peak amplitude A_c are used. The reference waveform has amplitude A_m and frequency f_m and placed at zero reference. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched ON. Otherwise, the device switched OFF. In this paper, the frequency ratio m_f =21 and modulation index m_a is varied from 0.8 to 1.

$$m_f = f_c / f_m \quad \text{except for VFPWM}$$

$$m_a = 2A_m/(m-1)A_c \quad \text{except for COPWM}$$

3.1 Phase Disposition (PD) PWM Strategy

The Principle of PDPWM technique is to use the several carriers with single modulating waveform. In phase disposition all the carriers are in phase and the carriers are disposed so that the bands they occupy are contiguous. The modulation wave is centered in the middle of the carrier set. Fig.2 shows the multicarrier arrangement for PDPWM strategy for m_a= 0.8 and m_f = 21.

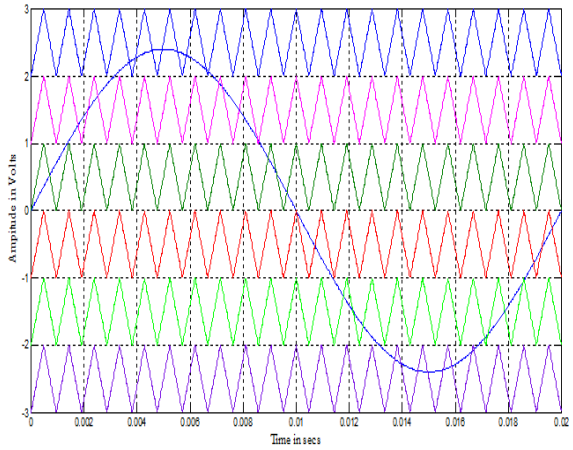

Fig 2: Carrier arrangement for PDPWM strategy

3.2 Phase Opposition Disposition (POD) PWM Strategy

With the POD method the carrier waveforms above the zero reference value are in phase. The carrier waveforms below zero are also in phase but are 180 degrees phase shifted from those above zero. Fig.3 shows the multicarrier arrangement for POD method for m_a= 0.8 and m_f =21.

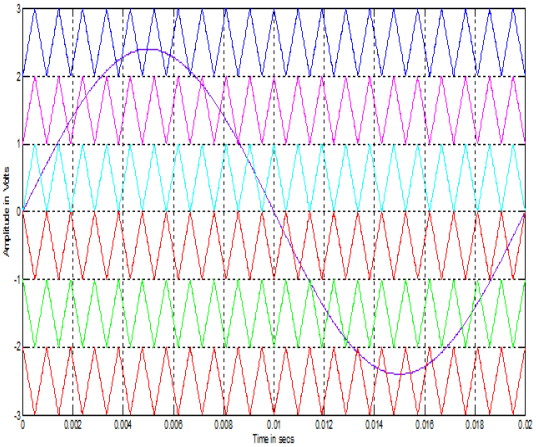

Fig 3: Carrier arrangement for PODPWM strategy

3.3 Alternative Phase Opposition Disposition (APOD) PWM Strategy

This method requires each of the six carrier waves for a seven level inverter to be phase displaced from each other by 180° alternately. Fig.4 shows the multicarrier arrangement for APOD method for m_a= 0.8 and m_f =21.

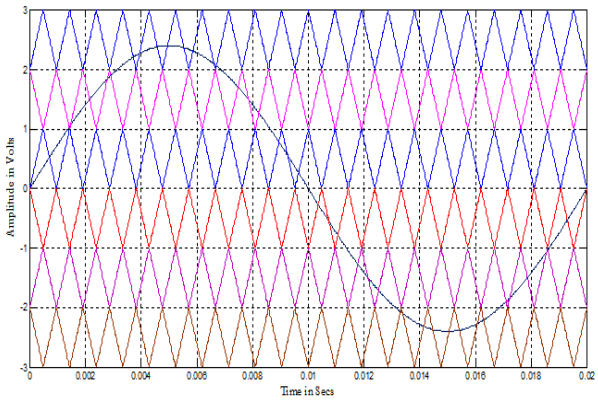

Fig 4: Carrier arrangement for APODPWM strategy

3.4 Variable Frequency (VF) PWM Strategy

The number of switchings for upper and lower devices of chosen Z-source inverter is much more than that of intermediate switches in constant frequency carriers. In order to equalize the number of switchings for all the switches, variable frequency PWM strategy is used as illustrated in Fig.5, in which the carrier frequency of the intermediate switches is properly increased to balance the number of switchings for all the switches.

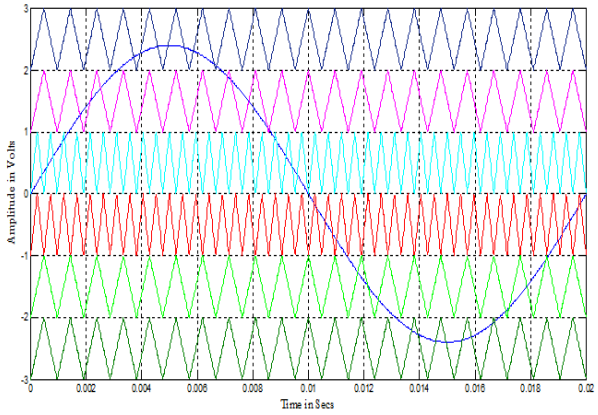

Fig.5 : Carrier arrangement for VFPWM strategy

3.5 Carrier Overlapping (CO) PWM Strategy

In the carrier overlapping strategy, m-1 carriers are disposed such that the bands they occupy overlap each other, the overlapping vertical distance between each carrier is $A_c/2$ (Ac=1.6).The reference waveform is centred in the middle of the carrier signals. The amplitude modulation index m_a is defined as follows:

$$m_a = Am/2Ac$$

The vertical offset of carriers for seven-level inverter with COPWM strategy is shown in Fig.6.

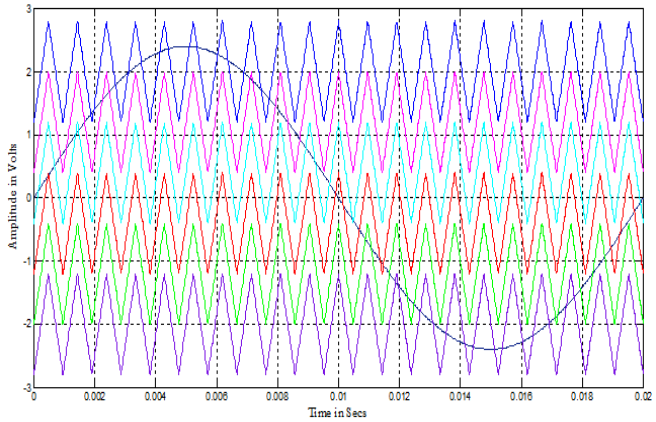

Fig 6: Carrier arrangement for COPWM strategy

4. SIMULATION RESULTS

The seven level diode clamped Z-source inverter is modelled in SIMULINK using Power System block set. Switching signals for Z-source multilevel inverter are developed using multicarrier sinusoidal PWM strategies are simulated. Simulations are performed for different values of m_a ranging from 0.8–1.

Figs.7–16 show the simulated output voltage of Z-source multilevel inverter and their corresponding FFT plots with above strategies but for only one sample value of m_a = 0.8. Fig.17 shows a graphical comparison of % THD for various strategies for different modulation indices.

For m_a=0.8, it is observed from Figs. (8, 10, 12, 14 and 16), the harmonic energy above 3% is present in (i) 7^{th} and 8^{th} orders in PDPWM strategy. (ii) 10^{th}, 18^{th} and 16^{th} orders in PODPWM strategy. (iii) 12^{th}, 14^{th}, 16^{th},18^{th} and 20^{th} orders in APODPWM strategy. (iv) 5th and 19^{th} order in VFPWM strategy. Among all the PWM strategies, COPWM contains no dominant harmonics. (v) Dominant lower side band harmonic (20^{th} order) is present in POD and APOD strategies. The corresponding %THD are measured using the FFT block and their values are listed in Table II. Table III shows the Distortion Factor (DF) of the output voltage of chosen MLI. Table IV displays the V_{rms} of fundamental inverter output (a measure of DC bus utilisation). Table V display the corresponding Crest Factor (CF). The following parameter values are used for simulation: V_{dc}=220V, C_1=C_2=400µF, C_3=C_4=C_5=C_6=C_7=C_8=1000mF,L_1=L_2=500µF,R(load)=100Ω, f_c=1050Hz and f_m=50Hz.

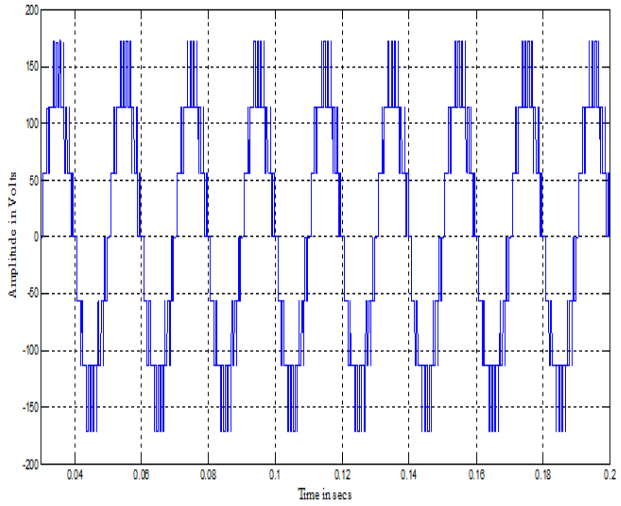

Fig 7: Output Voltage generated by PDPWM strategy

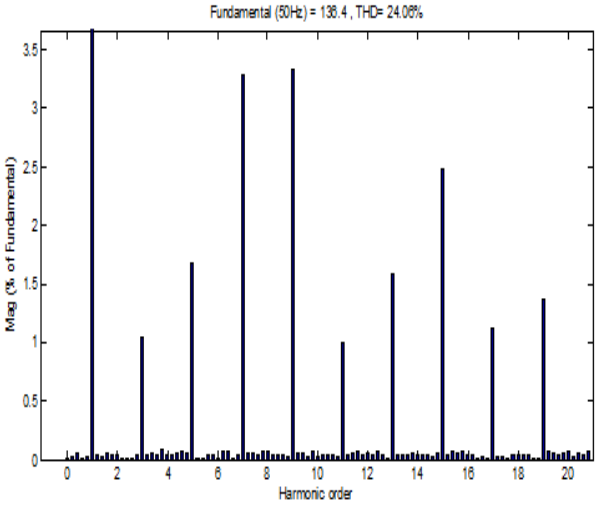

Fig 8:FFT plot for Output Voltage of PDPWM Strategy

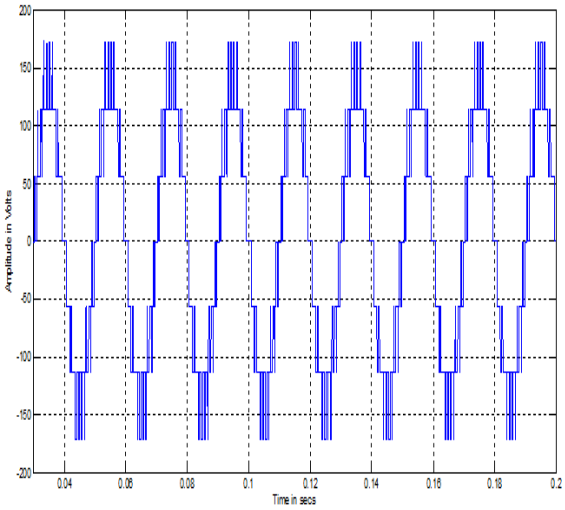

Fig 9: Output Voltage generated by PODPWM Strategy

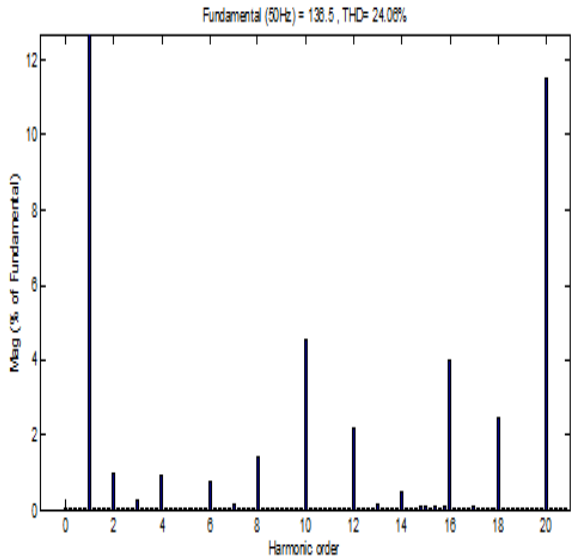

Fig 10: FFT plot for Output Voltage of PODPWM Strategy

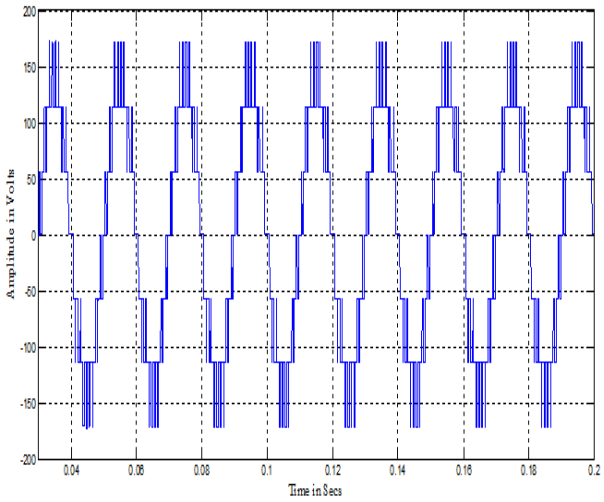

Fig 11: Output Voltage generated by APODPWM Strategy

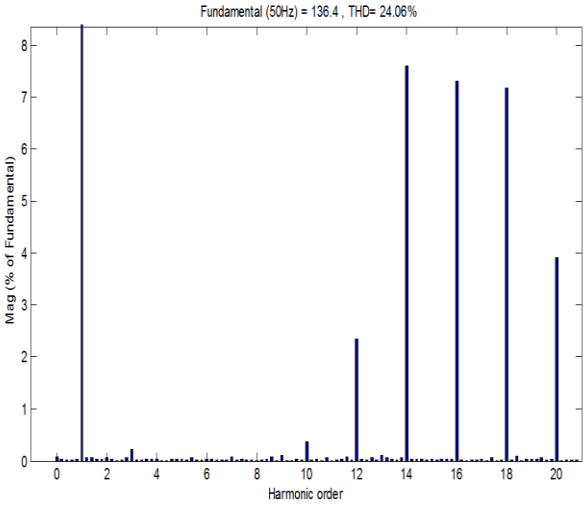

Fig 12: FFT plot for Output Voltage of APODPWM Strategy

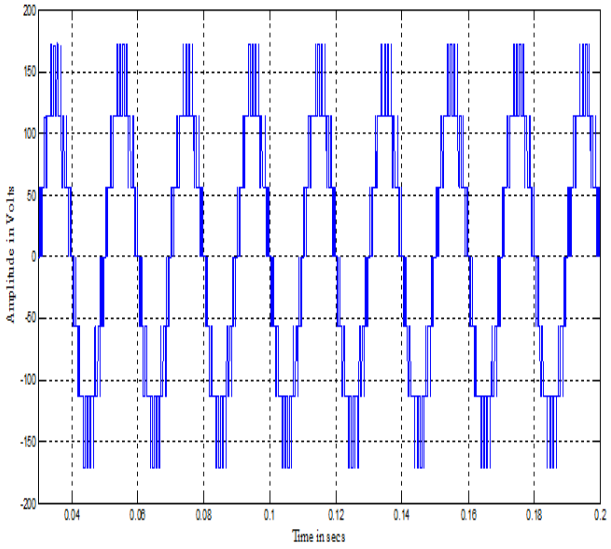

Fig 13: Output Voltage generated by VFPWM Strategy

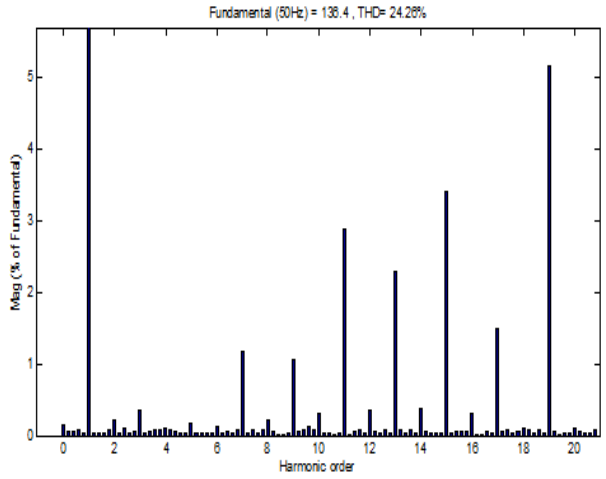

Fig 14: FFT plot for Output Voltage of VFPWM Strategy

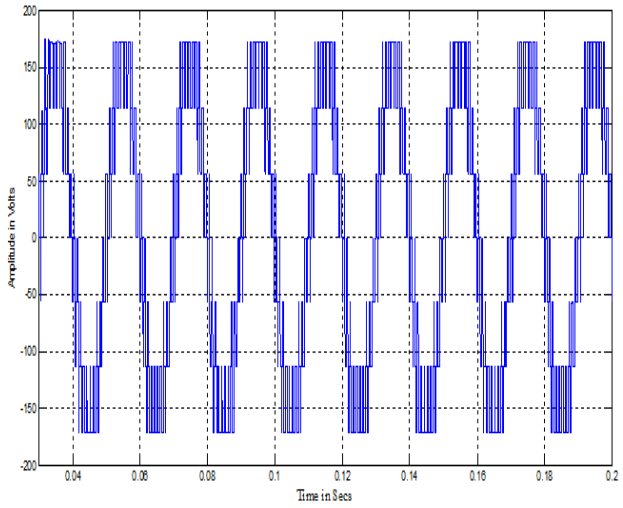

Fig 15: Output Voltage generated by COPWM Strategy

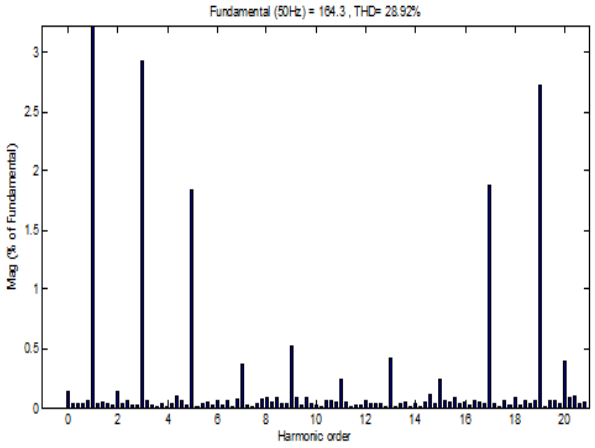

Fig.16 FFT plot for Output Voltage of COPWM Strategy

Table 2. %THD for different Modulation indices

m_a	PD	POD	APOD	VF	CO
1	17.89	17.84	17.91	17.95	22.00
0.95	20.62	20.61	20.65	20.67	24.52
0.9	22.60	22.65	22.62	22.57	22.77
0.85	23.22	23.24	23.33	23.39	26.64
0.8	24.06	24.06	24.06	24.26	28.92

Table 3. % Distortion Factor for different Modulation indices

m_a	PD	POD	APOD	VF	CO
1	0.3042	0.1762	0.0174	0.1473	0.8498
0.95	0.2559	0.1897	0.0723	0.1082	0.6749
0.9	0.1764	0.0997	0.0774	0.0581	0.5675
0.85	0.2204	0.1368	0.0726	0.1105	0.4706
0.8	0.1564	0.2544	0.064	0.0785	0.337

Table 4.V_{RMS} (Fundamental) for different Modulation indices

m_a	PD	POD	APOD	VF	CO
1	121	121.1	121	121	133.5
0.95	114.7	114.8	114.8	114.9	130.2
0.9	108.8	108.8	108.8	108.8	125.7
0.85	102.7	102.7	102.7	102.7	121.2
0.8	96.48	96.49	96.48	96.42	116.2

Table 5. Crest Factor for different Modulation indices

m_a	PD	POD	APOD	VF	CO
1	1.414	1.413	1.414	1.414	1.414
0.95	1.414	1.413	1.413	1.414	1.413
0.9	1.413	1.413	1.413	1.413	1.414
0.85	1.414	1.413	1.413	1.414	1.413
0.8	1.414	1.414	1.413	1.414	1.413

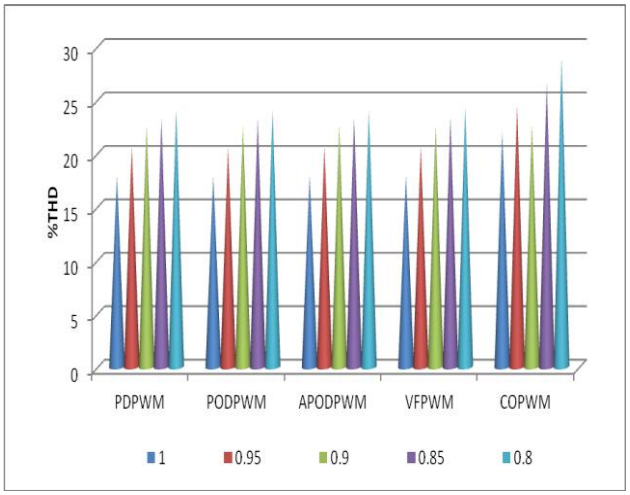

Fig 17: %THD Vs m_a

Of the five strategies developed, PODPWM Strategy provides output with minimum distortion (Table II), APODPWM strategy has low %DF (Table III), COPWM strategy provides relatively higher RMS output voltage Table (IV) and CF is almost same for all the strategies (Table V).

5. CONCLUSION

In this paper, various multicarrier PWM strategies for chosen Z-source diode clamped seven level inverter have been developed and simulation results are presented for different modulation indices ranging from 0.8-1.Various performance factors like %THD (a measure of closeness in shape between a waveform and its fundamental component), DF, Vrms of fundamental and CF (used to specify peak current rating of the devices) have been evaluated, presented and analysed. It is observed that the PODPWM strategy provides lower THD (Table II). The maximum DC bus utilization is achieved in COPWM strategy (Table IV). Appropriate PWM strategies may be employed depending on the performance measure required in a particular application.

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