

A Physics based Mosfet Noise Model for Nanoscale Applications

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ABSTRACT

Recently MOSFET has been considered as an important aspirant in the field of VLSI technology since it minimizes short-channel effect. FinFETs are promising substitute for CMOS at the nanoscale for meeting the challenges being posed by the scaling of conventional MOSFET. Continuous scaling of technologies towards the nanometer range will severely enhance noise implication. In this paper, a physics based MOSFET noise model that can accurately predict the noise characteristics over all the three operating regions known as subthreshold region, weak inversion region and strong inversion region is proposed. The physics based expressions for thermal noise has been derived and experimentally verified with corresponding graphs by using MATLAB simulation.

Keywords

FinFET, SCE, MOSFET, Thermal noise.

1. INTRODUCTION

The current trend of scaling down the size of the CMOS device is generally to improve the package density and speed of the device. Accurate modeling of FinFET is very essential to increase the performance of the circuit. FinFET is the easiest one to fabricate among the multigate devices and it consumes low power. Physics based modeling is to compute the structural parameters via physical simulation to predict the noise behavior of the device.

FinFET is typically to avoid short channel effect and leakage current when the device scales down to smaller size. As the channel length shrivel down to the nanoscale, these short-channel effects become more prominent in noise behaviors. The main focus of noise model is particularly the thermal noise of MOSFET, since it is the most dominant noise source in the device. Thermal noise is produced by the random Brownian motion of electrons due to the agitation of heat by means of some voltage fluctuations.

2. Noise Spectral Density

The noise power spectral density of drain current in presence of mobility degradation is given from [1] and [6]

$$S_{id} = \frac{1}{I_{DS} L_c^2} \int_0^{V_D} \frac{g_c^2(V, E)}{g(V, E)} S_{\delta i_n^2} dV \quad (1)$$

$S_{\delta i_n^2}$ is the power spectral density of local current fluctuation. $g_c(V, E)$ is channel gate conductance. $g(V, E)$ is the gate conductance. The expression for the current at any position in non uniform channel device is given by,

$$I(x) = g \left(V, \frac{dV}{dx} \right) \frac{dV}{dx} \quad (2)$$

$$g = W \mu Q_{inv} \quad (3)$$

Where W is the width, μ is the mobility, Q_{inv} is the inversion charge density. The ratio of the channel conductance to the overall conductance is expressed as,

$$\frac{g_c(V, E)}{g(V, E)} = \frac{g(V, E)}{g(V, E) + \frac{dg(V, E)}{dE} . E} \quad (4)$$

Where channel conductance is expressed as,

$$g_c(V, E) . E = g(V, E) \left(1 + \frac{E}{E_{crit}} \right) \quad (5)$$

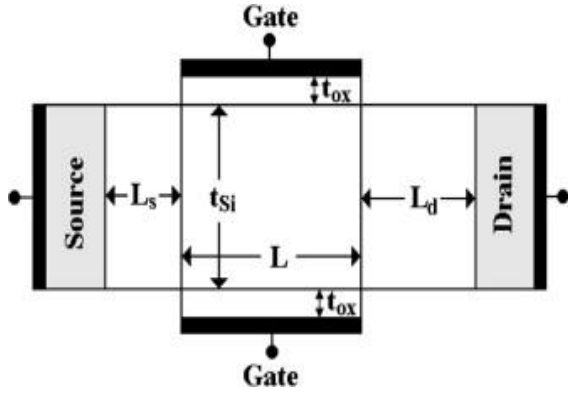


Figure 1. Schematic representation of double gate FinFET

The differential mobility is given by [2]

$$\mu(x) = \frac{\mu_{eff}}{\left[1 + \left(\frac{E}{E_{crit}}\right)^\beta\right]^{1/\beta}} \quad (6)$$

μ_{eff} is a effective mobility β is the fitting parameter, E_{crit} is the critical electric field. So combining (4), (5) and (6) the drain current noise power spectral density is given by

$$S_{id} = \frac{1}{I_{DS} L_C^2} \int_0^{V_D} g \left(1 + \frac{E}{E_{crit}}\right)^2 S_{\delta_{in}}^2 dV \quad (7)$$

2.1 Power Spectral Density of Drain Current

The local current fluctuations power spectrum density of the channel thermal noise is given by [1]

$$S_{\delta_{in}^2|_{thermal}} = 4KT_L \left(\frac{g^2(V, E)}{g_c(V, E)}\right) \left(\frac{T_n}{T_L}\right) \quad (8)$$

Where K is the Boltzmann constant,

T_L is the lattice temperature, T_n is the noise temperature.

From [7] and [8], we have

$$\frac{T_c}{T_L} = \left(\frac{\mu_0}{\mu_{eff}}\right)^2 = \left(1 + \frac{E}{E_{crit}}\right)^2 \quad (9)$$

μ_0 is the surface mobility. The spectral density of drain current can be expressed as,

$$S_{id} = \frac{4KT}{I_{DS} L_C^2} \int_0^{V_D} \left(1 + \frac{E}{E_{crit}}\right)^3 g^2(V, E) \quad (10)$$

Therefore, power spectral density of DG FinFET is given as,

$$S_{id|thermal} = B \int_{Q_S}^{Q_D} \frac{Q_{inv}^3}{Q_{inv} - A} \left(\frac{dQ_{inv}}{2C_{ox}} + \frac{KT}{q} \left(\frac{dQ_{inv}}{Q_{inv}} + \frac{dQ_{inv}}{Q_{inv} + 2Q_0} \right) \right) \quad (11)$$

Q_S is the charge density at source, Q_D is the charge density at drain and Q_{inv} is given as,

$$Q_{inv} = C_{ox} (V_{GS} - V_{TH}) \quad (12)$$

Where,

$$A = \frac{I_{DS}}{W \mu_{eff} E_{crit}} \quad (13)$$

$$B = \frac{4KT_L W^2 \mu_{eff}^2}{I_{DS} L_C^2} \quad (14)$$

2.2 Power Spectral Density of Gate Voltage

This is the power spectral density of thermal noise in double gate FinFETs. As mentioned earlier the inversion charge density is given by, from [5]

$$Q_{inv} = C_{ox} (V_{GS} - V_{TH}) \quad (15)$$

V_{GS} is the gate to source voltage, V_{TH} is the threshold voltage, C_{ox} is the gate capacitance per unit area, from [2] and [3]

$$g_c(V, E) = g(V, E) \left(1 + \frac{E}{E_{crit}}\right) \quad (16)$$

S_{id} is the drain current power spectral density, g_m is the conductance of the material given as

$$g_m = \frac{2\mu_0 C_{ox}}{WL} [V_{GS} - V_{TH}] \quad (17)$$

The power spectral density of local current fluctuations for the channel thermal noise is given as

$$S_{\delta i_n^2|_{thermal}} = 4KT_L \left(\frac{g^2(V, E)}{g_c(V, E)} \right) \left(\frac{T_n}{T_L} \right) \quad (18)$$

From [4]

$$S_{id} = \frac{1}{I_{DS} L_c^2} \int_0^{V_D} g \left(1 + \frac{E}{E_{crit}} \right)^2 S_{\delta i_n^2} dV \quad (19)$$

V_D is the drain voltage

The power spectral density of the drain current of thermal noise is given by

$$S_{id}|_{thermal} = \frac{4k_B}{I_{DS} L_c^2} \int_0^{V_{deff}} T_n g^2(V, E) \cdot (1 + E / E_{crit}) dV \quad (20)$$

Where V_{deff} the effective source is referenced drain voltage.

Therefore the gate voltage referred noise spectral density is given from [9],

$$S_{Vg} = \frac{S_{id}}{g_m^2} \quad (21)$$

So from (17) and (19) the gate voltage of noise spectral density is obtained as

$$S_{Vg} = \frac{K_B W^2 L^2}{I_{DS} L_c^2 \mu_0^2 C_{ox}^2} \frac{\int_0^{V_{deff}} T_n g^2(V, E) \left(1 + \frac{E}{E_{crit}} \right) dV}{(V_{GS} - V_{TH})^2} \quad (22)$$

3. RESULTS AND DISCUSSIONS

Fig.1 shows the noise power spectral density of the drain current $S_{id|_{thermal}}$ as the function of V_{ds} . This model is applicable in the velocity saturation region.

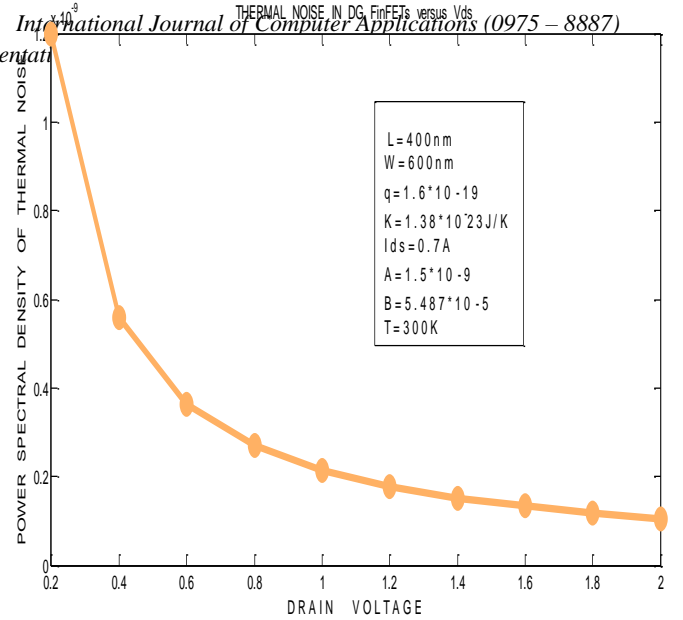


Fig 1. Power Spectral density of thermal noise versus drain voltage

From fig.1 thermal noise decreases with increase in V_{ds} . So that noise contribution from the velocity saturation region of channel is negligible.

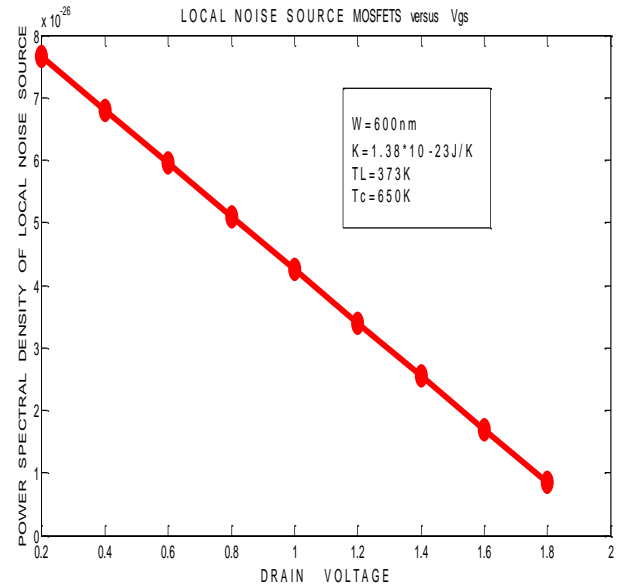


Fig 2. Shows the Power Spectral density of the local noise source versus drain voltage.

Fig 2.demonstrates that the thermal noise decreases with increase in the drain voltage. It is valid for all operating regions of the finfets. Thus the comparison with the power spectral density of local noise source against the drain voltage is plotted.

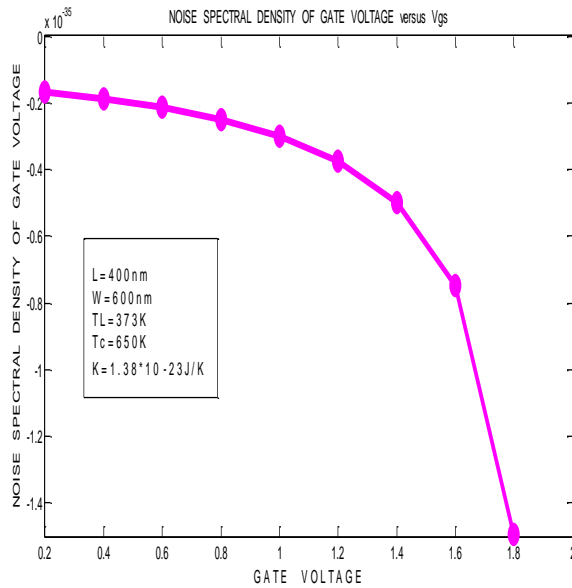


Fig 3. Shows the Power Spectral density of the gate voltage versus drain voltage.

This fig 3 illustrate the thermal noise for a saturated p-channel transistor of the same technology and with the same aspect ratio. It is valid for all operating regions of the FinFETs. Thus the simulation between the noise power spectral density of gate voltage and the gate voltage is plotted.

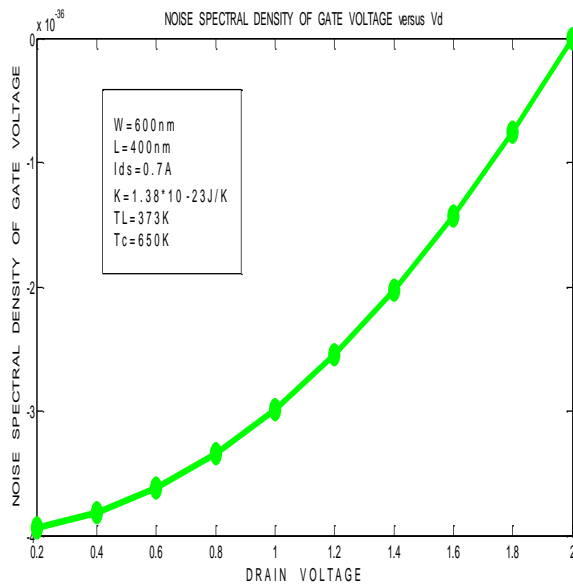


Fig 4.shows the simulation graph between power spectral density of gate voltage versus gate voltage.

In Fig 4.shows that as the channel length is scaled down, the saturation region can take over a considerable path of the channel with increasing V_{DS} , thus enhancing the thermal noise amplitude.

4. CONCLUSION

The proposed thermal noise model have been evaluated in all the operating regions of double gate FinFETs namely under the sub threshold region, moderate inversion region and strong inversion region. The resulting thermal noise shows that carrier heating effect is significant at high gate biases and channel length modulation is significant at low gate biases. The modeling of thermal noise is incorporated in circuit simulation platform to implement the noise performance in various sources. This paper will pave the way for compact modeling the noise including various noise sources, which will be very helpful for the low-noise analog IC design.

5. REFERENCES

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