2d Threshold and Tran Conductance to Drain Current Ratio Modeling of Triple Material Double Gate (TMDG) Mosfet

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ABSTRACT
VLSI technology is constantly evolving towards smaller line widths. In this paper analytical modeling for triple material double gate (TMDG) MOSFETs has been presented in the field of VLSI technology. An entire circuit is manufactured in a single piece of silicon. The level of integration of silicon technology as measured in terms of number of devices per IC. This leads to the concept of scaling in MOSFET devices. And further MOSFET occupies much smaller area of silicon than the equivalent BJT, due to which MOSFET requires less current and less power than its bipolar counterpart. SCALING enhances the design or manufacturing of extremely small complex circuitry using modified semiconductor material.The miniaturisation is achieved through scaling in two ways – size reduction of the individual devices and increase in the chip or dice size. But eventually scaling leads to short channel effects(SCEs). So, the main objective of our project is to reduce the short channel effects (SCEs) and threshold voltage roll off by using triple material double gate MOSFET (TMDG) in which the gate is made of three materials with different work functions. The 2D Poisson's equation is solved for surface potential threshold voltage and electric field using parabolic approximation method and the work is extended to obtain transconductance for TMDG. Future work of our paper is extended to solve above mentioned parameters using Superposition method**.**

Keywords
Transconductance,TMDG,Thresholdvoltage, Surface potential, SCE,electric field,Scaling.

1. INTRODUCTION
Scaling opens the window for short channel effects which will reduce the performance of the device .The trend towards miniaturization is tremendously increasing nowadays. And this forces the recent technologies to prefer downscaling of the metal-oxide semiconductor field-effect transistor (MOSFET) devices. When these devices are scaled to lower feature lengths it paves the way for serious short channel effects (SCEs). But double-gate (DG) MOSFETs seems to have some control over SCEs. And further the higher

capability of DG MOSFETs to be scaled down in the sub-45 nm node technology makes it more attractive than the single-gate MOSFETs. Normally, these short channel effects arises when the gate losses its control over the channel [1]. This detrimental presence of SCEs leads to degradation in the device performance.

In order to have control on SCEs and to reduce the drain control over the channel, a simple technique adapted is to make the step-function like shaping of the surface potential function which screens the effects of drain. And therefore, the gate contact of a MOSFET is formed by using more than one material with different work functions which is used to generate the step-shape of the surface potential profile. And this technique has shown improvements for SCEs and hot carrier effects (HCEs) [1-6] in the silicon-on-insulator (SOI) MOSFETs and DG MOSFETs.

Many experiments have been dealt with dual-material-gate (DMG) MOSFETs in which the gate of the MOSFET consists of two different materials with different work functions, was proposed by Long [2]. This induces the step function in the DMG at the interface between different gate materials which improves the carrier transit speed. So due to the screening effects of the gate, the high electric field at the drain end is reduced which helps to suppress the HCEs. This was further expanded as dual-material DG MOSFET by Kumar and Reddy [3] by incorporating the advantages of both the DG MOSFETs and single-gate DMG MOSFET. And they manifested that there is an improved transconductance, an increased drain breakdown voltage, a reduced drain conductance, and a desirable threshold voltage roll-up even for channel lengths of far below 50 nm.

2. PROPOSED METHOD
A new structure called triple material (TM) is likely to provide significant improvement over the DM-DG MOSFETs as it efficiently screens the effects of drain because it creates two step-shapes in the surface potential profile. This bestride-gate structure was proposed by Tiwari [4] in which the gate of the MOSFET is made up of three different materials with three different work functions; so as to reduce the SCEs to a maximum extend by creating smaller threshold voltages in the TM structure. The sub threshold current model for the TM gate SOI MOSFETs was proposed by Chiang et al. using the separation of variables method. Further Razavi [5] demonstrated the superiority of the TM-DG MOSFETs over the DM-DG MOSFETs using TCAD simulation results but

theoretical model was not reported to support the simulation results.

The TM-DG MOSFET structure is shown in Figure. 1 where L is the gate-length, t_{si} is the channel thickness, and t_{ox} is the gate-oxide thickness. In the TM-DG MOSFET structure the gate electrode is made of three materials with three different work functions which are deposited on the gate-oxide layers L_1, L_2 and L_3 respectively where $L=L_1+L_2+L_3$. The three work functions are denoted by $\phi w1, \phi w2, \phi w3$ respectively. The work functions are chosen such that $\phi w1 > \phi w2 > \phi w3$.

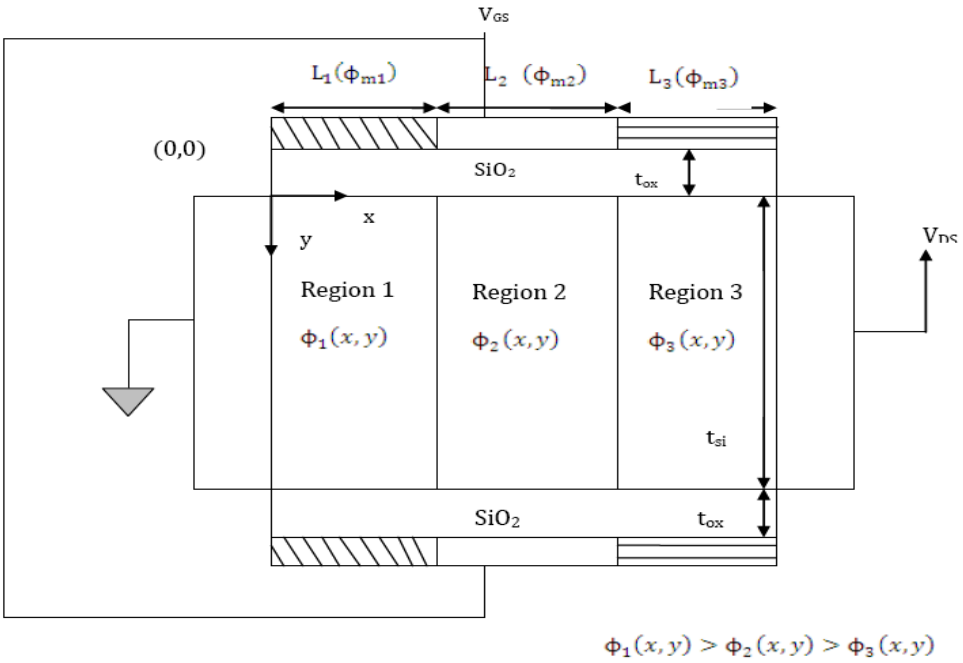

Figure 1. Structure of TMDG MOSFET

The control gate is formed by placing the gate material with the highest work function $(\phi w1)$ at the source end, whereas the first screen gate is formed by using the gate material with intermediate work function $(\phi w2)$. Similarly the second screen gate is formed by placing the lowest work function at the drain end. Tungsten disilicide (WSi_2) is used as the control gate with work function 4.8 (eV). In the same way $Hf_{0.27}Ta_{0.58}N_{0.15}$ is used as the first screen gate with work function 4.6 (eV) and $Hf_{0.40}Ta_{0.46}N_{0.14}$ is used as the second screen gate with work function 4.4 (eV). In the source and drain regions the doping concentration is considered to be heavily doped with $N_{sd} = 10^{20}$ cm^{-3}. For the channel region the acceptor doping concentration is assumed to be lightly doped with $N_a=10^{16}$ cm^{-3}. In this the device is considered as the fully depleted (FD) device because it reduces the leakage current and power consumption. Further it does not have floating body effect and SCEs can be controlled easily.

3. SURFACE POTENTIAL

To determine the surface potential for the TMDG MOSFET let us take $\phi_p(x,y)$where p=1, 2, 3 be the surface potentials in the channel regions I, II, and III, respectively. Thus $\phi_p(x,y)$ can be obtained by solving the following 2D Poisson's equation:

$$\frac{\partial^2\phi_p(x,y)}{\partial x^2} + \frac{\partial^2\phi_p(x,y)}{\partial y^2} = \frac{qN_a}{\varepsilon_{si}} \quad (1)$$

It can be known as the built in potential at the junctions of source-channel and channel-drain region.

By following the method of Young [6] the solution for the 2D-poisson equation using parabolic approximation for the regions I, II, and III may be written as,

$$\phi_p(x,y) = k_{p0}(x) + k_{p1}(x)y + k_{p2}(x)y^2 \quad (2)$$

By using the boundary conditions which are discussed above the arbitrary functions of x

$$k_{p0}(x) = \phi_{Sp}(x) \quad (3)$$

$$k_{p1}(x) = \frac{\varepsilon_{ox}[\phi_{Sp}(x) - V_{GS} + V_{fbp}]}{\varepsilon_{si}t_{ox}} \quad (4)$$

$$k_{p2}(x) = \frac{\varepsilon_{ox}[\phi_{Sp}(x) - V_{GS} + V_{fbp}]}{\varepsilon_{si}t_{ox}t_{si}} \quad (5)$$

Substitute $y = \frac{t_{si}}{2}$ in Eq.(3), the potentials at the center and the surface can be related as ,

$$\phi_{Sp}(x) = \frac{\phi_{Cp}(x) + \frac{r}{4}(V_{GS} - V_{fbp})}{\left(1 + \frac{r}{4}\right)} \quad (6)$$

The mid channel potential for the device is $\phi_{Cp}(x) = \phi_p(x,y)$ at $y = \frac{t_{si}}{2}$ and $r = \frac{\varepsilon_{ox}t_{si}}{\varepsilon_{si}t_{ox}}$ which can be defined as the ratio of gate oxide capacitance and silicon-channel capacitance. Along with a characteristic length λ the mid-channel potential plays a major role in determining the short channel effects of TM-DG MOSFETs, we determine the characteristic length λ [12] as follows.

At the middle of the silicon channel the 2D Poisson's equation can be solved as,

$$\frac{\partial^2\phi_{Cp}(x)}{\partial x^2} - \frac{\phi_{Cp}(x)}{\lambda^2} = \frac{qN_a}{\varepsilon_{si}} - \frac{V_{GS}-V_{fbn}}{\lambda^2} \quad (7)$$

The general solution for the Eq. (22) can be written as,

$$\phi_{Cp}(x) = X_p exp(tx) + Y_n exp(-tx) - \frac{S_p}{\alpha} \quad (8)$$

Where $\alpha = \frac{1}{\lambda^2} = t^2;\ S_p = \frac{qN_a}{\varepsilon_{si}} - \frac{V_{GS}-V_{fbp}}{\lambda^2}$

With the help of Eqs., (2), (3), (4) the 2D channel potential for the regions I, II, and III can be written as

$$\phi_p(x,y) = \begin{pmatrix} X_n exp(tx) + Y_n exp(tx) - \frac{S_n}{p^2} \Big/ \left(1+\frac{r}{4}\right) \\ +\frac{r}{4}(V_{GS}-V_{fbn}) \end{pmatrix} \times \left[1 + \frac{r}{t_{si}}y - \frac{r}{t_{si}^2}y^2\right] - \frac{r}{t_{si}}(V_{GS}-V_{fbp})y + \frac{r}{t_{si}^2}(V_{GS}-V_{fbp})y^2 \quad (9)$$

If the minimum value of $\phi_{C1}(x)$ at $x = x_{0\,min}$ is $\phi_{C1\,min} = \phi_{C1(x_{0\,min})}$. then the distance $x_{0\,min}$ is

$$x_{0\,min} = \frac{1}{2p} ln \frac{Y_1}{X_1} \quad (10)$$

Then from the Eqs. (16) and (21), we can get the minimum surface potential for the TM-DG MOSFETs is given by,

$$\phi_{C1\,min} = 2\sqrt{X_1 Y_1} - \frac{\lambda^2 qN_a}{\varepsilon_{si}} + V_{GS} - V_{fb1} \quad (11)$$

3.1 ELECTRIC FIELD

The electric field along the channel determines the velocity of electron transport through the channel therefore, in 'r' direction it is represented as

$$E_1(Z) = \frac{\partial\phi_{S1}(r,z)}{\partial r}$$

$$E_1(Z) = X_1 pexp(px) - Y_1 pexp(-tx) \quad (12)$$

3.2 THRESHOLD VOLTAGE

The threshold voltage may be defined as the gate voltage at which the surface potential becomes twice the Fermi potential, the conducting channel of the device will be established until and unless all the three channels are turned ON. Because of these criteria, the control gate region of length L1 with the highest gate function is used to monitor the threshold voltage of the device.

$$V_{TH} = Vfb1 - \left(\frac{4}{4+r}\right)\left((2\sqrt{A_{11}B_{11}}\right) - \frac{(\lambda^2 qNa)}{\varepsilon_{si}}) (1+ (3r/16))$$

$$+ \left(\frac{KT}{q}\left(\frac{\ln Q_{TH}}{n_{si}t_{si}}\right)\right) \quad (13)$$

3.3 TRANSCONDUCTANCE

The amplification of a device is determined through the transconductance behavior of that device, so in order to obtain the amplification the essential criteria is power dissipation. The term drain current represents the power dissipated of that device. The ratio transconductance-to-drain current is an important parameter for achieving a highly improved CMOS technology performance. When this ratio increases, then the voltage gain of a MOSFET will reached to its maximum value. For analog applications, high value of transconductance-to-drain current ratio will be preferable.

In order to facilitate and extend the use of TMDG MOSFETs in integrated circuits, it is essential to design a compact and accurate model. Balamurugan et al proposed a design model based on the surface potential approach of finding the transconductance to drain current ratio of DMSGT MOSFET.

$$\phi_{Cp}(x) = X_p exp(tx) + Y_p exp(-tx) - \frac{S_p}{\alpha} \quad (14)$$

$$\phi_{C1}(x) = X_1 exp(tx) + Y_1 exp(-tx) - \frac{S_1}{\alpha} \quad (15)$$

$$\phi_{C2}(x) = X_2 exp(tx) + Y_2 exp(-tx) - \frac{S_2}{\alpha} \quad (16)$$

$$\phi_{C3}(x) = X_3 exp(tx) + Y_3 exp(-tx) - \frac{S_3}{\alpha} \quad (17)$$

Where V_{bi} is the built in potential between the source and the body, V_{ds} is the drain-source voltage, L_1 is the channel length and also Q parameter corresponds to the respective regions.

Minimum surface potential($\phi_{C1\,min}$) of the TMDG MOSFETs will be under the gate having the highest work function, so $\phi_{C1\,min}$ lies under the control gate(M_1) being the highest work function metal in TMDG structure. Hence $\phi_{C1\,min}$ is given by $\phi_{C1\,min} = 2\sqrt{X_1 Y_1} - \frac{S_n}{\alpha}$

And the minimum surface potential occurs at

$$z_{min} = \frac{1}{2P} ln\left(\frac{Y_1}{X_1}\right) \quad (18)$$

$$\left(\frac{Y_1}{X_1}\right) = \left(\frac{2F\,sinh(PL_1) - E}{+Fexp(-PL_1) - G\,cosh(PL_2) - H\,cosh(PL_3)}{E - Fexp(-PL_1) + G\,cosh(PL_2) + H\,cosh(PL_3)}\right) \quad (19)$$

$$\lambda_{tm} = \frac{1}{P} = \sqrt{\frac{t_{si}t_{ox}\varepsilon_{si}}{2\varepsilon_{OX}}} \quad (20)$$

Transconductance-to-drain current ratio is defined as the amplification obtained from the device divided by the energy supplied to achieve this amplification(I_{ds}).

The direct measure of efficiency of the transistor is given by the ratio $\left(\frac{g_m}{I_{ds}}\right)$.It is a measure of the effectiveness for the control of the drain by the gate voltage.

The transconductance-to-drain current $\left(\frac{g_m}{I_{ds}}\right)$ ratio is given as

$$\frac{g_m}{I_{ds}} = \frac{q}{kT}\left(\frac{\phi_{C1\,min}}{\partial V_{GS}}\right) \quad (21)$$

Where $\phi_{C1\,min}$ is the minimum surface potential K is the Boltzmann's constant and T is the temperature in Kelvin.

On differentiating the minimum surface potential with respect to V_{GS}, the resultant expression obtained from differentiation is

$$\frac{g_m}{I_{ds}} = \left(\frac{\left(\left((sinh\,Pz)(2Fexp(-Pz)) - E - F\right) + \right)}{\left(2\sqrt{XY}(sinh(Pz))^2\right)}\right) + 1 \quad (22)$$

4.RESULT AND DISCUSSION

The theoretical results for the analytical model are validated by comparing the TMDG MOSFET with DMDG MOSFET. The comparison of electric field and surface potential values for DMDG and TMDG MOSFETs are shown in figure. Our results are in good agreement with those derived by Tiwari et al by solving the 2D Poisson's equation in the oxide and silicon regions.

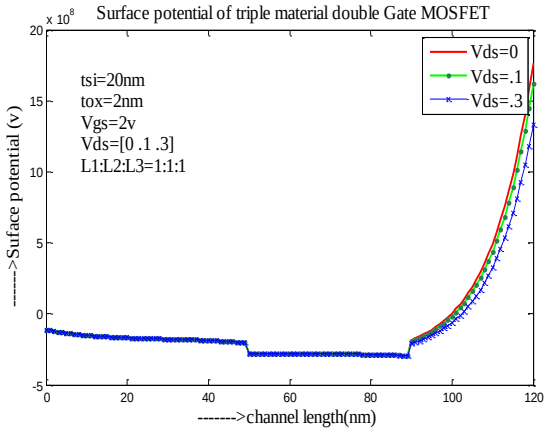

Figure. 2. Surface potential variation along the channel for different values of drain-source voltage

In Figure.2 presents the surface potential variation with respect to the drain to source voltage Vds. The parameters which are used in Fig.2 are L=120nm, tsi=20nm, tox=2nm, Vgs=2V. As from the figure it is observed that surface potential value in TMDG MOSFET shows the step up compared to the surface potential values in DMDG MOSFETs. It is also visible that area under the TMDG structure control gate the drain voltage has very little impact towards drain current after saturation.

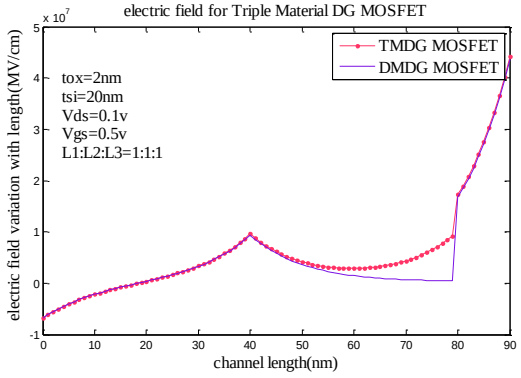

Figure.3.Electric field variation with respect to different channel lengths

From the discussions it is known that the electric field is derived by taking the first spatial derivative of surface potential. In Figure.3 it shows the electric field variation with respect to the different channel length values. It can also be observed in the figure that the values of electric field show a peak at the drain end of TMDG MOSFET. This peak is higher than the peak value showed in DMDG MOSFET. The parameters which are used are variable channel lengths, Vgs=0.5V, Vds=0.1V, t_{si}=20nm, t_{ox}=2nm.

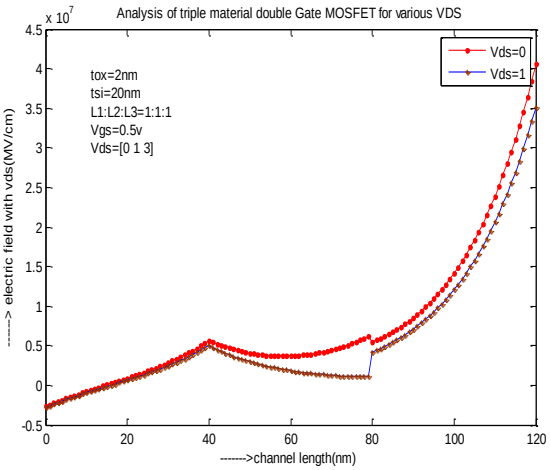

Figure.4.Electric field variation along the channel length with various Vds values

In Figure.4 it shows the electric field variation along the channel length with respect to the different Vds values. It can also be observed in the figure that the values of electric field show a peak at the drain end of TMDG MOSFET. This peak is higher than the peak value showed in DMDG MOSFET.

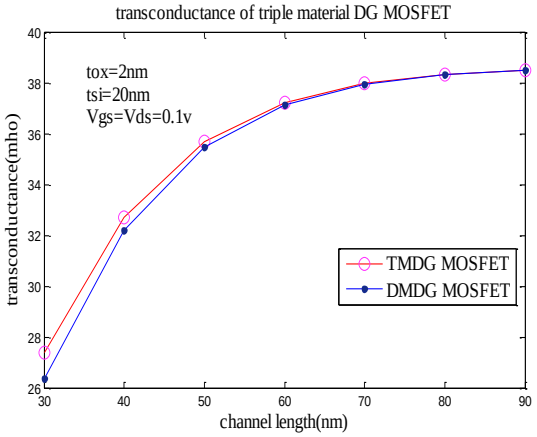

Figure.5.Transconductance along the channel length in TMDG MOSFET

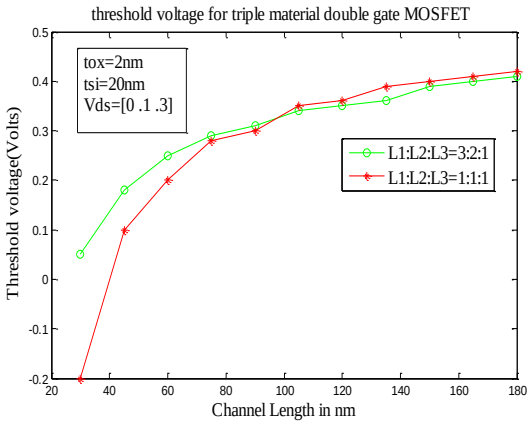

Figure.6.Threshold voltage variation with channel length for different Vds values

In the Figure.5 it is clearly visible that there is some peak

value which is higher than the DMDG MOSFET. So it is evident that efficiency of TMDG MOSFET gets increased compared to the DMDG MOSFET. In Figure.5. it shows the transconductance figure along the potential channel length where the transconductance is increased in TMDG MOSFET compared to the transconductance value calculated in DMDG MOSFET.

In Figure.6 the threshold voltage variation with the channel length for different values of Vds is represented. From the result it is observed that the device with higher length ratio will decrease the roll off effect .further the threshold voltage device with higher L1:L2:L3 ratio are observed to be having higher threshold voltages as lower channel length devices which are clearly not a favorable condition for the device for the design of low power circuits with such devices.

4. CONCLUSION

In this paper, the transconductance for the TM-DG MOSFET has been presented using parabolic potential approximation, along with the electric field and surface potential. It shows that TM-DG produces better reduction of short channel effects when compared to DM-DG and SM-DG. Moreover, the overall device performance of TM-DG MOSFET is improved than other structures

APPENDIX

The boundary conditions is to be obtained for the channel interfaces (i.e.) I-II and II-III because the potential function is needed to be a continuous function over the entire region of channel

$$\phi_1(L_1, 0) = \phi_2(L_2, 0) \quad \text{(A1)}$$

$$\phi_1(L_1, t_{si}) = \phi_2(L_1, t_{si}) \quad \text{(A2)}$$

$$\phi_2(L_1 + L_2,) = \phi_3(L_1 + L_2, 0) \quad \text{(A3)}$$

$$\phi_2(L_1 + L_2, t_{si}) = \phi_3(L_1 + L_2, t_{si}) \quad \text{(A4)}$$

As similar to DM-DG MOSFETs [8] it is also noted in TM-DG MOSFETs that electric fluxes will be continuous at the interfaces. Thus the boundary conditions for the interfaces is given by

$$\frac{\partial \phi_1(x,y)}{\partial x} = \frac{\partial \phi_2(x,y)}{\partial x}\Big| \; x = L_1 \quad \text{(A5)}$$

$$\frac{\partial \phi_2(x,y)}{\partial x} = \frac{\partial \phi_3(x,y)}{\partial x}\Big| \; x = L_1 + L_2 \quad \text{(A6)}$$

The interfaces of source-channel potential and channel-drain potentials are given by [8].

$$\phi_1(0,0) = \phi_{S1}(0) = V_{bi} \quad \text{(A7)}$$

$$\phi_1(L_1 + L_2 + L_3, 0) = \phi_{S3}(L_1 + L_2 + L_3) = V_{bi} + V_{DS} \quad \text{(A8)}$$

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