Energy Aware Processor Utilization Control for Mobile Devices

Kanimozhi.K
PG Scholar,
Anna University,
Regional Centre,
Coimbatore.

S.N.Deepa, Ph.D
Associate Professor,
Dept. of EEE,
Anna University,
Regional Centre,
Coimbatore.

ABSTRACT

Power consumption is considered as an important factor for battery operated (i.e portable) devices. This paper proposes a completely unique technique for the processor power management downside . The proposed technique does not require definitive power performance model of a processor. The proposed technique exploits control principles for a given workload.

Experimental results obtained from various literatures are presented demonstrating usefulness and practicable proposed solution.

INDEX TERMS

Mobile Power Management, control, Energy conservation, Operating System, DVFS

1. INTRODUCTION

Due to increase in popularity of mobile devices such as Smartphone, LAPTOP, pad/Tablet computers(ex.ipad),energy efficiency conservation schemes have recently received a lot of attention .Those schemes achieve power savings through Dynamic Voltage and Frequency

Scaling(DVFS) by either predicting the operation at low power states or by reducing the supply voltage and clock frequency. If a processor supports Dynamic Voltage and frequency scaling during operation ,the V and f and as a result ,reduce the total power consumption while still satisfying performance demands.

Some application-aware Dynamic Voltage and frequency scaling techniques have been analyzed [1][2][3]. For a single service contributor (core processor),the power management literature is ample and formalisms with ideal solution.

1.1 DVFS Scheme

In recent years, mobile device have transpire as a solution for hi-speed computing demands. DVFS is wide wont to cut back the active power, however its efficacy and value depends on graininess at that it's applied. The process of dynamically sterilization the availability voltage and operative frequency is often referred as Dynamic Voltage and Frequency Scaling (DVFS) and also the corresponding schedule is named as DVFS schedule. A key part of DVFS is that the use of one or a lot of voltage regulators that transport to a circuit from an energy supply.

Dynamic voltage scaling could be a power Management technique in PC design, wherever the voltage utilize in a element embellished or assuage, relying upon circumstances. Dynamic voltage scaling to extend comes from battery and so is constrained. Dynamic voltage scaling is additionally noted as Overvaulting. Overvaulting is finished so as to extend PC performance, or in rare cases, to extend dependability .Dynamic frequency scaling is additionally referred to as processor asphyxiation wherever by the frequency of micro chip are often perfunctorily adjusted either to safeguard power or to engrave back the number of heat generated by the chip. Dynamic frequency scaling is usually employed in laptops and different mobile devices wherever the energy comes from electric battery and so it's controlled. it's additionally employed in quiet computing settings and to decrease energy and cooling prices for tenderly loaded machines. Less heat output ,in turn permits the system cooling fans to be throttled down or turned off, reducing noise levels and any decreasing power consumption. it's additionally reducing heat insufficiently cooled system once the temperature reaches a particular threshold , like in feebly cooled over clocked system

2. RELATED WORKS

J.Cho et. al provided the primary study on Dynamic voltage. And it had been analyzed with the time forecast for specific workloads. For Processor, the facility management literature is wealthy in technique and formalisms with optimum solutions. This can be applicable once the optimum power policies square measure outlined fr DVFS ate degree correct power consumption and performance of processor.

Choi et.al projected another prediction attitude employing a frame based mostly history [6] for power conservation. They divided the specified cryptography time for every frame into 2 components namely: a) frame reliant (FD) and b) frame freelance half (IFD) half. The cryptography time of a FD half is calculable solely on frame dependent kind half is calculable based solely on frame kind.

An experimental verification of power savings during a DVS-based transmission signal Processor system(DVS-MSP) was performed[7].Assuming the procedure work needed to decrypt every frame follows the arithmetical distribution, the authors showed that the typical power savings increase once there square measure voltage frequency scaling levels.

Last Liu et al. given Chameleon architecture, that is bracket together degree application level power management approach oppression application domain data involves estimating work prediction.

The dead-zone based mostly management formula was given by Lutetium et al [9], that maintains decoded frames during a variety of buffers and adjusts clock frequency per the quantity of decode frames within the buffers.

Im et al.[10], provided a theoretical analysis on the minimum buffer size and therefore the fine-tuning of task deadline to cut back energy consumptions however their methodology assumes that the simplest and worst case cryptography times of frames square measure offered as priori, that is impractical.

Lee et al.[11] projected ILI based mostly formula on the actual fact that the link between frame size and cryptography times is non-linear. The magnitude of the intervals square measure dynamically adjusted to equally distribute the quantity of frames that belong to every interval. This can be done by subdividing the frame size axis into tiny sized steps, maintain data regarding the quantity of frames and add of work for every step.

The QLB formula projected by Lee et al. depends on a feedback mechanism to change between low-power and quality modes. The video playback with and while non DVFS is analyzed.

In order to attain low power and at same time maintain quality, the QLB premise has 2 modes of operation :Q mode – Quality of Video playback, whereas L mode – provides Low Power. The QLB formula at first operates in Q- mode to guarantee the standard of video playback.

3. EXISTING SYSTEM

In this section, a basic power manageable by model is accessible along with the justification of feedback control. The blocks such as sensors, controller is presented for the feedback control.

3.1 Power Management Model

Power Management could be a feature of some mobile devices that turns off the ability or switches the system to a auburn power state once inactive. In computing, this is often referred to as laptop power management and is made around normal known as ACPI. This supersedes APM. All recent mobile devices have ACPI support. The foremost goal of power management for automatic data processing system is to cut back overall energy consumption and to keep up prolong battery life for mutability and to cut back cooling needs, in conclusion to cut back noise.

Lower power consumption conjointly suggests that lower cooling, that will increase system stability, and fewer energy use, that saves cash and reduces the impact on the atmosphere. the ability management will be done over the complete processor or in specific areas with dynamic voltage, clock rate or each will be tainted to decrease power consumption at the worth of probably lower performance.

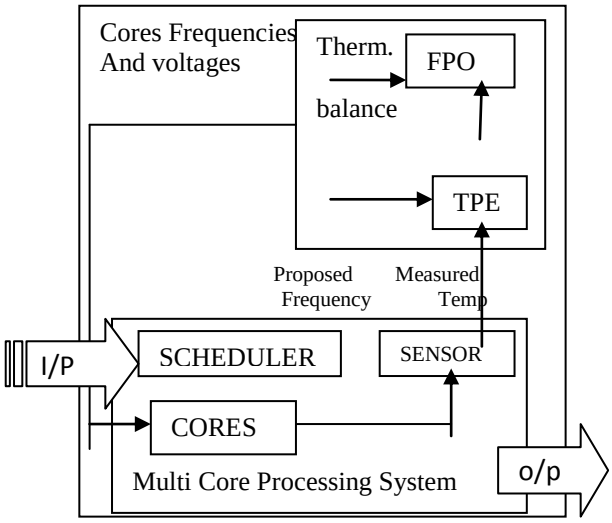

Fig 1: Basic Power management model

In the above figure (fig. 1)FPO denotes Frequency assignment problem Optimization ,TPE denotes Thermal Profile Estimation.

3.2 Feedback Control

Based on the related works some methods are stated above. Least-square estimation is used to model the dynamics of the power management model.

The parameters used to calculate the dynamic voltage ad frequency for approximation are;

"t"-> time variable(discrete series)

"h"-> Sampling period

The operator q has the property ;

$q\ x(t)=x(t+1)$

where the signal x(t) is considered as infinite sequence,

$\{x(t):t= -1,0,1\}$

$(q+a_1)\ y_s(t)= b_1\ u(t)$ → (1)

For a general linear controller, the equation may be given as;

$R(q)\ u(t) = T(q)u_c(t) - s(q)\ y_s(t)$ → (2)

The saturation temperature which is set as minimum or maximum according to least square estimation method are

$$sat(u)= \begin{cases} u_{min} & \text{if } u \le u_{min} \\ u & \text{if } u_{min} < u < u_{max} \\ u_{max} & \text{if } u \ge u_{max} \end{cases} \quad (3)$$

The Control law, including for the controller design is given by;

$$u(t)=sat(a_1u(t-1)+(1/b_1)u_c(t)-(a_1^2/b_1)Y_s(t))\rightarrow(4)$$

The reference input $u(t)$ can be controlled by output signal $y_s(t)$.

Section III deals with module description and the power consumption system are described.

4. SYSTEM MODEL & SPECIFICATION

The power manager may be a program feasible by the processor even as software system and work. The subsequent power policies area unit compared with the work explicit in [11].The Metrics area unit evaluated to power management policies. The performance and method utilization decreases with the frequency, at the value of larger power consumption.

The various steps concerned are: hardware and Memory Usage:

In this module we tend to monitor the usage of CPU(central processing unit, hardware)additionally user will read current Running process standing in system.

Battery Status:

During this module the standing of battery usage (i.e) the laptop computer is functioning in battery mode or Main power mode is monitored and additionally displays the Remaining Battery standing ongoing Bar.

observance and dominant Processes:

Here we tend to monitor the number of battery usage and Remaining Battery charge for dominant the Running method and save the battery life, Alert are going to be given to user to begin the dominant method if the battery level reaches essential level and method is controlled by adding High Level method into block list and begin observance it. It means by enabling the Firewall to a hi-power consumption process.

Verifying Application Performance:

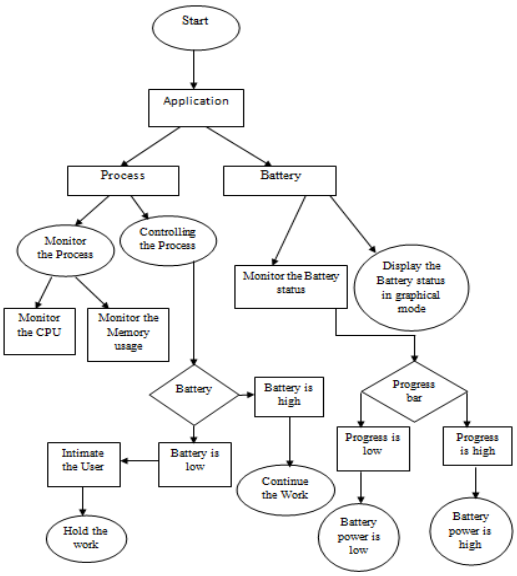

Fig2: Process Implementation flowchart

In this module we display the CPU usage, power usage and current status of laptop and all this information's are displayed with the help of graphical diagram.

The graphical presentation for the processor utilization and control are presented with the help of visual studio C++.The power consumption for the proposed technique is smaller than for DVFS at the cost of higher performance.

5. PROPOSED SYSTEM

The proposed control technique was implemented as a User space application. But power policies implemented in the Operating System may have less overhead to measure the processor utilization and to issue commands to change the processor frequency.

6. RESULTS AND DISCUSSION

In this paper, a power management policy based on control and utilization was presented. The previous approaches was based on accurate power model and performance system is available.

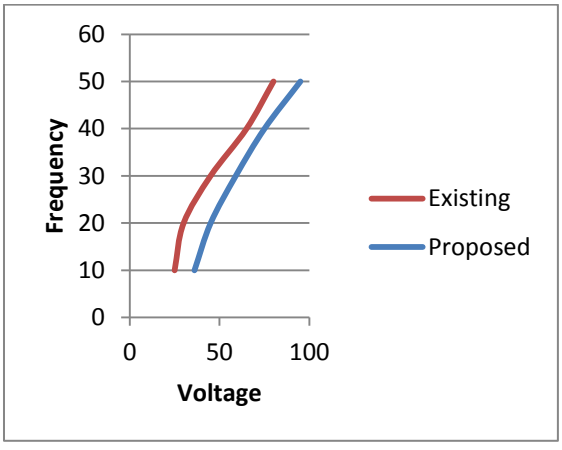

Fig3: Graph showing percentage of DVFS

It is worthwhile to notice that an identified model was used instead of a model obtained from previous knowledge of the system. The experimental results have shown that the presented power management policy may be optimized either for power consumption according to the choice of the input(User space) reference at design times.

The future work is to implement the proposed technique in identification and controlling the process by giving alert signal either by ending the process or by ignoring the process. The alerts such as STOP, CONTINUE, IGNORE are given to user in the aim of controlling the process. Since IGNORE option can be used to continue Uninterruptable process like CD Burning and Data Downloading from Internet. This will result in high Battery Performance and a low power consumption.

7. REFERRENCE

[1]Saulo.D.Luiz, Angelo Perkuisch, A.M.N.Lima, J.J.Silva, "System identification and Energy-aware processor utilization control";IEEE Trans. Consum. Electron. Vol 58, no. 1, February 2012.

[2]Jinsung cho, Ilyong cho, Dae-young kim , Ben lee, member, IEEE;"A combined approach for Qos-guranteed and low power video decoding";IEEE Trans. Consum. Electron. Vol 57,no.2, PP651-657,May 2011.

[3]Y.Yi and I.C.Park ,"A fixed point MPEG Audio processor operating at low frequency";IEEE Trans. Consum. Electron. Vol 47, PP 779-786,Nov 2001.

[4]S.O.D.Luiz , A.M.N.Lima , A.Perkuish, "Workload estimation for power management";prof. conf. ICCE'09, Las vegas ;IEEE Consumer Electronics society,2009;PP 7.2-4.

[6]K.Choi, W.Cheng, M.Pedram, "Frame based Dynamic Voltage & Frequency Scaling for an MPEG player ".Proc. of IEEE/ACM International conf. on Computer Aided Design,2002.

[7]B.I. Kim and T.G. Chang ,"A low power Multimedia system based on the microscopic dynamic voltage scaling(DVS) ",Proc. Of IEEE International conference on consumer electronics,'06.

[8]X.Liu, P.Shenoy, M.D.Corner ,"Chameleon: Application-level power Management", IEEE Trans. On Mobile Computing, Vol. 7 , no.8,2008.

[9]Z.Lu, J.Lach, M.Stan & K.Skadron, "Reducing Multimedia decode power using feedback control," Proc. Of International conference on comp.design,2003.

[10]B.Lee, E.Nurvitadhi, R.Dixit, C.Yu and M.C.Kim, "Dynamic Voltage Scaling Technique for efficient Video coding, "Journal of system Arch. Vol.41, no.10-11,2005.

[11] Saulo.D.Luiz, Angelo Perkuisch, A.M.N.Lima, J.J.Silva, H.Almeida & G.R.B.Silva ,"Identification and control for processor power management";proc. Conf. ICCE'12,Lasvegas,USA,Jan'12,PP 414-415.