Performance Analysis of 4-bit Flash ADC with Different Comparators Designed in 0.18um Technology

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ABSTRACT
This paper concerns the design of Flash type of Analog to Digital Converter (ADC) which is more likely to be used for high quality audio and video signals. It uses resistor ladder logic, comparator and encoder to convert the continuous input signal into binary form. Comparator, encoder circuits are designed using CMOS technology and its output response is obtained to meet the requirements. Comparators form the main element to design Flash ADC.

Different architectures of comparators are designed to build 4 bit Flash ADC. Dynamic characteristics of the converter are analyzed and its performance is compared with different comparator architecture. Design of these circuit use gpdk 180nm technology in cadence tool and simulated using SPECTRE.

Keywords
Flash ADC, CMOS Comparator, Open loop comparator, Latched comparator

1. INTRODUCTION
With the merit of the digital circuit that gives strong motivation to make the digital world, the main aspect in nature is that real world signals are analog signals. This naturally occurring signal is made to digital for accuracy and better quality. The trend toward increased integration of analog and digital signals need data converters such as ADC, DAC be embedded in large digital IC's. There are various architectures in ADC and selected depending on the application. One such relatively easy architecture which is used for converting continuous time varying signal to digital signal is Flash ADC [6].

Mixed signal applications require high speed low resolution ADCs which are usually implemented with flash architecture [4]. By their nature, these applications which rely on DSP will perform best when implemented on the finest geometry of CMOS process. Usually conversion is done by sampling the input signal which is then compared against reference voltage generated within ADC. Finally digital output is produced using logic circuit which is designed according to number of bits in the output.

Flash ADC is a parallel architecture which has voltage ladder logic with a comparator which produces discrete output in unary form[3]. The comparator output is fed to encoder which exactly produces digital output [10]. This type of ADC does not necessarily need sample and hold circuit for the conversion.

Comparator is the important element that forms Flash ADC. Main purpose of the comparator is to compare the input against a reference signal and produce an output depending on the input signal whether greater or lesser than reference signal [1]. Many architectures of comparators are present that exist for various purpose. In this work two stage open loop comparator, latched comparator and fully differential comparator are taken as choice so as to bring the variations in the dynamic performance of ADC. The comparators are designed in CMOS technology using 0.18um technology.

Encoder circuit implements digital logic which produces binary output. The output of encoder in flash ADC signifies the number of bits. Priority encoder is implemented using logic gates in this paper. Logic gates are realized using CMOS technology [5].

After completing comparator and encoder design, complete Flash ADC is made with these blocks and is simulated to check and compare ADC performance. Dynamic characteristic such as ENOB, SNR, SFDR, THD and conversion time for ADC with different comparators are compared to get the best architecture in terms of needed application.

In this work, section 2 describes general architecture of flash ADC section 3 discusses different comparator architecture. Encoder design is explained in section 4. Section 5 gives the detailed description of 4bit flash ADC and its performance. The design results are validated in CADENCE tool using SPECTRE simulator.

2. FLASH ADC
For high speed applications, flash ADC is often used. Flash ADC is very fast and used for low resolution application due to its parallel architecture. It is best and less complex up to 8 bits. But when the number of bits increased complexity increases since the number of comparator needed is large. The main significance of flash ADC is that they are used within pipeline and sigma delta converters.

The flash ADC consists of three main components resistor string, comparator bank, encoder logic. Sample and hold circuit is not used usually in this type. For N bit ADC, 2^N resistors and 2^{N-1} comparators and 2^{N-1} to N bit encoder is needed [2]. The block diagram for typical flash ADC architecture is shown in the Figure 1.

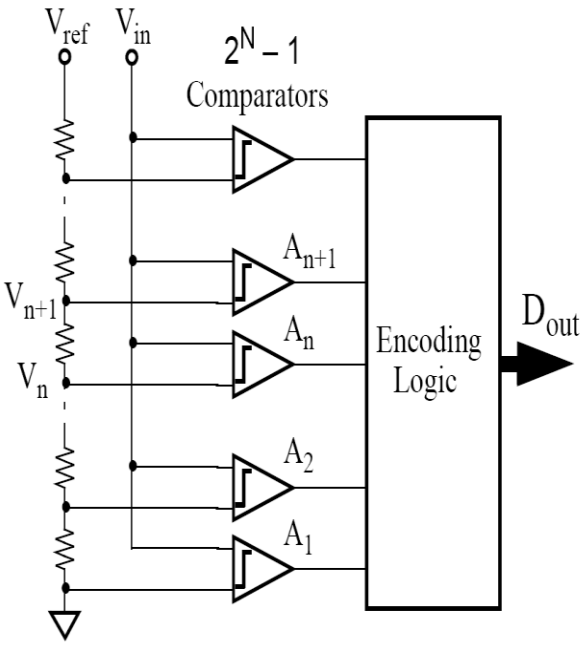

Figure 1 Flash ADC Architecture

Each resistor in the resistor string divides the reference voltage to feed the comparator. So for the input signal, if it is found to be small when compared to reference voltage means comparator produce a value of '1' and for greater voltage of input signal than reference voltage comparator produce the value of '0'. Thus the comparator bank produces the value which is unary form [5]. But for the digital processing, binary form is needed. For this purpose encoder is designed which gives digital output of binary form

3. COMPARATORS

Comparators are probably second most widely used components after operational amplifier in electronic world. Comparator by itself forms 1 bit ADC so for this reason it is used abundantly in almost all the type of ADC [1]. Comparator is classified as open loop comparator and regenerative comparator. The difference in the classification is because of the feedback given to the circuit.

3.1 Two Stage Open Loop Comparator

Two stage open loop comparator is basically an Opamp without any feedback or compensation [10]. Two stage Opamp with high gain is used as an comparator to produce discrete output. This kind of comparator design is very simple and their performances are similar in a way as an Opamp. This design produces an output swing which is more compatible to drive digital logic circuit.

The schematic for the two stage open loop comparator is shown in the figure 2

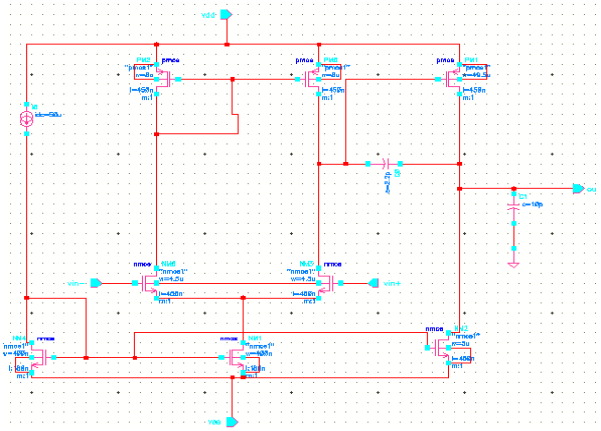

Figure 2 Two Stage Open Loop Comparator

3.2 Latched Comparator

Latched comparator is another type of comparator which uses latch along with Opamp. Comparison of the analog input signal and reference signal is done at given time instant [7]. Working of latch used here depends on the clock signal. Thus this type of comparator is used in sampled data systems. As a result increased speed of conversion is achieved.

Opamp used in this work is two stage Opamp which is combined with D latch to form latched comparator. The schematic showing latched comparator is shown in the figure 3

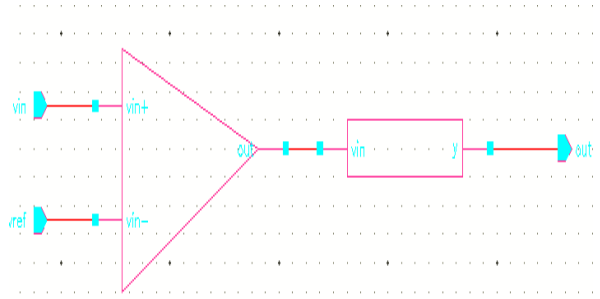

Figure 3 Latched comparator

D latch used in this work is formed using transmission gates and not gates that are realized using CMOS technology. Clock used to trigger the latch is of period 250us. The schematic showing latched comparator is given in figure 4

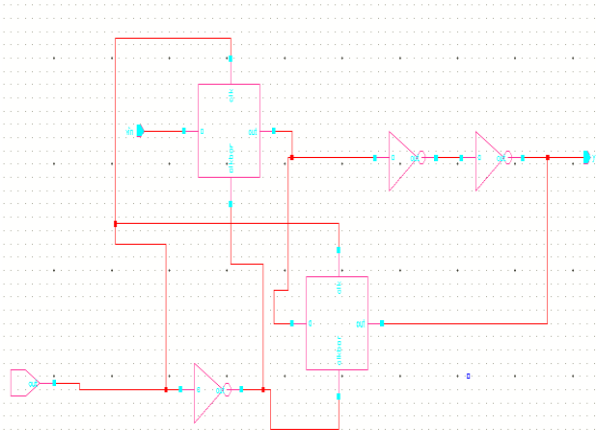

Figure 4 Schematic of D Latch

3.3 Differential Comparator

Differential comparator is a regenerative comparator which consists of three stages input pre-amplifier, a positive feedback, output buffer. The preamp stage amplifies the input signal to improve sensitivity [8]. The positive feedback stage is used to determine which of the input signal is of larger value. The output buffer amplifies this signal information and gives digital output signal [3].

Differential comparator in this paper is designed using 0.18um technology. This is a high performance comparator which increases the speed of conversion when it is used in data converters. The schematic showing the differential comparator is given in figure 5

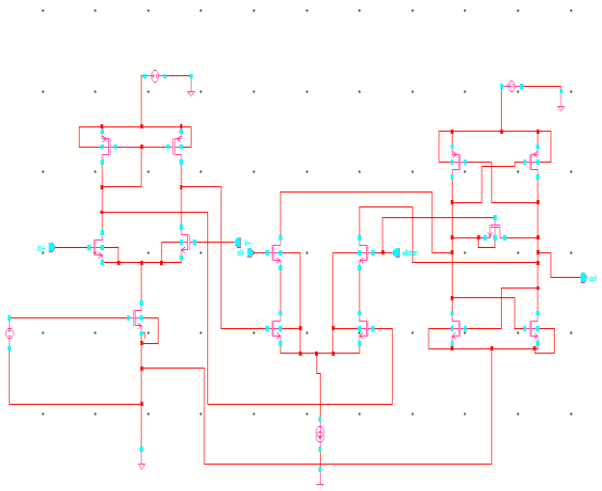

Figure 5 Differential Comparator

4. Encoder

Encoder is a digital circuit which is realized using different logic gates. The main function of the encoder is to convert the discrete output of comparator into digital form which will be obtained as per the required number of bits.

Priority encoder is taken as a choice of design which compresses the comparator output having multiple binary inputs into small digital number of output [4]. This encoder depends on the priority of the input. It outputs the binary value representing highest position of active input. The logic showing the priority encoder design for 4 bit output is shown in table 1. The output equation which is obtained using the logic is given below

$$04 = i15+i14+i13+i12+i11+i10+i9+i8$$

$$03 = i15+i14+i13+i12+i7+i6+i5+i4$$

$$02 = i15+i14+i11+i10+i7+i6+i3+i2$$

$$01 = i15+i13+i11+i9+i7+i5+i3+i1$$

Table 1 can be used to design a suitable combinational circuit as shown in figure 6

Table 1 Priority Encoder Logic

Output															Input			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	4	3	2	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	x	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	1	X	x	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	1	x	X	x	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	x	x	X	x	0	1	0	1
0	0	0	0	0	0	0	0	0	1	x	x	x	X	x	0	1	1	0
0	0	0	0	0	0	0	0	1	x	x	x	x	X	x	0	1	1	1
0	0	0	0	0	0	0	1	x	x	x	x	x	X	x	1	0	0	0
0	0	0	0	0	0	1	x	x	x	x	x	x	X	x	1	0	0	1
0	0	0	0	0	1	x	x	x	x	x	x	x	X	x	1	0	1	0
0	0	0	0	1	x	x	x	x	x	x	x	x	X	x	1	0	1	1
0	0	0	1	x	x	x	x	x	x	x	x	x	X	x	1	1	0	0
0	0	1	x	x	x	x	x	x	x	x	x	x	X	x	1	1	0	1
0	1	x	x	x	x	x	x	x	x	x	x	x	X	x	1	1	1	0
1	x	x	x	x	x	x	x	x	x	x	x	x	X	x	1	1	1	1

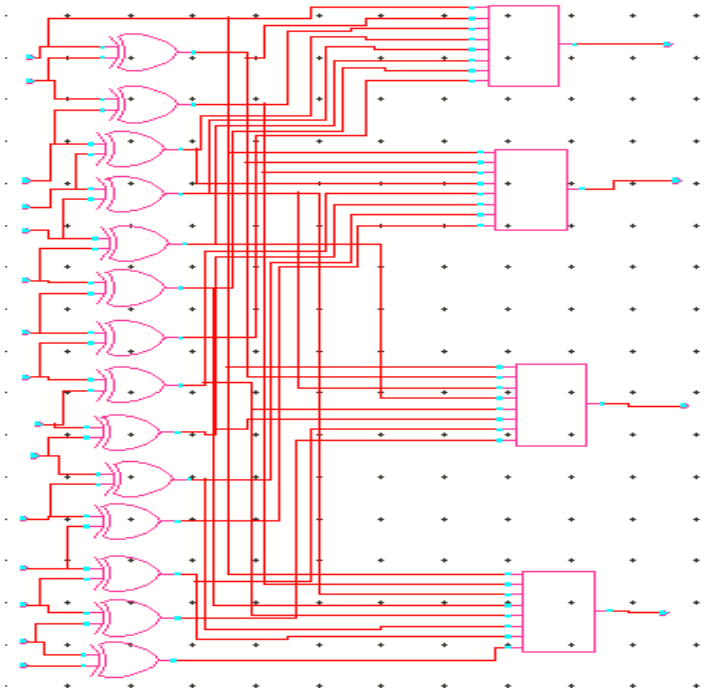

Figure 6 Priority Encoder Design

5. 4 BIT FLASH ADC

For 4 bit flash ADC, 16 resistors and 15 comparators are needed. Voltage reference is taken as 1.8 V and hence the resistor string divides the reference voltage. In general the voltage division takes place as follows

$$V_a = (M*Vref)/ 2^N$$

M= resistor tap at which voltage division occurs
N= no of bits
2^N= total number of resistors used

Table 2 shows voltage division at different taps for resistor string where Vref= 1.8 V [4]

Table 2 Voltage Division by Resistor String

M	Va (V)
Tap 1	0.1125
Tap 2	0.225
Tap 3	0.3375
Tap 4	0.45
Tap 5	0.5625
Tap 6	0.675
Tap 7	0.7875
Tap 8	0.9
Tap 9	1.0125
Tap 10	1.1.25
Tap 11	1.2375
Tap 12	1.35
Tap 13	1.4625
Tap 14	1.575
Tap 15	1.6875

The above divided voltage feeds comparator. Comparator finds out whether a signal greater or smaller than input signal and produce binary output based on the comparison. Thus the row of comparators form 15 bit binary output called thermometer code (TC) which is a combination of series of zeros and ones eg., 001110001110111. Encoder takes these TC and converts it into 4 bit binary code (BC). The schematic explaining 4 bit flash ADC is shown in the figure 7

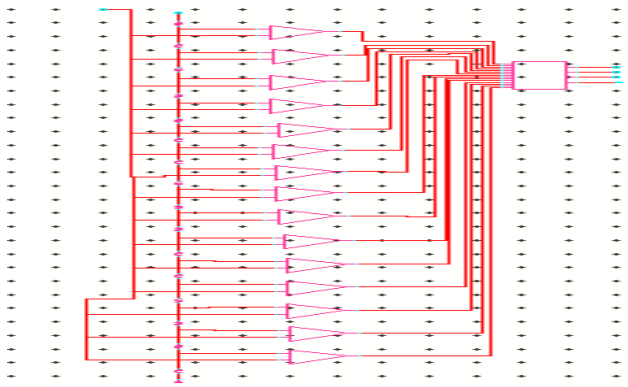

Figure 7 4 Bit Flash ADC

The output response of ADC is taken for 3 different comparator architecture embedded in Flash ADC

5.1 Output for Open Loop Comparator ADC

Though this comparator architecture gives high speed of conversion, but when comparing with other architectures it is found to be slow in conversion. Open loop comparator produces an output with conversion time of 31.25 ns. Output response is shown in the figure 8

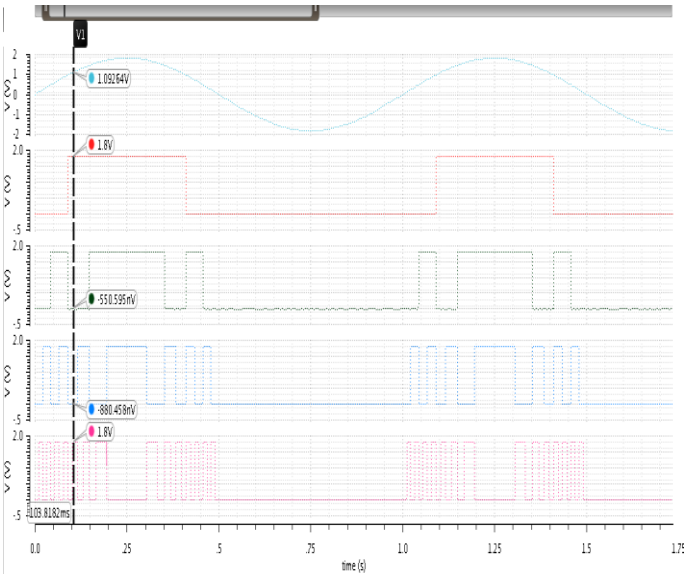

Figure 8 Output Response for Open Loop Comparator ADC

5.2 Output for Latched Comparator ADC

This type of comparator produce high speed of conversion than open loop comparator but it is of low speed when compared with differential comparator. Conversion time is around 0.134ns. Output response is shown in the figure 9

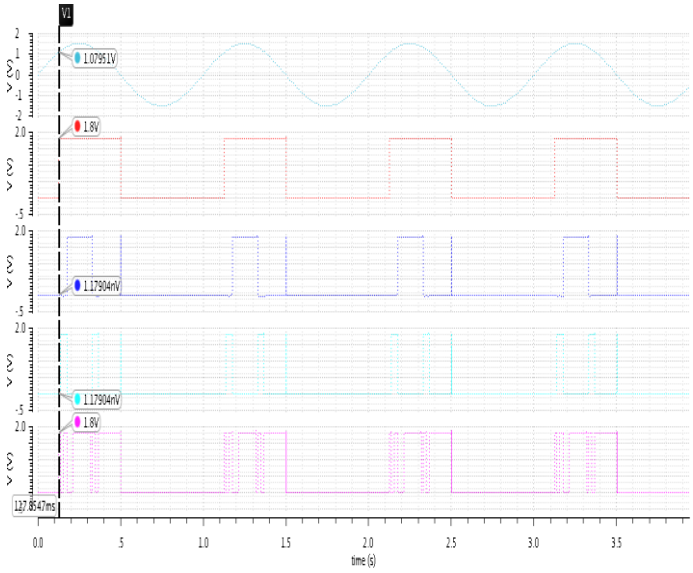

Figure 9 Output Response for Latched Comparator ADC

5.3 Output for Differential Comparator ADC

Differential comparator is found to best among the other two in terms of speed of conversion. The conversion time is found to be 0.057ns. Output response is shown in the figure 10

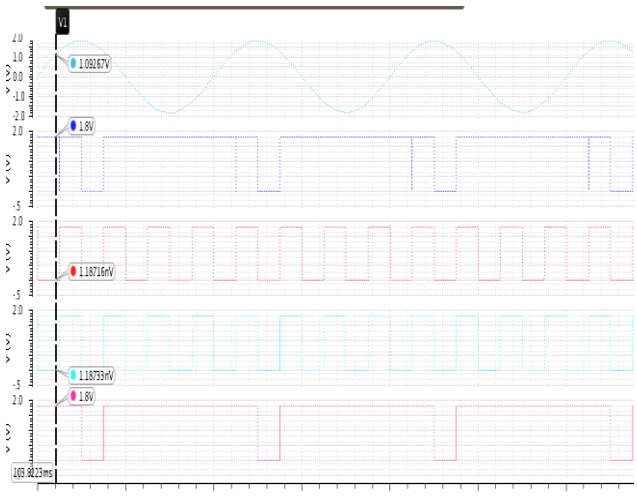

Figure 10 Output Response for Differential Comparator ADC

Dynamic characteristics of ADC is obtained using spectrum analysis and it is found that differential comparator ADC provides better performance than other two architectures. The comparison table showing the difference is given in the table 3

Table 3 Comparison of Flash ADC Characteristics with Different Comparators

Parameters/ type of adc	Open loop comparator ADC	Latched Compara tor ADC	Differential comparator ADC
CONVERSION TIME (ns)	31.25	0.134	0.057
ENOB (bits)	3.233	3.31	3.34
SNR (db)	16.14	19.76	20.15
SFDR (db)	9.44	12.77	9.54
THD (%)	38.11	43.86	47.4

6. CONCLUSION

The schematic of comparator and priority encoder stage are designed and integrated. Flash ADC dynamic performance is compared by using different comparator architectures and found that differential comparator produces better performance. This integrated flash ADC is operated at 4 bit with analog input voltage of 0 to 1.8 V with supply voltage of ± 1.8 V. The ADC is designed and implemented using gpdk 180nm CMOS technology using Cadence Virtuoso tool and simulated using Spectre simulator

7. ACKNOWLEDGEMENT

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