Efficient Design of Low Power ALU using PTL-GDI Logic Full Adder

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ABSTRACT

In this paper, we proposed a low power 1-bit full adder (FA) with 10-transistors and this is used in the design ALU. 16-bit ALUs are designed and compared with the existing design. The proposed design consists of PTL-GDI adder and mux circuits. By using low power 1-bit full adder in the implementation of ALU, the power and area are greatly reduced to more than 50% compared to conventional design and 30% compared to transmission gates. So, the design is attributed as an area efficient and low power ALU. This design does not compromise for the speed as the delay of the full adder is minimized thus the overall delay. The leakage power of the design is also reduced by designing the full adder with less number of power supplies to ground connections. In fact, power considerations have been the ultimate design criteria in special portable applications. For large number of computations, efficient ALU is to be designed for minimum area and low-power without compromising the high speed. The proposed ALU design simulated using tanner version 13 software.

Key Words

Gate Transmission Input, Pass Transistor Logic, 10T full adder, mux.

1. INTRODUCTION

Today all the VLSI circuits operates on low power with high speed. The GDI technology and PTL technology are used achieve low power operation with minimum area consumption. In this project a full adder based on PTL-GDI logic ,which consists of 10 transistor along with 2:1 multiplexer consists of two transistor , 4:1 multiplexer consists of six transistors are used to design Arithmetic and Logic Unit(ALU). The ALU is basic unit of central processing unit which performs all the arithmetic and logical operations. Thus ALU is used in the microprocessor and act as critical component of the microprocessor mostly all the digital circuits uses ALU. Since the digital design is amazing and broad field. Achieving of low power with high speed in digital design is the challenging task makes digital design as the future growing business. The applications of digital design present in our daily life like computer, calculator, camera, mobile phone, etc.

Large gains, in terms of performance and silicon area, have been made for digital processors, microprocessors, DSPs (Digital Signal Processors), ASICs (Application Specific integrated circuits), etc. In general, "small area" and "high performance" are two constraints for any design. The IC designer's activities have been involved in trading off these constraints. In fact, power considerations have been the ultimate design criteria in special portable applications such as wristwatches and pacemakers for a long time. The objective in these applications is minimum power for maximum battery life time [12].The explosive growth in laptop and portable systems and in cellular network has identified the research effort in low power electronics. High power system may often lead to several circuit damages .Low power leads smaller power supplies and less expansive batteries. Low power is not only needed for portable application but also to reduce power of high performance system. Generally the full adder structure includes two types; they are static and dynamic types. The static type is more reliable and consumes less power. Dynamic adder is fast adder, some times more compact then static adders and suffering from charge sharing problem.

2. ARITHMETIC AND LOGIC UNIT

The Arithmetic and Logic Unit (ALU) is the critical component in the microprocessor it performs all arithmetic like addition, multiplication, subtraction, etc and logical calculations like OR, XOR, AND, NAND. In computer Central Processing Unit (CPU) is the brain of the computer and ALU is fundamental block of CPU. The processor found inside Graphical Processor Unit is also contains powerful ALU. We design ALU using full adder and the multiplexer circuits. The full adder circuits used here is single bit full adder .the multiplexer circuit is of 4X1 mux and 2X1MUX. The full adder circuits are designed PTLGDI logic style.

The multiplexer used in the ALU is for input signal selection and to determine what kind operation to performed .The multiplexer is implemented using six and two transistors .the transistor count is reduced and power consumption is also low compared to pass transistor multiplexer. This design is simple in terms of time and area consuming. The full adder performs the computing functions of ALU. The pass transistor logic reduces the parasitic capacitance and GDI logic increase the speed of the operation.

3. EXISTING SYSTEM

The existing ALU consist of eight 4Xl mux, four 2XI mux and four full adders. In proposed method full adders are designed using 8 transistors and the multiplexers were designed using pass transistor logic.

3.1 Design of Full Adder

The full adder performs the computing function of the ALU. A full adder could be defined as a combinational circuit that forms the arithmetic sum of three input bits. The table 1 shows the truth table for the full adder.

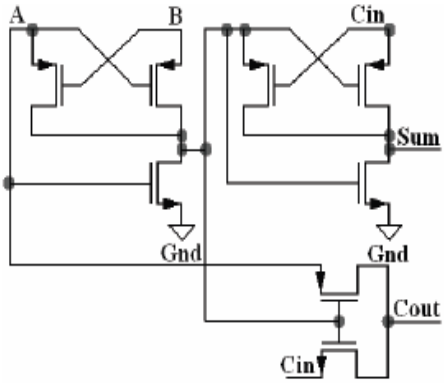

Fig 1: Circuit level diagram of proposed 8T full adder

It consists of three inputs and two outputs. In proposed method 8 transistor full adder is designed. Transistor count is reduced and thus the power consumption is also reduced [I]. Figure 1 shows the circuit level diagram of 8T full adder.

Table1.truth table for full adder

A	B	C	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

3.2 Design of Multiplexer

In existing method multiplexers were designed using pass transistor logic. By using pass transistor logic numbers of transistors were reduced and thus the power consumption also reduced [6]. Figure 2 shows the circuit level diagram of 2Xl proposed method multiplexers.

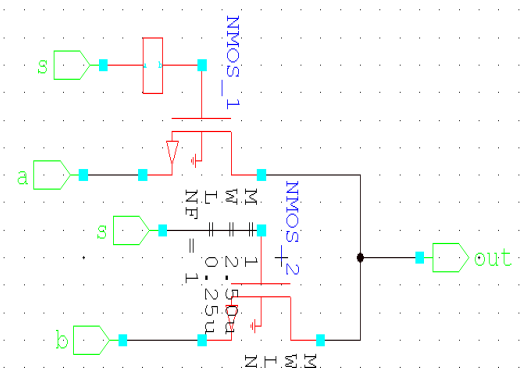

Fig 2: Schematic view of proposed 2XI mux

Existing 4Xl mux is designed using pass transistor logic. And thus the power consumption has been reduced. Figure 3 shows the schematic view of 4Xl mux.

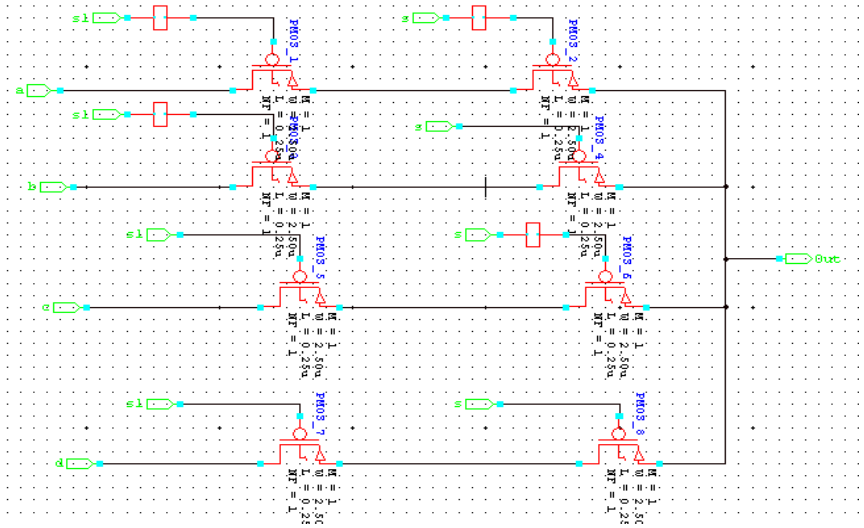

Fig 3: Schematic view of 4XI mux

3.3 Design of ALU

In existing method ALU is designed using 4Xl mux, 2Xl mux and full adder. The multiplexers were designed using pass transistor logic. And the full adder is implemented using 8 transistors. The transistor count is reduced and thus the power consumption and the area also reduced. Figure 4 shows the schematic view of proposed ALU design

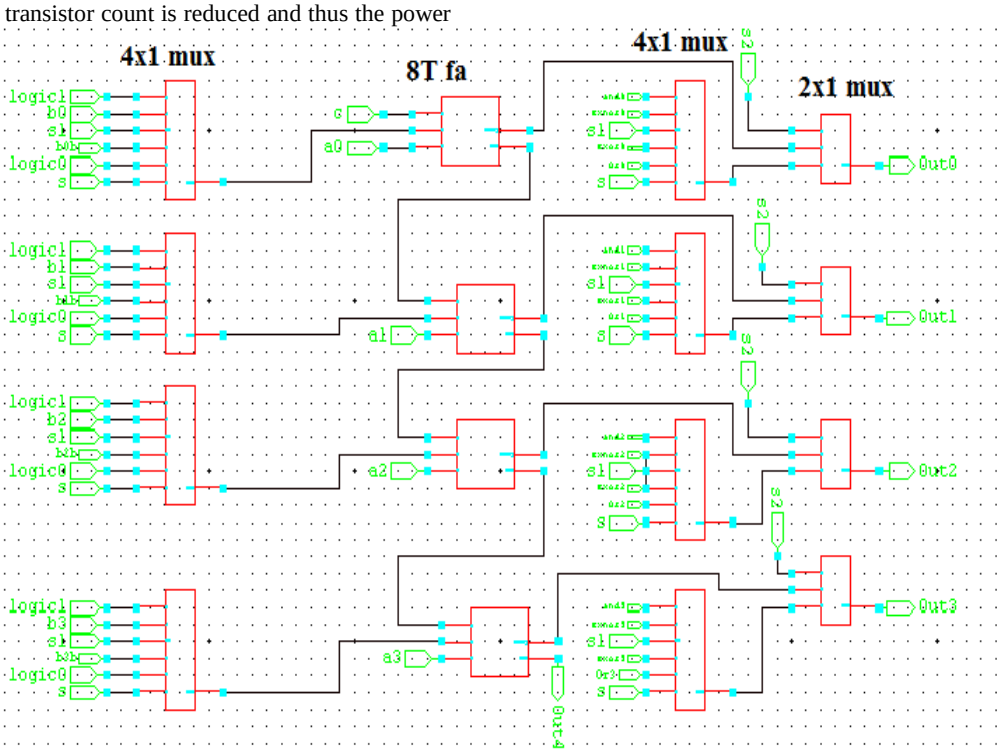

Fig 4: Schematic view of ALU design

4. PROPOSED DESIGN

The proposed design includes design of PTL-GDI full adder and the multiplexer.

4.1 Design of Full Adder:

The full adder performs the computing functions of ALU. The full adder is combinational circuit of three input s which performs the addition operation. It has three inputs and two outputs. The inputs are A, B, and carry the output sum and carry out. The architecture consists of ten transistors.

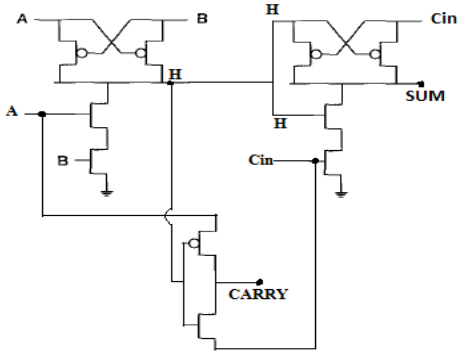

Fig 5: PTL-GDI full adder

The figure 5 shows the PTL GDI full adder. The sum output is obtained using the PTL logic and the carry output is obtained by GDI logic. The power consumption is reduced.

4.2. Design of Multiplexer:

The multiplexers have been used in the ALU design for input and output signal selection Multiplexers were implemented using six transistors and two transistors .the output of the 4X1 multiplexer is passed as input to the full adder circuit. A combination of the 2X1 multiplexer, 4X1 multiplexer at the input and at output stages selects the signals depending upon the operations to be performed. The figure shows 6 and figure 7 six transistor 4X1 mux and two transistor 2X1 mux.

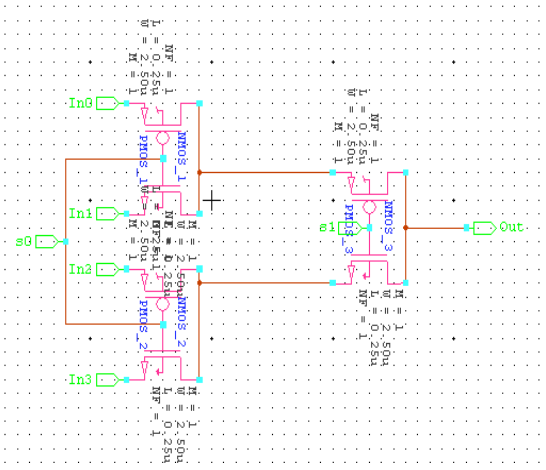

Fig 6: 4X1 multiplexer.

The ALU consist of eight 4X1 multiplexer and four 2X1 multiplexer and four full adders. The four bit ALU is designed in 180 nm technology. For increment and decrement logic 1 and logic 0 is applied for multiplexer input. The complement of b is used for the subtraction operation. Thus the full adder performs subtraction operation using the two's complement method. An increment operation is analyzed as adding '1' to the addend and the decrement operation is analyzed as subtraction.

Table 2.Truth table for 2x1 multiplexer.

S1	S2	OUTPUT
0	0	In
0	1	In1
1	0	In2
1	1	In3

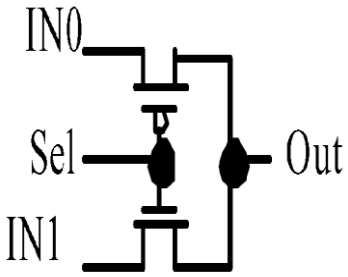

Fig 7: 2X1 mux using two transistor.

4.3 Design of ALU

The proposed ALU has four 2X1 multiplexer and eight 2X1 multiplexer and four full adders. The output is taken across the 2x1 multiplexer. The figure 8 shows the schematic of ALU

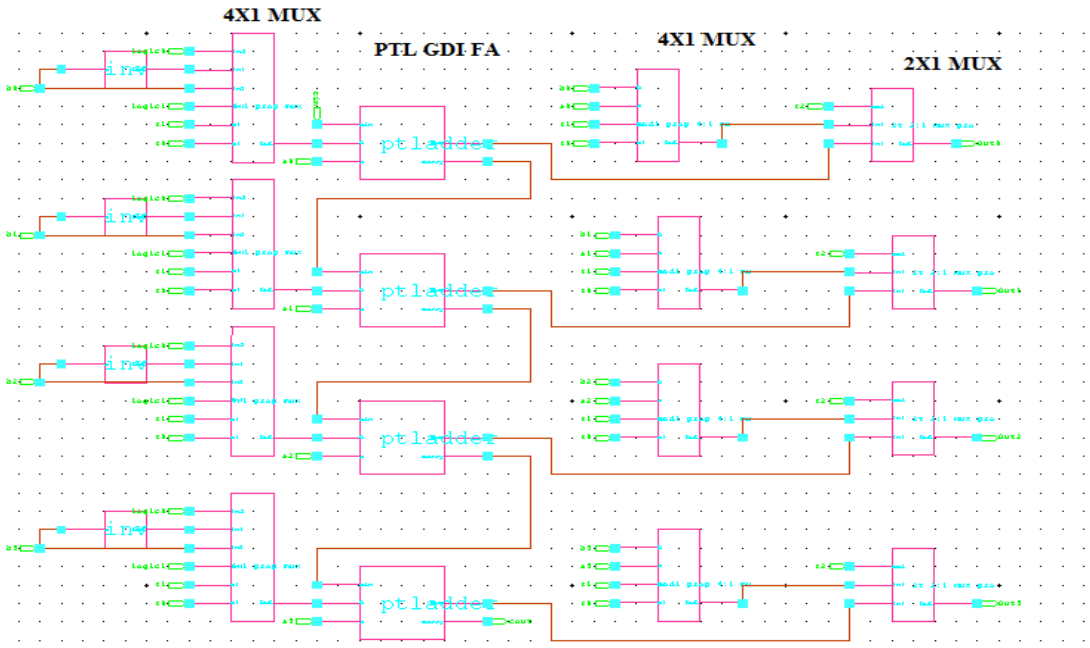

Fig 8.schematic view of 4 bit ALU

5. RESULTS AND DISCUSSIONS

The proposed architecture of 4x1 mux, 2X1 mux and full adder designed and the output waveforms are generated. The powers results of the existing design and the proposed design are tabulated .We perform the simulations using tanner EDA Tool in 125nm technology with operating voltage ranging from 5v and frequency 50 MHz. The waveforms and graph comparison are shown by

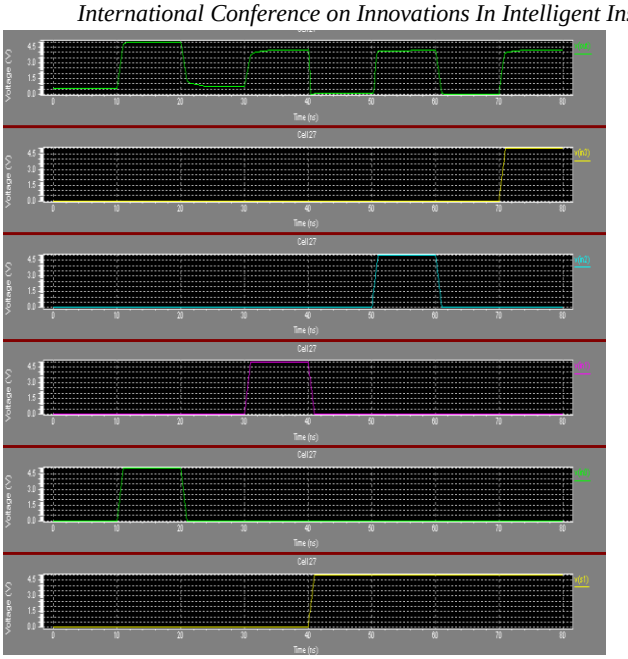

Fig : 9Waveform for 4X1 multiplexer using six transistors.

Table 3.Average power comparison table between 4X1 mux using pass transistor and 6T mux

Input (a,b,c,d,s,s1)	Average power consumed	
	Existing Module	Proposed Module
11001100 00110011 10101010 01010101 11110000 00001111	$5.338x10^{-6}$ watts	$0.254x10^{-6}$ watts

The table 3 shows power comparison table for 4X1 Mux. The 2:1 mux is basic unit for 4:1 mux which is used in our proposed design. The waveform is shown in figure 10 and the power results are shown in table 4.

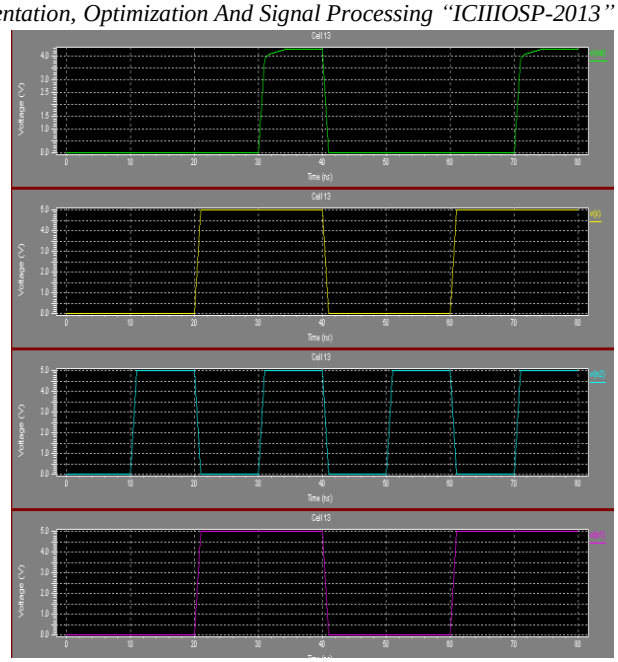

Fig: 10 Waveform for 2X1 Multiplexer using two transistor

Table 4. Average power comparison table between 2X1 mux using pass transistor and two transistor mux

Input (a,b,s)	Average power consumed	
	Existing Module	Proposed Module
11001100 00110011 11110000	$4.3447x10^{-6}$ watts	$.61221x10^{-6}$ watts

The full adder circuit consumes very less power since the GDI logic is used. The pass transistor logic reduces the number of transistor. The tanner W Edit waveform for full adder is shown below. The figure 11 shows waveform window and table 5 shows power comparison table for full adder circuits.

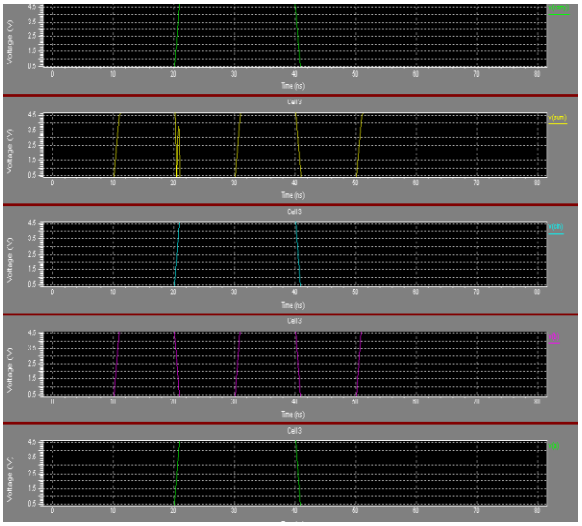

Fig: 11 Waveform for 10T full adder using PTL-GDI logic

Table 5 Average power comparison table between 10T full adder and 8T full adder

Inputs (a,b,c)	**Average power consumed**	
	Existing Module	**Proposed Module**
11001100, 00110011, 10101010	1.78709×10^{-6} watts	0.821173×10^{-6} watts

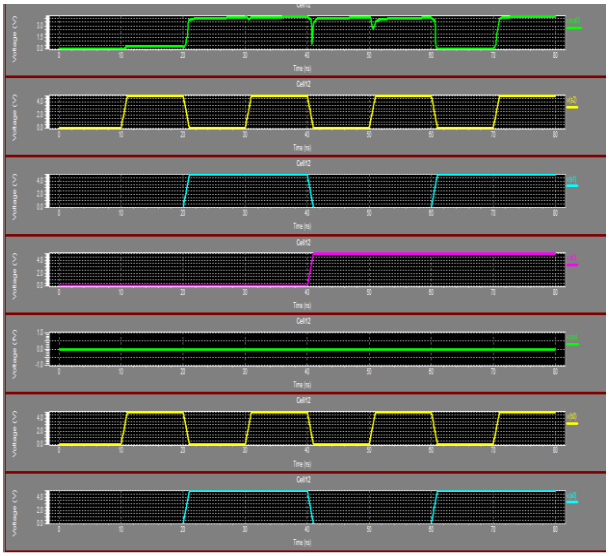

Fig12: Waveform for proposed 4-Bit ALU using 10T full adder

Table 6 Average power comparison table between Existing and proposed ALU

Inputs (a,b,c)	**Average power consumed**	
	Existing Module	**Proposed module**
11001100, 00110011, 10101010	3.0798×10^{-2} watts	3.76772×10^{-3} watts

The figure 12 shows the waveform of ALU circuit. Power Comparison chart of 4X1 mux, 2X1 mux, and Full adder is shown below which predicts that proposed design consumes less power than existing design.

Fig: 13 Power Comparison o f 4X1 mux, 2X1 mux, Full adder

The power comparison chart shown below gives comparison result for existing and proposed Arithmetic and logical unit.

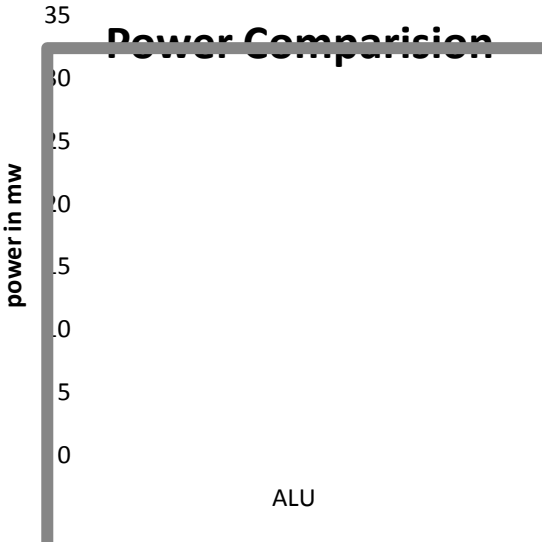

Fig 14 : Power comparision of ALU

6. CONCLUSION

In this project, the proposed ALU design gives significant reduction in power consumption. Initially, the ALU circuit is designed with 10T full adder and pass transistor based multiplexer design. The schematics are drawn and simulated. The power result shows that 8T full adder gives less power. Then the 8T full adder and transmission gate based multiplexer design is replaced with 10T full adder and new multiplexer design. The result shows that the average power consumption for the design is 60% less than pass transistor logic logic.

By comparing the average power consumption, ALU with the proposed adder and multiplexer consumes less power than other designs.

7. REFERENCES

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