Design of Mixed – Signal Integrator for RF Amplifier

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ABSTRACT
A method described in this paper is to design a mixed signal integrator, where the signal integrations performed are analog, but the results have both analog and digital signals. The function of an electronic integrator is to integrate any arbitrary analog signal exactly without saturation. The mixed signal integrator collects the signal integral further than the supply rails without operational amplifiers saturation and the operational amplifier design has been carried out using cadence tools based on 180nm technology and the simulation results are verified. The mixed signal integrator is consisting of an analog integrator (operational amplifier with feedback capacitor) with comparators, counter registers, and the logic. As a building block, the two Stage CMOS operational amplifier is designed and trade-off curves have been computed between all characteristics such as Gain, ICMRR, CMRR, Slew Rate etc., and the mixed signal integrator is promising that the strengths of analog are often weaknesses of digital, and vice versa..

Keywords
Two stage CMOS Operational amplifier, analog integrator, mixed - signal integrator.

1. INTRODUCTION
Operational Amplifier is necessary and important part of many analog and mixed (analog - digital) signal systems. The operational amplifier design continues as challenging that the transistor channel lengths and supply voltage are reduced with every generation of CMOS technologies and it is the most common building blocks used in many of the electronics system and it is familiar to analog designers. An electronic integrator has to integrate any arbitrary analog signal exactly, without op – amp saturation [1]. Applications that include analog signal processors, control systems, analog computers [6], and slope - based analog to digital (A/D) converters, filters, delta-sigma converters and modulators among others.

Frequently, integrations are performed digitally, via quadratures that involve sums. Traditional analog integrator, which places a feedback capacitor in across an operational amplifier [2], cannot integrate further than the supply rail voltage, because of saturation. In force, the supply rail voltage limits the number range of the analog integrator. Log-domain and other operations are applied before and after analog integrator increase the dynamic range by log compression [3]. This benefits noise "wash-out" of minor signals, but small signal fidelity is still negotiated.

• Analog integrators, limited by the operational amplifiers fixed gain at minimum frequency, act as first order elements [3], instead of pure integrators. This changes low frequency fidelity and drift gets worse. Also, traditional analog integrators tend to drift, show low precision (normally0.1% to 20%), and the results are sensitive to electronic noise [2-3]. Precision will become promised by inability

to attain desired values of resistors and capacitors, parasitic, intrinsic noise, and stray signals[13].

• Digital integrators need to convert analog to digital, and has to apply a numerical method [9]. Though the precision can be guaranteed, this conversion can introduce discretization errors and sampled data aliasing. The numerical method comes close to integration with a time-discrete quadrature or difference. This introduces concomitant stability problems, truncation errors, and a "time-step" parameter.

• In mixed signal electronics the analog and digital in combination can be complementary. These devices will have new functionality, or avoid limits of digital or analog alone. Present mixed signal frequently samples analog, processes by digital, and converts back to analog [1]. Mixed signal bring together special problems of suppression of noise, and isolating analog from digital, especially in CMOS [8].

This paper describes a mixed signal integrator design. Signal integrations are analog, [1] but the results are analog and digital. Analog is not sampled over time, but each time the analog integration matches unity, a counter register will be incremented. This event driven digitization at unity prevents sampled data problems and conserves results digitally, and then renders the digital portion of the integral unaffected to noise.

2. MIXED – SIGNAL INTEGRATOR
The proposed mixed-signal integrator consists (Figure. 1) of an analog integrator; the input of the analog integrator v_i given by a precharged capacitor switched into and out by 0–4 switches, a couple of comparators with reference voltages $\pm V_s$, a synchronous up - down counters, and the reset control circuit [1]. Resistor (R_C, feedback with analog integrator) is setting the time constant of charging of the precharged capacitor through the supply V_s.
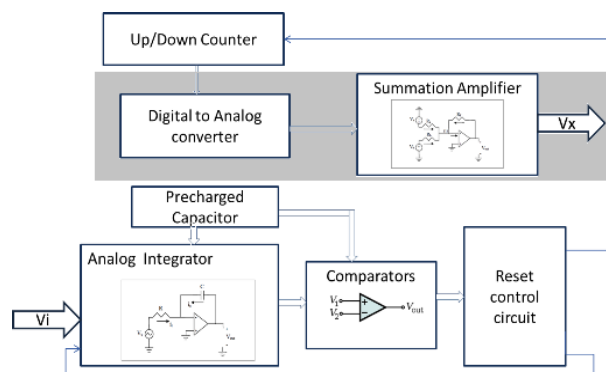

Fig 1: Mixed - signal integrator
(Elements within the shaded box (digital to analog converter, and summing op-amp) are for testing.

Elements inside the shaded box used for testing shown in the block diagram of figure1, including a digital to analog converter [DAC], a summation amplifier, and the resistor R_o (series with analog integrator output to summing amplifiers inverting terminal). R_a is the feedback resistor which is not part of the mixed signal integrator, will be added later to show computer application.

V_i is an analog input voltage applied to the analog integrator through input resistance R_i. Integrator output $V_a \approx -1/R_iC \int V_i$ dt, where C is the capacitance in feedback. As the integrator collects charge from the input currents V_i/R_i, the comparators will compare V_a with $\pm V_s$, where it has been set to lower the supply rail voltage. When $V_a = \pm V_s$, the comparators activate the hard-wired logic set in the reset control circuit, which concurrently increments or decrements the up - down counter and clears $\pm V_s$, by switching the added capacitor precharged to V_s into the input of the analog integrator, for a T timed duration. While $V_a = +V_s$, the logic will close the odd number switches and open all other switches. While $V_a = -V_s$ the logic will close the even number switches, and open all others. Once switched into the input, the precharged capacitor take out one charge unit CV_s from the feedback capacitor, while concurrently new charge accumulate from the input V_i. After termination of T, the second capacitor will be switched out and recharged by closing switches 0 and 1, and opening others. Comparator logic action avoids saturation of the analog integrator, digitizes the integral every time when V_a will be $\pm V_s$, will add the digital result to the counter register. The integer portion of the integral m in the counter register, being digital, then becomes a smaller amount of sensitive to drift and noise.

From the integral the fractional portion is held on the analog integrator as capacitor charge CV_a, or voltage V_a. Voltage V_s is equal to unity in a number system well-defined by the comparators and counter register. At that instant a comparator activates, the charge $\pm CV_s$ collected on the analog integrator. The real number ($\lambda = V_a/V_s$) stored as voltage V_a, and it is varying continuously from -1 to 1. Since the lsb (least significant bit) of the counter register decrements or increments every time when V_a is $\pm V_s$, the real number$\lambda$is representing that part of the integral having significance fewer than the counter register's lsb (least significant bit). An "analog bit," which is the contents of the analog integrator can be interpreted situated below the least significant bit of the counter register as covering integer m. Since the real number $|\lambda|$is from -1 to 1, the analog bit can fill the gaps among integers m on the number line.

Thus, x = m+λ is a real number that is continuous and equivalent to the integral. Meanwhile these integrations are time continuous and results are real numbers x, there are no rounding or truncation errors. Digitization's at unity, (when $V_a = \pm V_s$,) avoids discretization errors and aliasing difficulties linked with data sampling (there is no fractional portion to digitize). This strategy will also overcome the supply rail saturation.

3. TWO STAGE CMOS OPERATIONAL AMPLIFIER

The 2 stage CMOS operational amplifier [2] includes four major circuitries in this project - an input differential amplifier, a bias circuit, a second gain stage and a compensation circuit. Input of the operational amplifier formed by the Input Differential Amplifier block and provided

a good portion of the overall gain to improve offset performance and noise. The 2nd Gain circuit block is configured as a simple common source stage which is allowing maximum output swings. The Bias Circuit establishes the proper operating point for all transistors in its saturation region. Main use of the Compensation Circuit is to maintain stability while negative feedback is applied to the op amp. Block diagram of the operational amplifier circuit is shown in figure 2:
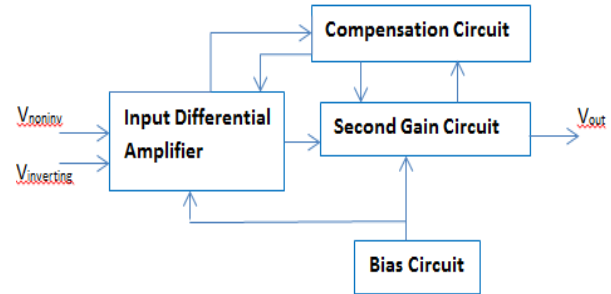
operational amplifier

Figure 3 shows the circuit configuration of an unbuffered 2 stage operational amplifier (includes the Input Differential Amplifier and the Second Gain Circuit) [8 - 15]. In the first stage of the operational amplifier transistors (**M1, M2, M3** and **M4**) form - the differential amplifier. The differential amplifier configuration is designed as differential to single ended transformation. The conversion from differential to single ended in this stage, is done by using a current mirror (**M3** and **M4)**. The current from M1transistor *is* mirrored by M3and M4transistors and subtracted from the current from the transistor M2. The differential current from **M1** and **M2** is multiplied by the output resistance of the differential input stage gives the single-ended output voltage. This establishes the input of the 2nd gain stage. The 2nd stage is a current sink load inverter. **M6$_a$, M6$_b$, M6$_c$, M6$_d$** is the driver's whereasM7acts as the load. The capacitor Cc is used to reduce the gain at high frequencies and provides the compensation for the operational amplifier. The 1st stage and the 2nd stage circuits use the same reference current; therefore, the bias currents in the two stages will be controlled together.

Table1. Operational amplifiers custom design specifications:

Specification Names	Values
Supply VDD	2.5V
Gain	$\geq$ 70dB
Gain Bandwidth	5MHz
Slew Rate	10V/u Sec
Input common Mode Range	-1 to 2 V
Power Dissipation	$\leq$ 2mV
V_{out}range	$\pm$2V
C_L	10 $_p$F

International Journal of Computer Applications (0975 – 8887)

International Conference on Innovations In Intelligent Instrumentation, Optimization And Signal Processing "ICIIIOSP-2013"

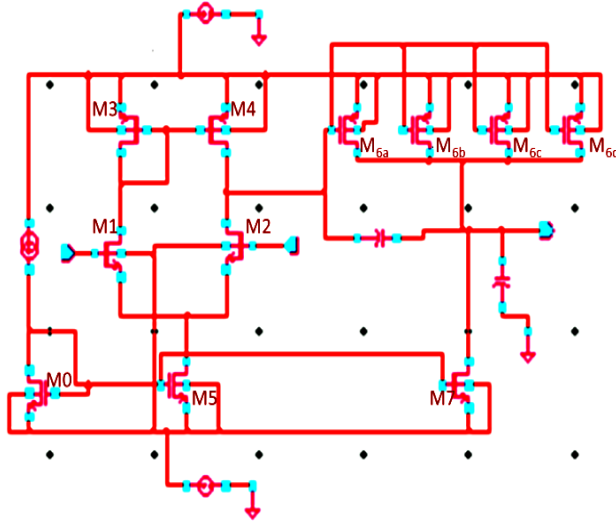# 4. OPERATIONAL AMPLIFIER CIRCUIT DESIGN

Fig 3: Circuit Configuration for a two-stage operational amplifier

The two stage CMOS operational amplifier design in this project is with an n-channel input pair. The operational amplifier uses a dual-polarity power supply (*Vdd* and *Vss*). Because of dual - polarity the ac signals will swing above and belowground and also be centered at ground. Though the Negative power supply can be a problem for a CMOS circuit because of remaining reverse bias of the source-substrate and drain-substrate p-n junctions, this problem is solved as the substrate of the nMOS transistors which should always be tied to the most negative voltage (Vss) in the circuit [4]. The power supply here is constrained within +2.5V and -2.5V (Table 1). The 1st part considered in the op amp design was the specifications are to be met. Table 1 shows their specifications.

4.1 Design methodology of operational amplifier

Determine the necessary open-loop gain (A$_o$) [2]

gm1 = gm2 = gmI, gm6 = gmII,
gds2 + gds4 = GI, and gds6 + gds7 = GII

$$Id= [\mu_{n,p}Cox(W/L)Veff2]/2 \qquad (1)$$

$$g_m=\sqrt{(2\mu_{n,p}Cox(W/L)Id)} \qquad (2)$$

$$g_m = 2 (Id/Veff) \qquad (3)$$

Slew rate $SR= I_5/C_C$ $\qquad$ (4)
$\qquad A_{v1}=- gm_{1/}(gds_2+gds_4)$
$\qquad = - 2gm_1/ (I_5 (\lambda_2+\lambda_4))$ $\qquad$ (5)

Gain stage 2
$\qquad A_{v2}=-gm_6/ (gds_6+gds_7)$
$\qquad = -gm_6/ (I_6 (\lambda_6+ \lambda_7))$ $\qquad$ (6)

$\qquad$ Gain Bandwidth GB $= gm_1/C_C$ $\qquad$ (7)
$\qquad$ Output pole $p_2= -gm_6/C_L$ $\qquad$ (8)

RHP zero $Z1= gm_6/C_C$ $\qquad$ (9)

Saturation voltage (sat) $= \sqrt{(2I_{DS}/\beta)}$ $\qquad$ (10)

It has been assumed that all transistors are in saturation for these relationships.

Open Loop Gain: It is the ratio between output voltage and differential input voltage. Because the output signal is much larger than the input signal [7], so it is commonly called as large signal voltage gain.
Slew Rate: The maximum rate of change of output voltage per unit time. (dVo/dt) The slope of the output signal is the slew rate.
Rise Time: the time required by the output to go from 10% to 90% of its final value is called the rise time.
CMRR: Common Mode Rejection ratio is the ratio between differential gain and common mode gain.

5. SIMULATION RESULTS AND DISCUSSIONS

Results of basic design of two stage CMOS Op-amp

AC Analysis: In AC- Analysis, Phase margin, Gain and GB of the OP-Amp are determined.
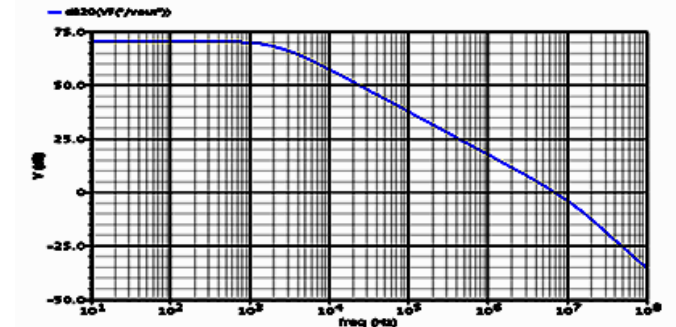- o Start frequency = 10Hz
- o Stop frequency = 100MHz

Fig 4: Frequency Response Simulation Result

Transient Analysis: The non-inverting terminal is connected to a pulse with a rise and fall time equal to 1n sec (0.1us) and a pulse width of 10us.
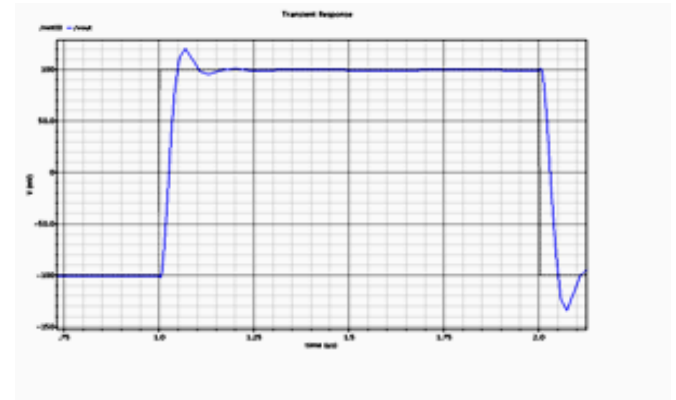

Fig 5: Simulation Result for Slew Rate

The value of pulse period is 20us. This analysis helps to determine the slew rate of the operational amplifier. Results taken from the simulation Cadence tool are as follows

- o Gain = 71.032 dB;
- o cut – off frequency = 1.3 KHz
- o Output Swing = 2.48 V ~ - 2.49
- o Slew Rate (positive) = 5.12V/us
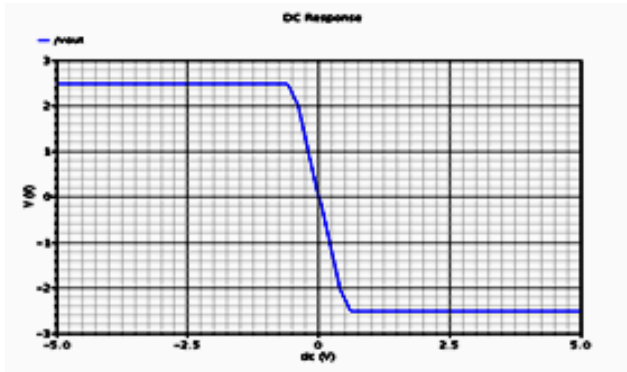- o Slew Rate (negative) = -5.06V/us

Fig 6: Simulation Result output swing

5.1 Design guidelines for Mixed – signal Integrator

Analog integrator is designed by two stage CMOS operational amplifier what has been tested already and with the input resistance and feedback capacitance that performs the mathematical operation of integration. Integrator will act as storage element that produces an output voltage which is proportional to the integral of its input voltage with respect to time. For the design of mixed – signal integrator, the two stage operational amplifier is used (analysis are taken using Cadence tool).
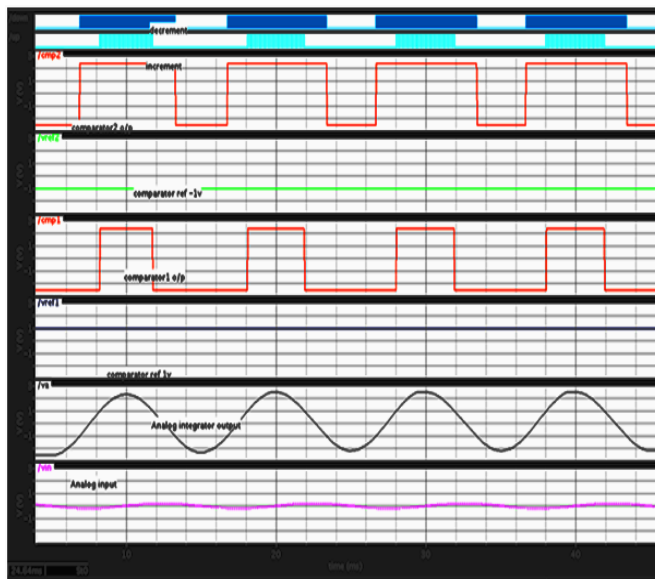

Fig 7: Simulation Result of an analog integrator with comparators

- • Comparator reference voltage V_s must allow integrator voltage V_a headroom relative to supply rail, to avoid analog integrator saturation caused by delays in charge removal during integrator resets.
- • Reset circuit must increment or decrement the counter register whenever v_a is compared with comparators reference voltage.
- • Digital to analog converter and summing amplifier in shaded box for testing of the circuit designed.

Figure7 shows the simulated sine wave result of analog integrator with comparator results. Inputs that have been given to the analog integrator are frequency = 100Hz, amplitude: 200mV, capacitor C: 100nF, resistor R1: 1.3K and the output is $V_o = 2.44\cos200\pi t$.

6. CONCLUSION

A Two Stage mixed signal (Analog- Digital) integrator based on 180nm CMOS technology described in this project, consisting of an analog integrator with comparators and counter register has been introduced, and the simulation results are analyzed two stage CMOS operational amplifier using Cadence tool. Through the mixed signal, strengths of analog can compensate weaknesses of digital, and vice versa. Specifically, the mixed signal integrator has following advantages:

- o no saturation, and effective operation beyond supply rails
- o extended low frequency bandwidth, below op-amp cut off
- o digital storage of integration results, decreasing sensitivity to noise
- o no aliasing, truncation, or rounding errors

7. ACKNOWLEDGMENTS

8. FUTURE SCOPE

As a future scope of the work, the reset control circuit can be added with comparators which cause the reset to the integrator and simultaneously increments or decrements the counter. Then as per the logic the saturation problem will be solved.

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